HITACH

LM092XMLN 491676.

- 40 characters x 2 lines
- Controller LSI HD44780 built-in (See page 115).
- +5V single power supply

MECHANICAL DATA (Nominal Dimensions)

Module size	192W x 35.5H x 15.5T (max)	mm
Effective display area	154W x 15.3H	mm
Character size (5 x 7 dots)	3.2W x 4.85H	mm
Character pitch	3.7	mm
Dot size	0.6W x 0.65H	mm
Dot pitch	0.65W x 0.7H	mm

ABSOLUTE MAXIMUM RATINGS

	min	max
Power supply for logic (VDD - VSS)	0	7.0 V
Power supply for LCD drive (VDD - VO)	0	13.5 V
Input Voltage (Vi)	VSS	VDD V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	-20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, VDD = 5.0V ± 0.25V

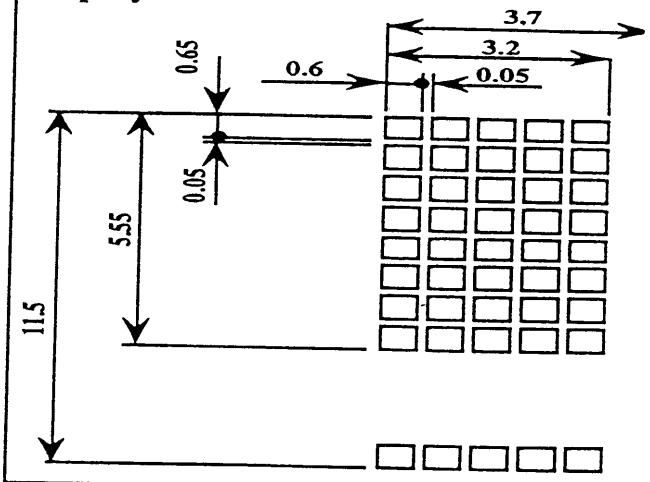
Input "high" voltage (ViH)	2.2V min
Input "low" voltage (ViL)	0.6V max
Output "high" voltage (VOH) (-IOH = 0.2mA)	2.4V min
Output "low" voltage (VOL) (IOL = 1.2mA)	0.4V max
Power supply current (IDD) (VDD = 5.0V)	1.0mA typ 3.0mA max
LED power supply current (ILED) (VLED = 5.0V)	170mA typ 250mA max
Power supply for LCD drive (recommended)	(VDD - VO) Duty 1/16
Range of VDD - VO	1.5 ~ 5.25V
Ta = 0°C	4.6V typ
Ta = 25°C	4.4V typ
Ta = 40°C	4.2V typ

Internal Pin Connection

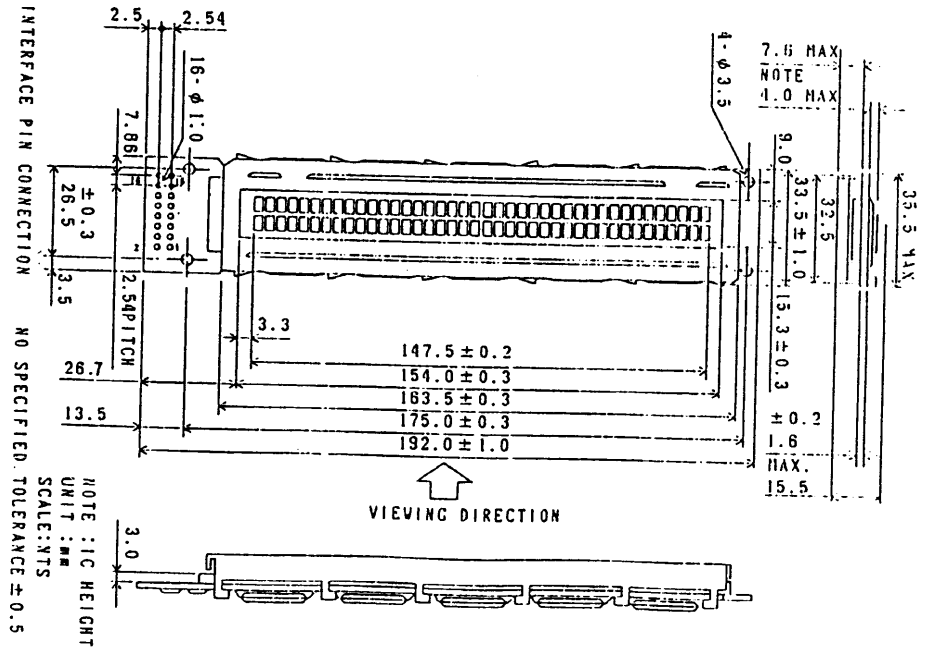
Pin No	Symbol	Level	Function	
1	VSS	-	0V	Power supply
2	VDD	-	+5V	
3	VO	-	-	
4	RS	H/L	L : Instruction code input H : Data input	
5	R/W	H/L	L : Data read (LCD - MPU) H : Data write (LCD = MPU	
6	E	H, H - L	Enable signal	
7	DB0	H/L	Data Bus Line Notes (1) and (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	VLED	-	+5V	LED power suppl
16	NC	-	-	

Notes :
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4- and 8-bit MPU's.
(1) When interface data is 4-bits long, data is transferred using only 4 buses of DB_4 ~ DB_7 and DB_0 ~ DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4-bits (contents of DB_4 ~ DB_7 when interface data is 8-bits long) is transferred first and then lower order 4-bits (contents of DB_0 ~ DB_3 when interface data is 8-bits long).
(2) When interface data is 8-bits long, data is transferred using 8 data buses of DB_0 ~ DB_7.

Display Pattern



External Dimensions



Interface Timing

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Enable cycle time	tcyc	Fig. 5, Fig. 6	1.0	-	-	µs
Enable pulse width	PWEH	Fig. 5, Fig. 6	450	-	-	ns
Enable rise/fall time	tEr, tEf	Fig. 5, Fig. 6	-	-	25	ns
RS, R/W set up time	tAS	Fig. 5, Fig. 6	140	-	-	ns
Data delay time	tDDR	Fig. 6	-	-	320	ns
Data set up time	tDSW	Fig. 5	195	-	-	ns
Hold time	tH	Fig. 5, Fig. 6	20	-	-	ns

Fig. 5 : Interface Timing (data write)

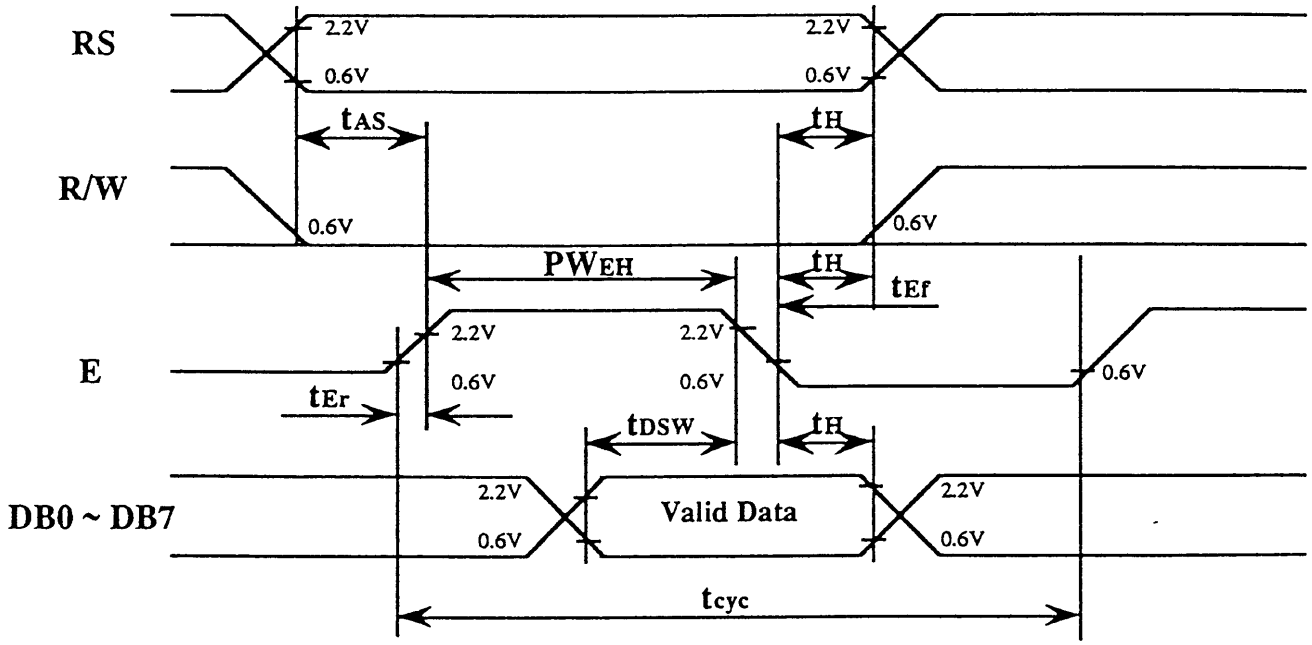
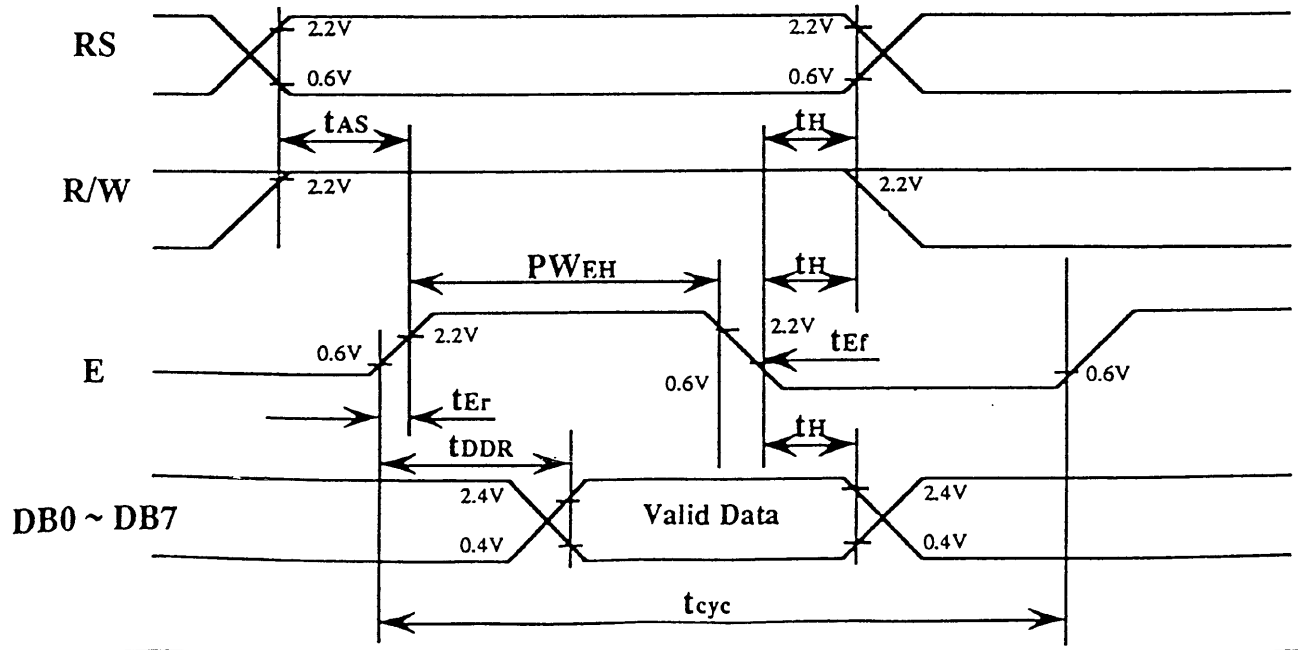
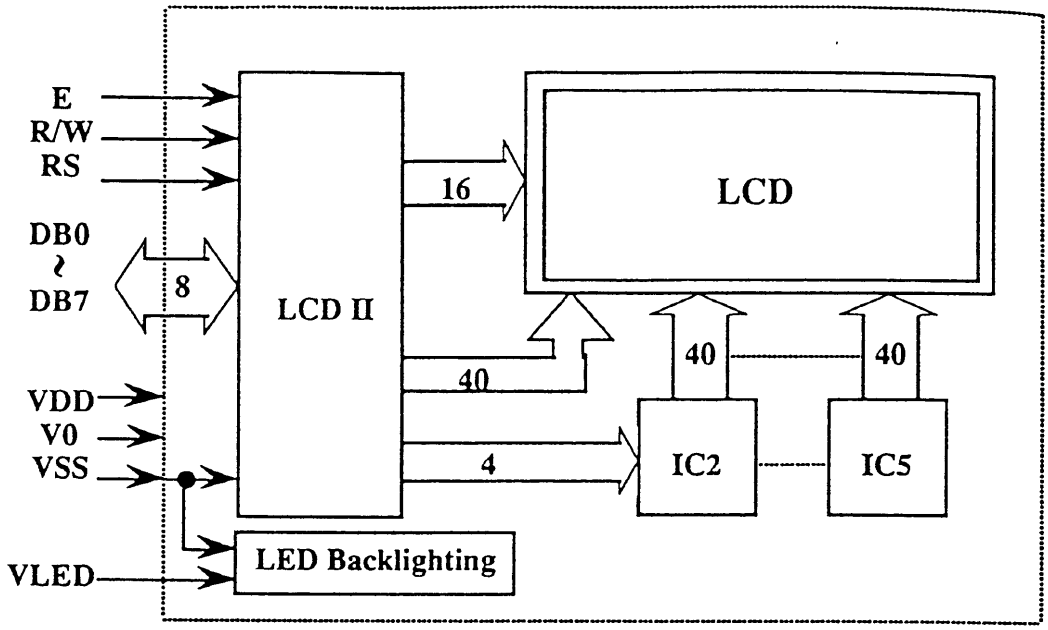


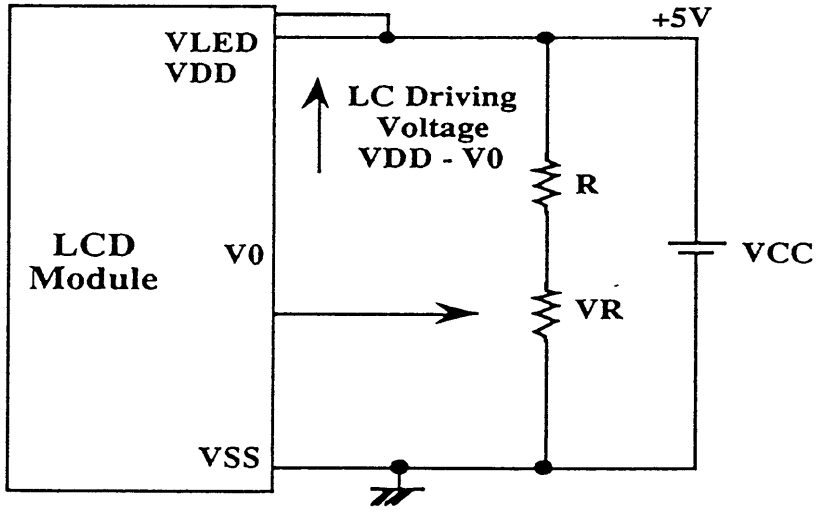
Fig. 6 : Interface Timing (data read)



Block Diagram



Power Supply



VDD - V0 : (1.5 ~ 5.25V)
R : Value must be fit for VDD - V0 ≥ 1.5V
VR : 10KΩ ~ 20KΩ