National Semiconductor

LM108AJAN

OBSOLETE
September 29, 2010

Operational Amplifiers

General Description

The LM108 is a precision operational amplifier having specifications a factor of ten better than FET amplifiers over a −55° C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with, and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices such as the 709 with 10 kΩ sources. Integrators with drifts less than 500 µV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 µF.

Features

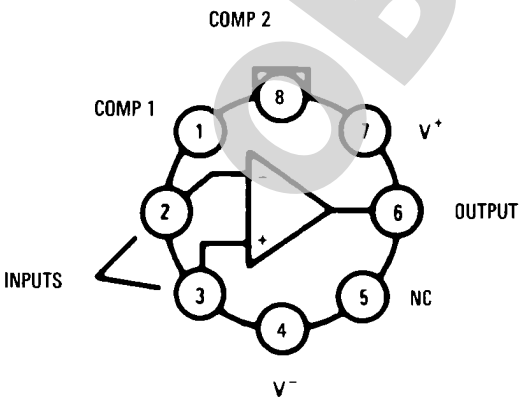
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 µA, even in saturation
- Guaranteed drift characteristics

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DISCRIPTION
JL108ABGA	JM38510/10104BGA	H08C	8LD Metal Can
JL108ABPA	JM38510/10104BPA	J08A	8LD CERDIP
JL108ABCA	JM38510/10104BCA	J14A	14LD CERDIP
JL108ABHA	JM38510/10104BHA	W10A	10LD CERPACK
JL108ABZA	JM38510/10104BZA	WG10A	10LD Ceramic SOIC
JL108ASGA	JM38510/10104SGA	H08C	8LD Metal Can
JL108ASPA	JM38510/10104SPA	J08A	8LD CERDIP
JL108ASCA	JM38510/10104SCA	J14A	14LD CERDIP
JL108ASHA	JM38510/10104SHA	W10A	10LD CERPACK

Connection Diagrams

Metal Can Package



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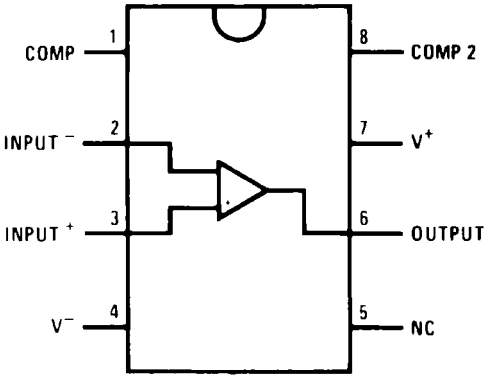
*Package is connected to Pin 4 (V−)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

See NS Package Number H08C

Dual-In-Line Package



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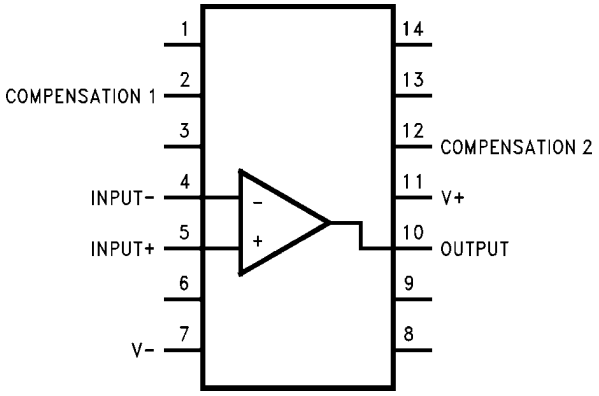
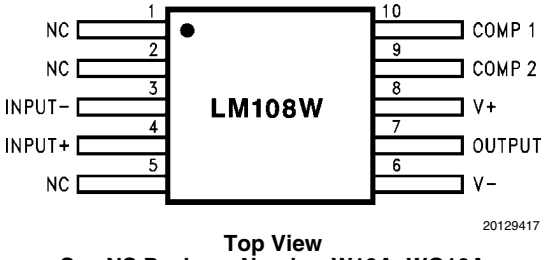
Top View
See NS Package Number J08A

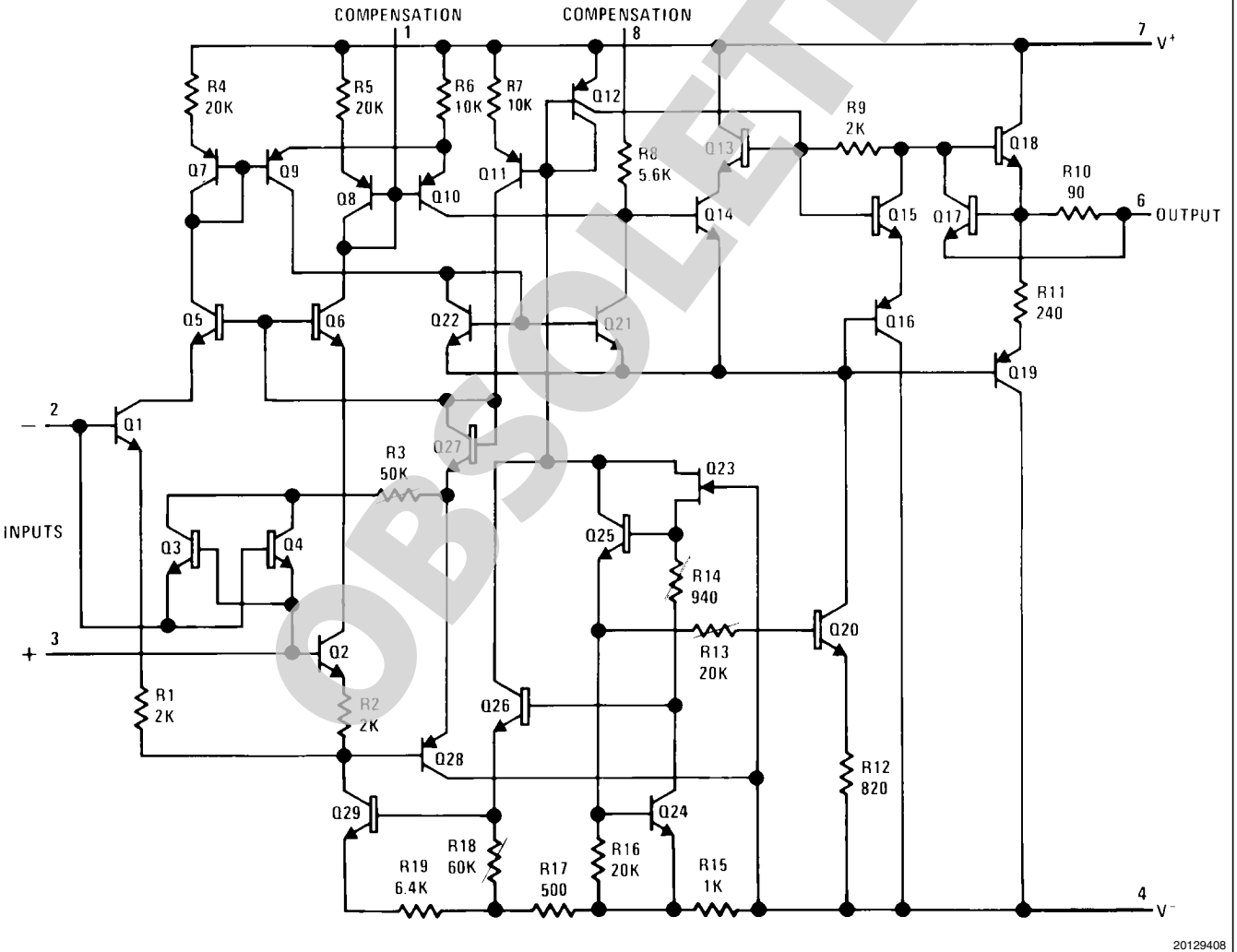


Top View
See NS Package Number J14A



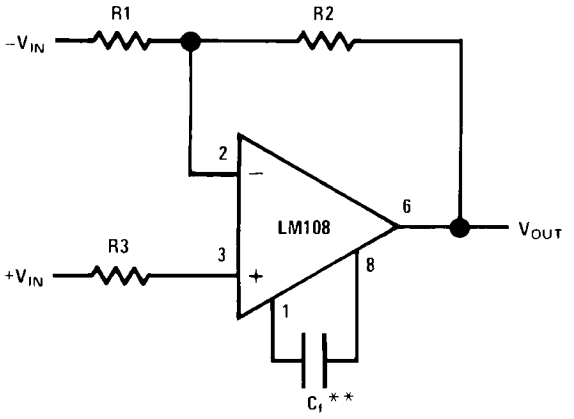
Top View
See NS Package Number W10A, WG10A

Schematic Diagram



Compensation Circuits

Standard Compensation Circuit



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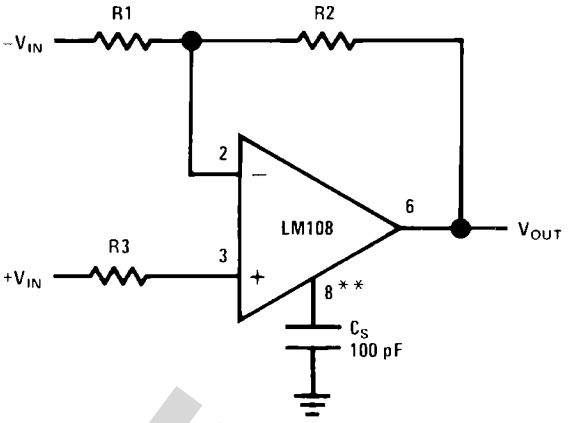
$$C_f \geq \frac{R1\ C_O}{R1 + R2}$$

C_O = 30 pF

**Bandwidth and slew rate are proportional to $1/C_f$

Alternate Frequency Compensation
(*Note 1*)



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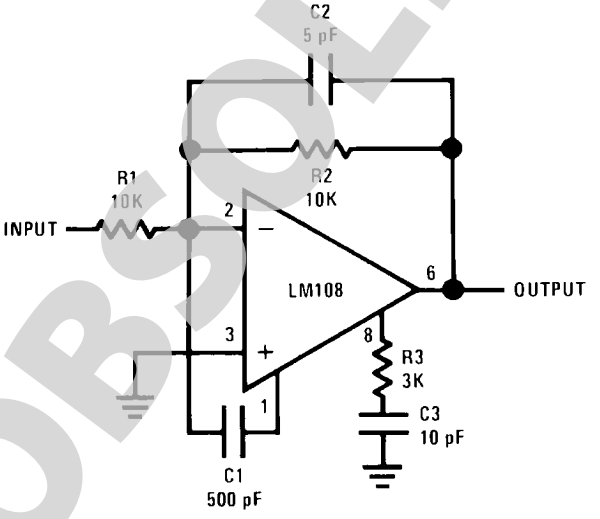
**Bandwidth and slew rate are proportional to $1/C_S$

Note 1: Improves rejection of power supply noise by a factor of ten.

Feedforward Compensation



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Absolute Maximum Ratings (*Note 2*)

Supply Voltage	±22V
Power Dissipation (*Note 3*)	
Metal Can 8LD	330mW @ +125°C
CERDIP 14LD	400mW @ +125°C
CERDIP 8LD	400mW @ +125°C
CERPACK 10LD	330mW @ +125°C
Ceramic SOIC 10LD	330mW @ +125°C
Differential Input Current (*Note 4*)	±10 mA
Differential Input Voltage(*Note 6*)	±30V
Input Voltage (*Note 5*)	±20V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$
Thermal Resistance	
θ_{JA}	
Metal Can 8LD Still Air	150°C/W
500LF / Min Air Flow	86°C/W
CERDIP 14LD Still Air	94°C/W
500LF / Min Air Flow	55°C/W
CERDIP 8LD Still Air	120°C/W
500LF / Min Air Flow	68°C/W
CERPACK 10LD Still Air	225°C/W
500LF / Min Air Flow	142°C/W
Ceramic SOIC 10LD Still Air	225°C/W
500LF / Min Air Flow	142°C/W
θ_{JC}	
Metal Can 8LD	38°C/W
CERDIP 14LD	13°C/W
CERDIP 8LD	17°C/W
CERPACK 10LD	21°C/W
Ceramic SOIC 10LD	21°C/W
Package Weight (typical)	
Metal Can 8LD	990mg
CERDIP 14LD	2,180mg
CERDIP 8LD	1,090mg
CERPACK 10LD	225mg
Ceramic SOIC 10LD	210mg
Maximum Junction Teperature	175°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD Tolerance (*Note 7*)	2000V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25°C
2	Static tests at	+125°C
3	Static tests at	–55°C
4	Dynamic tests at	+25°C
5	Dynamic tests at	+125°C
6	Dynamic tests at	–55°C
7	Functional tests at	+25°C
8A	Functional tests at	+125°C
8B	Functional tests at	–55°C
9	Switching tests at	+25°C
10	Switching tests at	+125°C
11	Switching tests at	–55°C

LM108A Electrical Characteristics

DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: $+V_{CC}$ = +20V, $-V_{CC}$ = –20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-0.5	0.5	mV	1
				-1	1	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V		-0.5	0.5	mV	1
				-1	1	mV	2, 3
				-0.5	0.5	mV	1
				-1	1	mV	2, 3
		$+V_{CC}$ = +5V, $-V_{CC}$ = -5V		-0.5	0.5	mV	1
				-1	1	mV	2, 3
Delta V_{IO} / Delta T	Temperature Coeffient of Input Offset Voltage	25°C ≤ T_A ≤ +125°C	(*Note 8*)	-5	5	µV/°C	2
		25°C ≤ T_A ≤ -55°C	(*Note 8*)	-5	5	µV/°C	3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-0.2	0.2	nA	1
				-0.4	0.4	nA	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V		-0.2	0.2	nA	1
				-0.4	0.4	nA	2, 3
				-0.2	0.2	nA	1
				-0.4	0.4	nA	2, 3
		$+V_{CC}$ = +5V, $-V_{CC}$ = -5V		-0.2	0.2	nA	1
				-0.4	0.4	nA	2, 3
Delta I_{IO} / Delta T	Temperature Coeffient of Input Offset Current	25°C ≤ T_A ≤ +125°C	(*Note 8*)	-2.5	2.5	pA/°C	2
		25°C ≤ T_A ≤ -55°C	(*Note 8*)	-2.5	2.5	pA/°C	3

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Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-0.1	2	nA	1
				-1	2	nA	2
				-0.1	3	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V		-0.1	2	nA	1
				-1	2	nA	2
				-0.1	3	nA	3
				-0.1	2	nA	1
				-1	2	nA	2
				-0.1	3	nA	3
		$+V_{CC}$ = +5V, $-V_{CC}$ = -5V		-0.1	2	nA	1
				-1	2	nA	2
				-0.1	3	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V		-16	16	µV/V	1, 2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V		-16	16	µV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±15V		96		dB	1, 2, 3
$+I_{OS}$	Short Circuit Current	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V, t ≤ 25mS		-20		mA	1, 2, 3
$-I_{OS}$	Short Circuit Current	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V, t ≤ 25mS			20	mA	1, 2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = +15V, $-V_{CC}$ = -15V			0.6	mA	1, 2
					0.8	mA	3
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ		16		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ			-16	V	4, 5, 6
$+A_{VS}$	Open Loop Voltage Gain	R_L = 10KΩ, V_O = +15V	(*Note 9*)	80		V/mV	4
			(*Note 9*)	40		V/mV	5, 6
$-A_{VS}$	Open Loop Voltage Gain	R_L = 10KΩ, V_O = -15V	(*Note 9*)	80		V/mV	4
			(*Note 9*)	40		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain	$+V_{CC}$ = ±5V, R_L = 10KΩ, V_O = ±2V	(*Note 9*)	20		V/mV	4, 5, 6

AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC $+V_{CC}$ = +20V, $-V_{CC}$ = -20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
TR_{TR}	Transient Response Rise Time	R_L = 10KΩ, C_L = 100pF, f < 1KHz, V_I = +50mV			1000	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	R_L = 10KΩ, C_L = 100pF, f < 1KHz, V_I = +50mV			50	%	7, 8A, 8B
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		0.05		V/µS	7, 8A, 8B
−SR	Slew Rate	A_V = 1, V_I = +5V to -5V		0.05		V/µS	7, 8A, 8B
NI_{BB}	Noise Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			15	µVrms	7
NI_{PC}	Noise Popcorn	BW = 10Hz to 5KHz, R_S = 100KΩ			40	µVpk	7

DC Parameters Drift Values

The following conditions apply to all the following parameters, unless otherwise specified.

DC $+V_{CC} = +20V$, $-V_{CC} = -20V$, $V_{CM} = 0V$, $R_S = 50\Omega$

Delta calculations performed on JAN S devices at group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-0.25	0.25	mV	1
$\pm I_{IB}$	Input Bias Current			-0.5	0.5	nA	1

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_D$max = ($T_J$max - T_A) / θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 4: The inputs are shunted with back-to-back diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 5: For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.

Note 6: This rating is ±1.0V unless resistances of 2KΩ or greater are inserted in series with the inputs to limit current in the input shunt diodes to the maximum allowable value.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Note 8: Calculated parameter

Note 9: Datalog reading in K = V/mV

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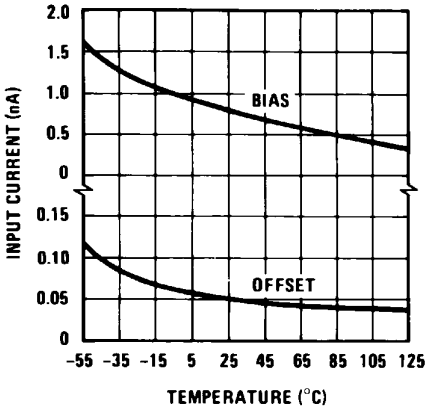
Typical Performance Characteristics

Input Currents



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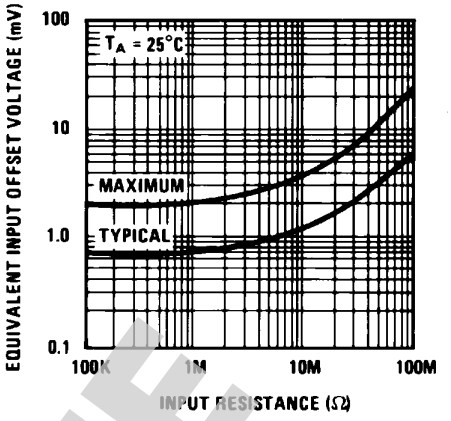
Offset Error



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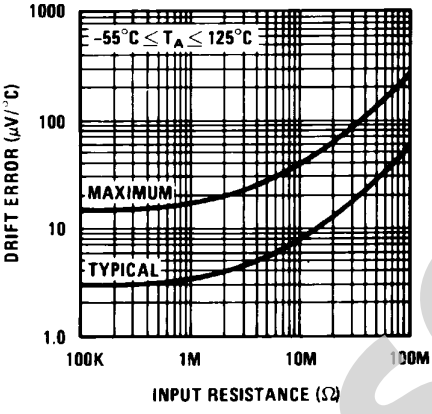
Drift Error



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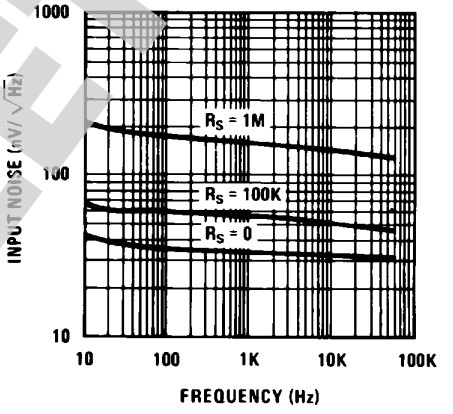
Input Noise Voltage



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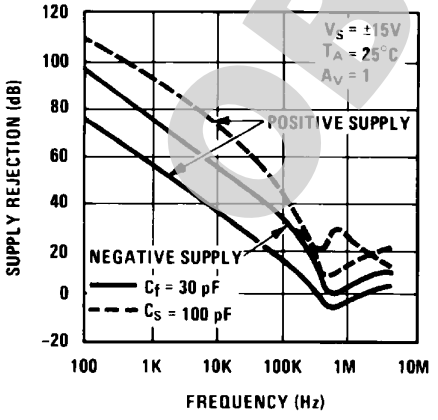
Power Supply Rejection



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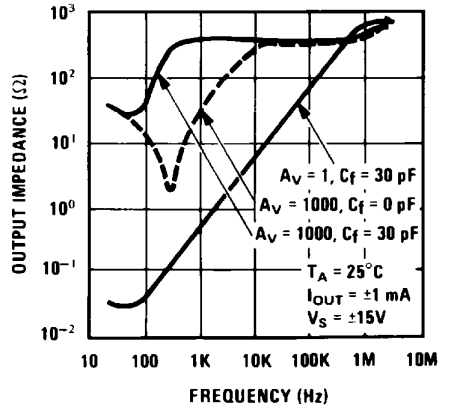
Closed Loop Output Impedance



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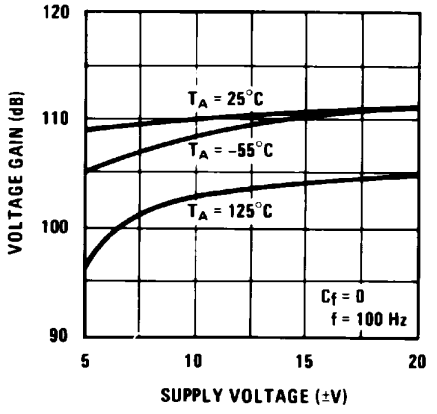
Voltage Gain



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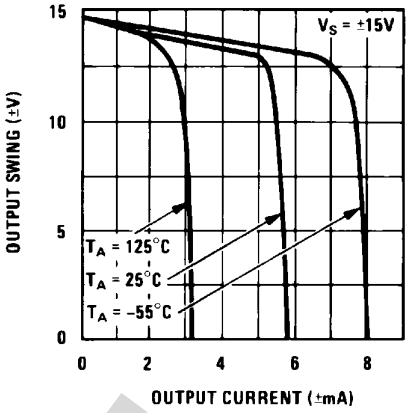
Output Swing



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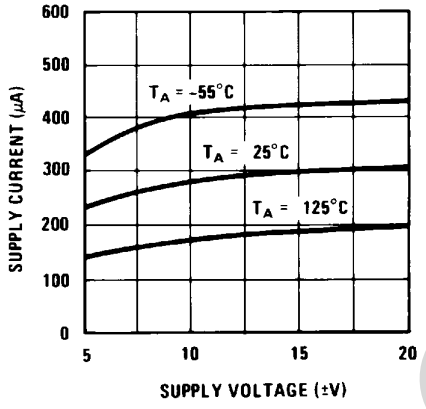
Supply Current



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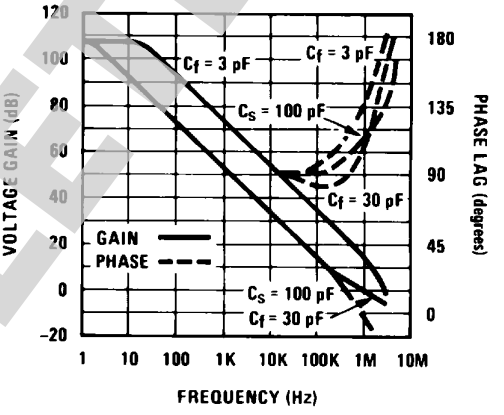
Open Loop Frequency Response



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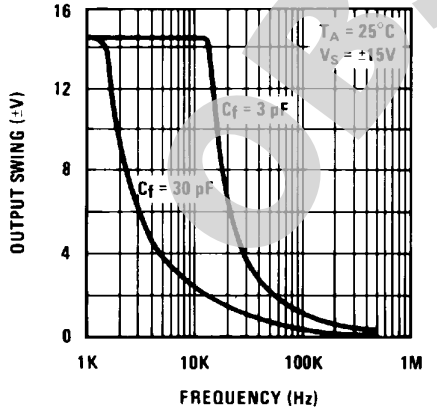
Large Signal Frequency Response



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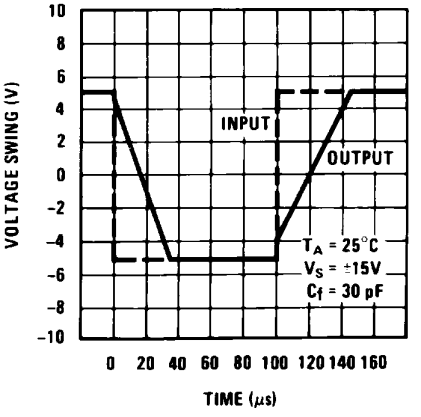
Voltage Follower Pulse Response



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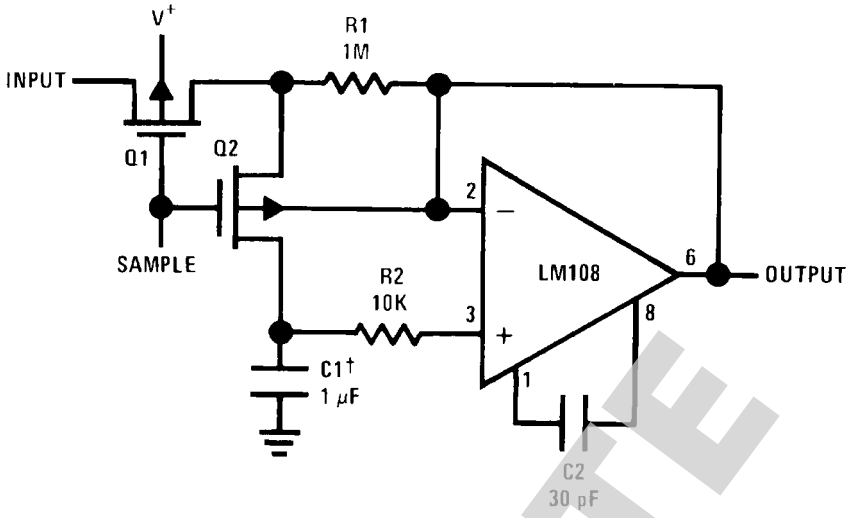
Typical Applications

Sample and Hold



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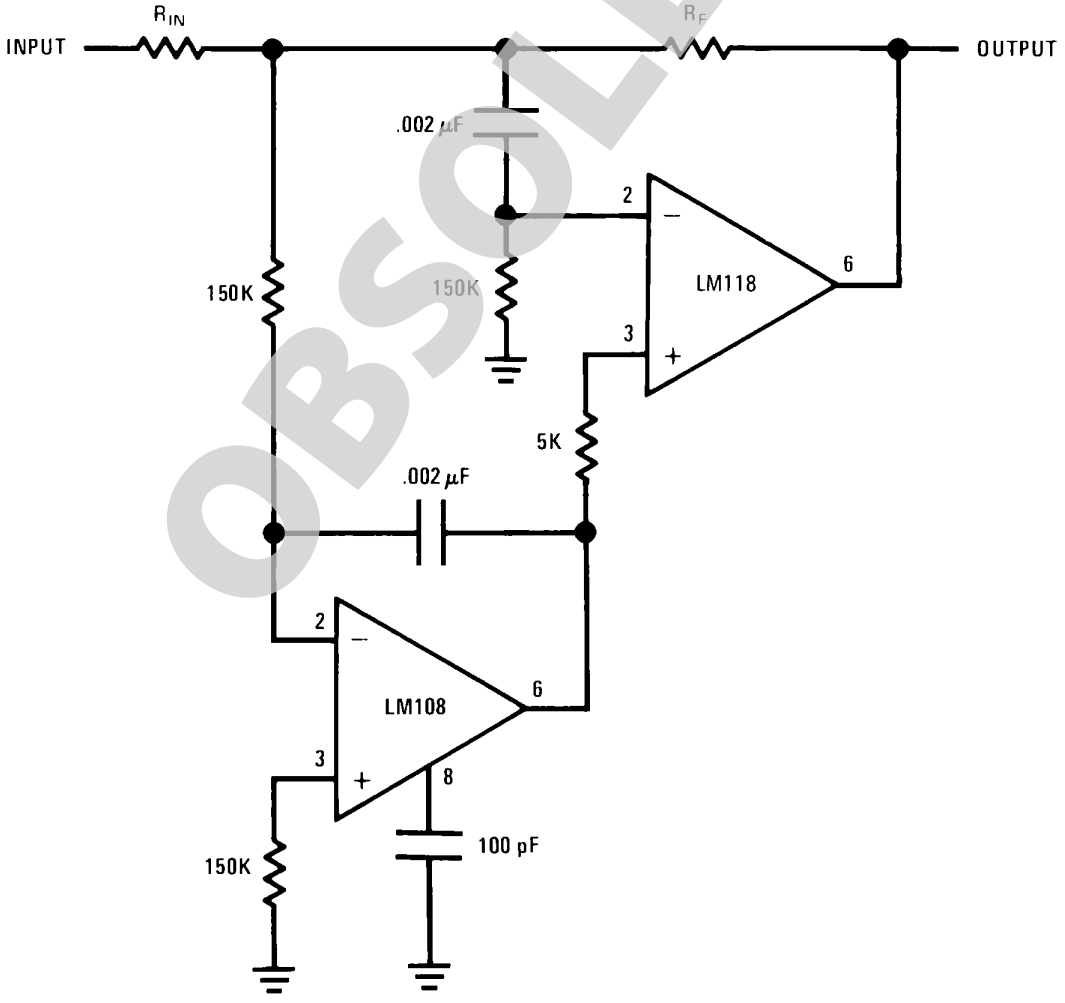
†Teflon polyethylene or polycarbonate dielectric capacitor
Worst case drift less than 2.5 mV/sec

High Speed Amplifier with Low Drift and Low Input Current



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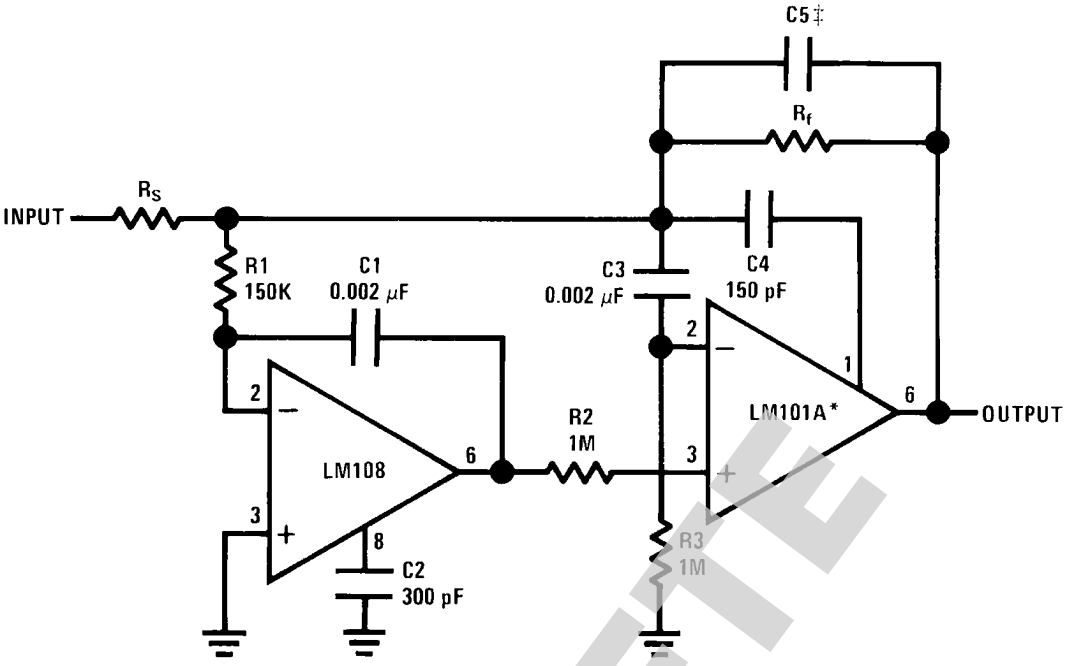
Fast Summing Amplifier (*Note 10*)



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$$\ddagger C5 = \frac{6 \times 10^{-8}}{R_f}$$

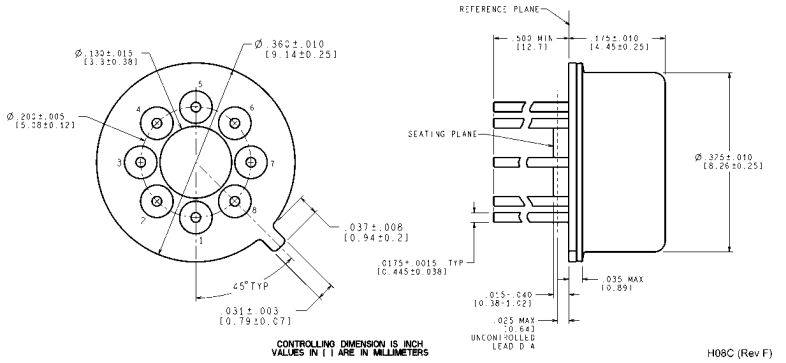
*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

Note 10: Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/µS

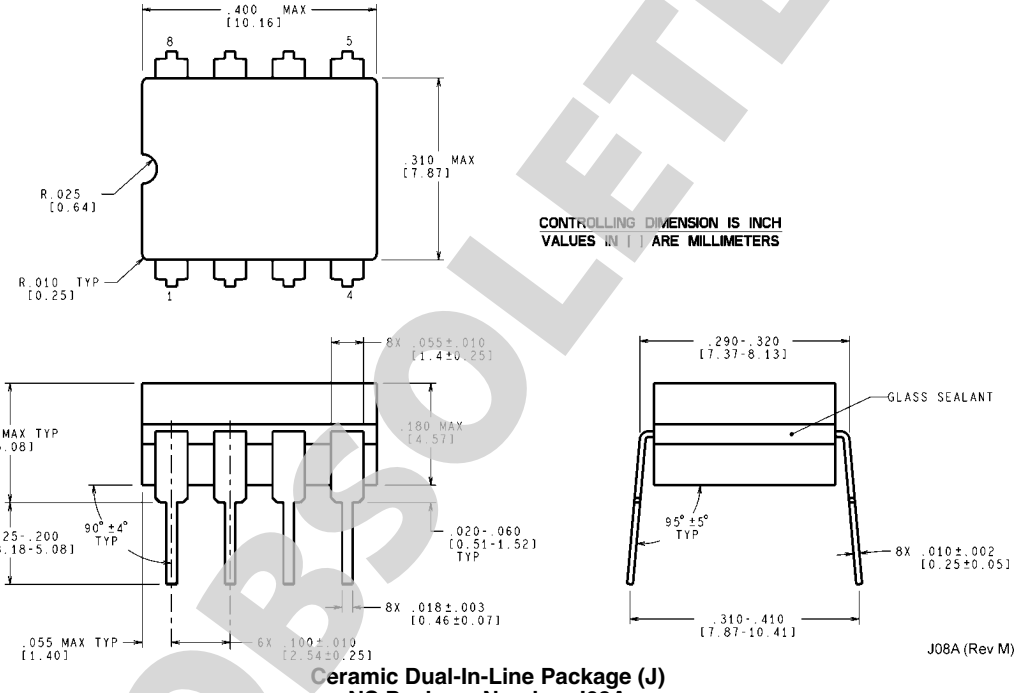
Revision History Section

Date Released	Revision	Section	Changes
02/25/05	A	New release, corporate format	1 MDS data sheets converted into one Corp. datasheet format. MJLM108A-X Rev 2A0. MDS will be archived.
01/05/06	B	DC Electrical's	All temps. +Ios from -15 mA Min to -20 mA Min and -Ios from +15 mA Max to +20 mA Max
09/24/10	C	Obsolete Data Sheet	Revision C, End of Life on Product/NSID Dec. 2008/09 Obsolete Data Sheet

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C



Ceramic Dual-In-Line Package (J)
NS Package Number J08A

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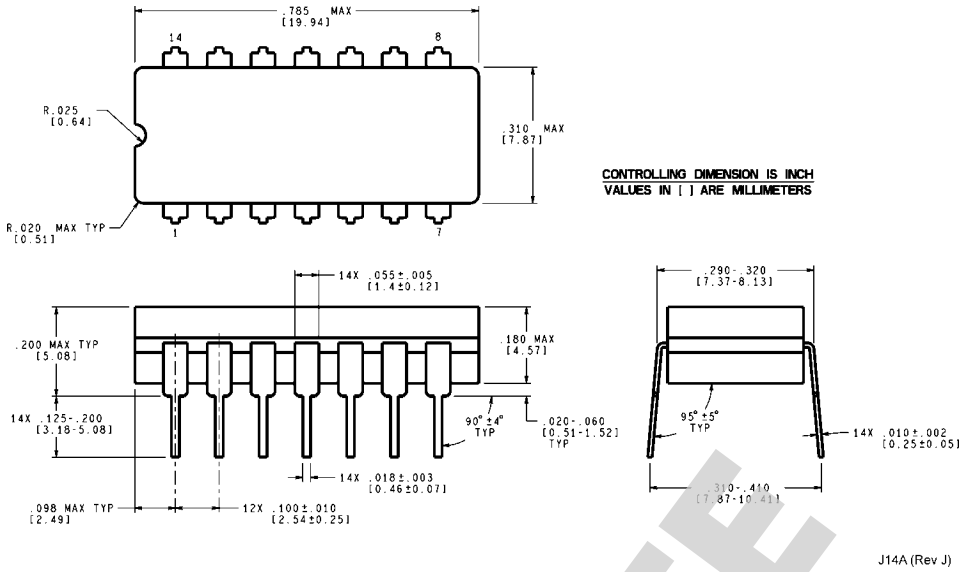
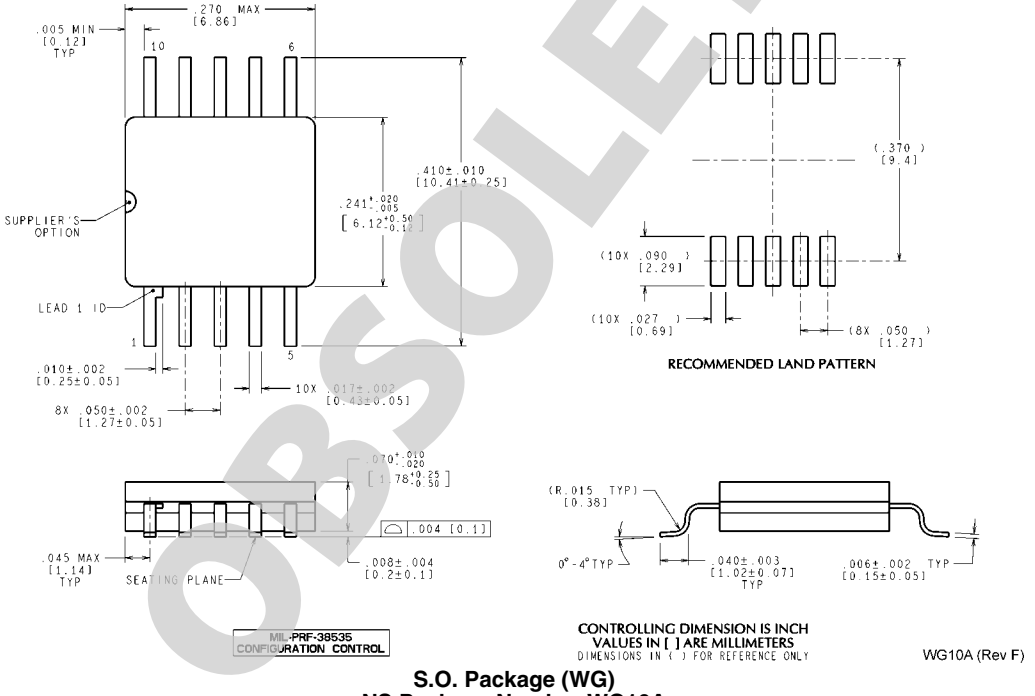
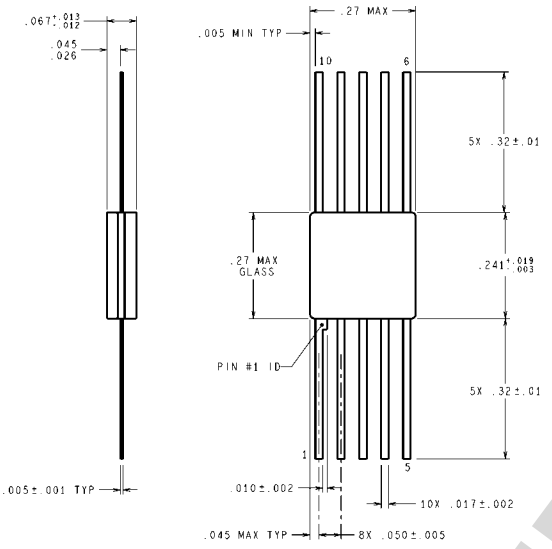


Ceramic Dual-In-Line Package (J)
NS Package Number J14A



S.O. Package (WG)
NS Package Number WG10A



DIMENSIONS ARE IN INCHES

W10A (Rev H)

Ceramic Flatpack Package (W)
NS Package Number W10A

201294 Version 3 Revision 3 Print Date/Time: 2010/09/29 22:46:28

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