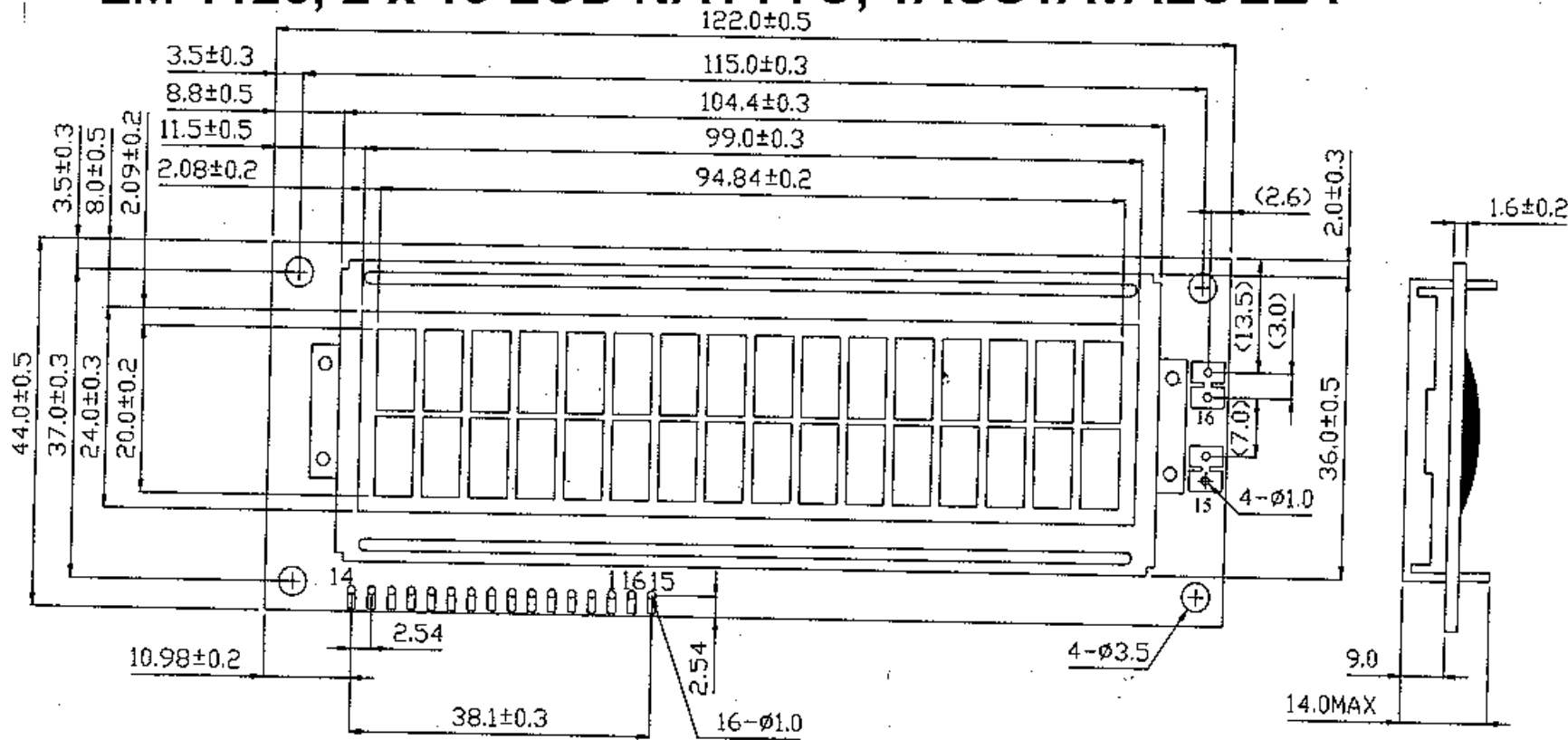


LM 1125, 2 x 16 LCD NÄYTTÖ, TAUSTAVALLOLLA



7. OUTLINE DIMENSION

15 = TAUSTAVALON KATODI 16 = TAUSTAVALON ANODI
 KÄYTTÖJÄNNITE 5V, VIRRRANRAJOITUSVASTUKSET
 OVAT NÄYTÖN PIIRILEVYLLÄ.

NOTE : (1)UNIT : mm

(2)NO SPECIFIED TOLERANCE IS ±0.5

(3)SCALE : NTS

VDD = +5V

VSS = GND = MIINUS

INTERFACE PIN CONNECTION

PIN NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SYMBOL	VSS	VDD	VO	R/S	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	K	A

CHARACTER GENERATOR ROM

INSTRUCTIONS

Instruction	Code										Description	Execution Time (max) (when fcp or fosc is 250 KHZ)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64 ms
Return Home	0	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B		Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*		Moves cursor and shifts display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*		Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	ACG							Sets CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40 μs	
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 μs	
Write Data to CG or DD RAM	1	0	Write Data									Writes data into DD RAM or CG RAM.	40 μs tADD=6 μs(Note2)
Read Data From CG or DD RAM	1	1	Read Data									Reads data from DD RAM or CG RAM.	40 μs tADD=6 μs(Note2)
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5x10 dots, F = 0: 5x7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM ACG : CG RAM address ADD : DD RAM address : Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. Example : When fcp or fosc is 270 KHZ : $40 \mu s \times \frac{250}{270} = 37 \mu s$	

*NO Effect

Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)

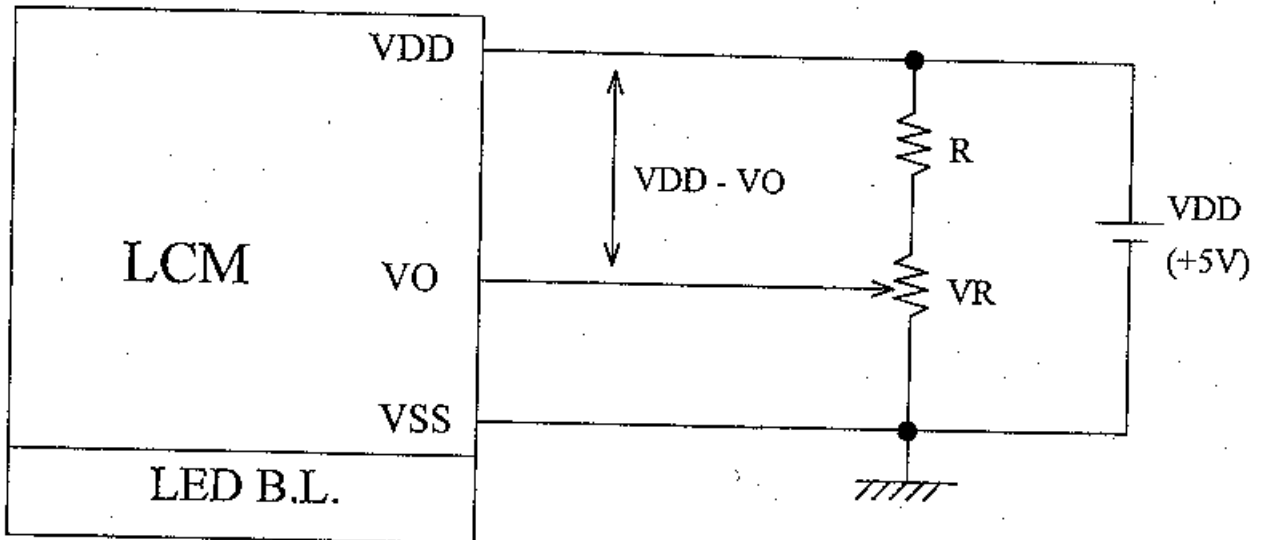
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)	+	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	1	CG RAM (2)	≡	!	1	A	a	2	a	3	a	4	U	Y	Y	Y	Y	Y	Y
	2	CG RAM (3)	7	"	2	R	b	r	e	e	5	'	e	e	e	e	e	e	e
	3	CG RAM (4)	L	#	3	C	c	s	a	a	6	'	7	7	7	7	7	7	7
	4	CG RAM (5)	7	\$	4	D	d	t	a	a	7	'	8	8	8	8	8	8	8
	5	CG RAM (6)	7	%	5	E	e	u	s	a	a	8	'	9	9	9	9	9	9
	6	CG RAM (7)	7	&	6	F	f	v	a	a	9	'	0	0	0	0	0	0	0
	7	CG RAM (8)	7	'	7	G	g	w	a	a	0	'	1	1	1	1	1	1	1
	8	CG RAM (1)	7	(8	H	h	x	a	a	1	'	2	2	2	2	2	2	2
	9	CG RAM (2)	7)	9	I	i	y	a	a	2	'	3	3	3	3	3	3	3
A	CG RAM (3)	7	*	A	J	j	z	a	a	3	'	4	4	4	4	4	4	4	
B	CG RAM (4)	7	+	B	K	k	0	a	a	4	'	5	5	5	5	5	5	5	
C	CG RAM (5)	7	,	C	L	l	1	a	a	5	'	6	6	6	6	6	6	6	
D	CG RAM (6)	7	-	D	M	m	2	a	a	6	'	7	7	7	7	7	7	7	
E	CG RAM (7)	7	.	E	N	n	3	a	a	7	'	8	8	8	8	8	8	8	
F	CG RAM (8)	7	/	F	O	o	4	a	a	8	'	9	9	9	9	9	9	9	

INTERFACE OF PIN CONNECTIONS

TYPE A VSS = GND, VDD = +5V

Pin No	1	2	3	4	5	6	7	
Symbol	VSS	VDD	VO	RS	R/W	E	DB0	
Pin No	8	9	10	11	12	13	14	
Symbol	DB1	DB2	DB3	DB4	DB5	DB6	DB7	

8. POWER SUPPLY FOR LCM AND LED BACKLIGHT.



VDD - VO : LCD DRIVING VOLTAGE

VR : 10KΩ ~ 20KΩ

RECOMMEND RESISTOR R : $VDD - VO \geq 1.5V$