



LM1141 Dolby B-C Type Noise Reduction Processor

General Description

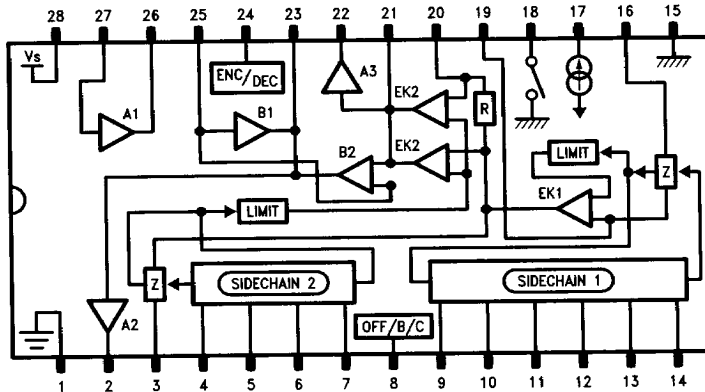
The LM1141 is a monolithic integrated circuit specifically designed to realise both Dolby B- and Dolby C-type noise reduction systems*. The circuit has a single input pin for Encode and Decode and includes all active components and switching internally to provide a single channel of a Dolby B- or Dolby C-type system. The low power consumption and compact package design make it ideal for use in automotive and portable Hi-Fi as well as quality cassette or tape sound systems.

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Features

- Very low supply current (11.5 mA typ.)
- Wide supply voltage range, 5–16V
- Alternative Dolby levels, 245 mV or 580 mV
- Provision for MPX filter
- Very high signal to noise ratio, 66 dB typ. for encode, C mode CCIR/ARM
- 50 mV encode input sensitivity (30 mV decode)
- D.C.-controlled mode switching
- Minimal switching transients
- 28 pin DIP or QUAD packages available

Block Diagram



TL/H/9242-1

Order Number LM1141N or LM1141V
See NS Package Number N28B or V28A

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_s 17V
 Input Voltage, Encode/Decode V_s
 Input Voltage, Switching $+V_s + 0.5V$
 $-V_s - 0.3V$

Soldering Information
 Dual-In-Line Package
 Soldering (10 seconds) 260°C

Plastic Chip Carrier Package
 Vapor Phase (60 seconds) 215°C
 Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range 0°C to +70°C
 Storage Temperature Range -65°C to +150°C

Package Dissipation
 @ $T_A = 25^\circ C$ (Note 1)
 { LM1141N = 2.5W
 { LM1141V = 1.7W

ESD rating is to be determined.

Electrical Characteristics

$V_s = 12V, T_A = 25^\circ C$ unless otherwise stated.

0 dB refers to Dolby level which is 245 mV measured at Encode Output 1 with NR OFF.

Note: Encode input sensitivity = 50 mV, Decode input sensitivity = 30 mV

Parameter	Conditions	Test Limit Note 2		Design Limit Note 3			Units
		Min	Max	Min	Typ	Max	
Supply Voltage	Min Signal Handling = 12 dB at Encode O/P 1	5	16				V
Supply Current	Encode, NR OFF, No signal		16		11.5		mA
Voltage Gain (Note 4)	Encode O/P 1, NR OFF	12.5	15.1		13.8		dB
	Encode O/P 2, NR OFF	19.8	22.8		21.3		dB
	Decode O/P 1, NR OFF	16.9	19.5		18.2		dB
	Decode O/P 2, NR OFF	24.2	27.2		25.7		dB
Input Resistance	Encode/Decode Input	35	80		55		kΩ
Signal To Noise Ratio (Note 5)	Encode O/P 1 or 2, $R_s = 5.6 k\Omega$ C Mode			62	66		dB
	C.C.I.R./A.R.M B Mode			70	76		dB
	Decode O/P 1 or 2, $R_s = 5.6 k\Omega$, NR OFF			78	84		dB
	Enc O/P 1, Dec O/P 1, 1 kHz $V_s = 5V$, NR OFF, 1% T.H.D.	12			13		dB
	Enc O/P 2, Dec O/P 2, 1 kHz $V_s = 9V$, NR OFF, 1% T.H.D.	12			13		dB
Distortion (T.H.D.)	Encode O/P2, C Mode 0 dB, 1 kHz				0.05	0.15	%
	Decode O/P2, C Mode 0 dB, 1 kHz				0.04	0.15	%
Encode Characteristics	B Mode, 5 kHz, 0 dB			-1.2	0.3	1.8	dB
	B Mode, 1 kHz, -20 dB			2.7	4.2	5.7	dB
	B Mode, 5 kHz, -30 dB	6.7	9.7		8.2		dB
	B Mode, 1 kHz, -40 dB	4.7	7.7		6.2		dB
	C Mode, 10 kHz, -0 dB			-5.5	-3.5	-1.5	dB
	C Mode, 1 kHz, -20 dB			3.9	5.9	7.9	dB
	C Mode, 5 kHz, -30 dB	6.4	10.4		8.4		dB
	C Mode, 1 kHz, -40 dB	14.2	18.2		16.2		dB
Control Voltage	Encode Mode		0.8	0			V
	Decode Mode	2.0				V_s	V
	B Mode		0.8	0			V
	Off Mode	2.0	3.2		Open		V
	C Mode	4.6				V_s	V

Note 1: Above $T_A = 25^\circ C$, derate with $\theta_{ja} = 50^\circ C/W$ (LM1141N)
 $75^\circ C/W$ (LM1141V)
 $T_j \text{ max} = 150^\circ C$

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: The resistors at the input and output of the MPX Filter are required to match the characteristic impedance of the filter block. The values shown correspond to the most commonly used filter for this application. Values should be checked for each individual application. If no filter is used, a 3.1 dB attenuation pad should be retained for correct operation of the processor.

Note 5: Gaussian noise, monitored over a period of 50 ms with a CCIR filter and an average-responding meter.

Pin Function Description

- PIN 1. Negative supply voltage, $-V_s$.
- PIN 2. High level decode (playback) output, (580 mV).
- PIN 3. Connection to the variable impedance of sidechain 2. A capacitor is connected between this pin and signal ground to give a variable high pass filter characteristic, controlled by the side-chain.
- PIN 4. A capacitor is connected between this pin and signal ground to provide pre-emphasis at amplifier D in sidechain 2.
- PIN 5. A capacitor is connected between this pin and signal ground which decouples the feedback components of amplifier D of sidechain 2, and reduces system offsets.
- PIN 6/7. Sidechain 2 transient response circuit.
- PIN 8. Selects OFF, B or C mode depending on the d.c. voltage applied.
- PIN 9/10. These pins are connected internally to low saturation switching transistors and externally to the transient response circuit of sidechain 1 in such a way that in C-mode the capacitor values are reduced.
- PIN 11/12. Sidechain 1 transient response circuit.
- PIN 13. A capacitor is connected between this pin and signal ground to provide pre-emphasis at amplifier D in sidechain 1.
- PIN 14. A capacitor is connected between this pin and signal ground which decouples the feedback components of amplifier D of sidechain 1, and reduces the system offsets.
- PIN 15. Signal ground, set internally to approximately half the supply voltage.
- PIN 16. Connection to the variable impedance of sidechain 1. A capacitor is connected between this pin and signal ground to give a variable high pass filter characteristic, controlled by the side-chain.
- PIN 17. A resistor is connected between this pin and $-V_s$. This sets up an accurate current required for correct maximum impedance filter characteristics.
- PIN 18. This pin is connected internally to a low saturation switching transistor and is energised to switch on the Spectral Skewing circuit in C-mode.
- PIN 19. The Spectral Skewing circuit is connected to this pin.
- PIN 20. The Anti-Saturation circuit is connected to this pin.
- PIN 21. Low level encode (record) output (245 mV).
- PIN 22. High level encode (record) output (580 mV).
- PIN 23. Low level decode (playback) output (245 mV).
- PIN 24. Selects encode or decode mode depending on the d.c. voltage applied.
- PIN 25. MPX filter output.
- PIN 26. MPX filter input.
- PIN 27. Signal input (encode and decode).
- PIN 28. Positive supply voltage, $+V_s$.

Typical Applications

Selection of encode/decode and off/B/C is achieved by applying the required d.c. voltage to the appropriate control pin. *Figures 1 and 2* show the relationship between the applied voltage and the mode selected.

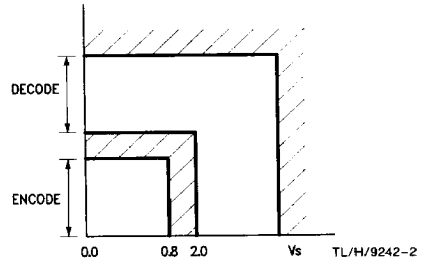
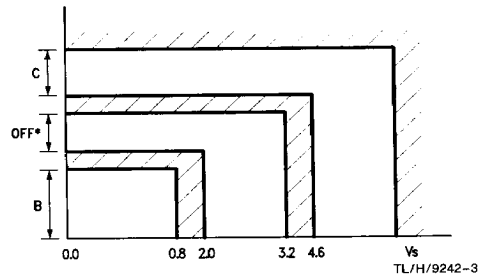


FIGURE 1. Pin 24 control voltage (V).



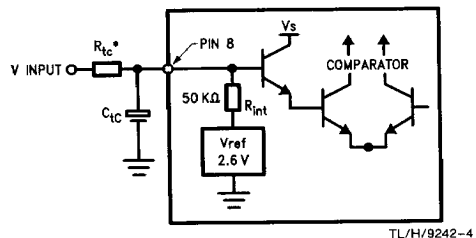
* Pin 8 open also gives Off mode.

FIGURE 2. Pin 8 control voltage (V).

Although audible switching pops have been reduced to a minimum, further improvement may be achieved by including an R-C time constant on the switching pins.

The values chosen for the R-C circuit connected to the OFF-B-C switching pin (8) are important in order that the switching circuitry functions correctly.

The internal configuration at pin 8 includes connection to a darlington input stage comparator and a 2.6V voltage reference via a resistor of value 50 k Ω , (see *Figure 3*) which allows selection of OFF mode when pin 8 is open-circuited, (See specification).



* R_{tc} max = 5 k Ω for 5V operation.

FIGURE 3

The capacitor C_{tc} affects the switching time when selecting OFF-mode (pin 8 open) from C mode. The discharge path is now via the 50 k Ω resistor to V_{ref} , hence the switching time

Typical Applications (Continued)

is a function of $R_{int}C$. The Encode/Decode switching pin (24) is unaffected by the connection of a similar R-C network.

Connection of Supply Voltage

The device may be operated in either single ended or dual supply modes, since the internally generated bias voltage (pin 15) is approximately half the supply voltage.

For single supply applications a large electrolytic capacitor ($200 \mu\text{F}$) should be connected between pin 15 and $-V_s$.

For dual supply operation this capacitor is not required and pin 15 can be connected to 0V directly.

Sidechain Variable High Pass Filters

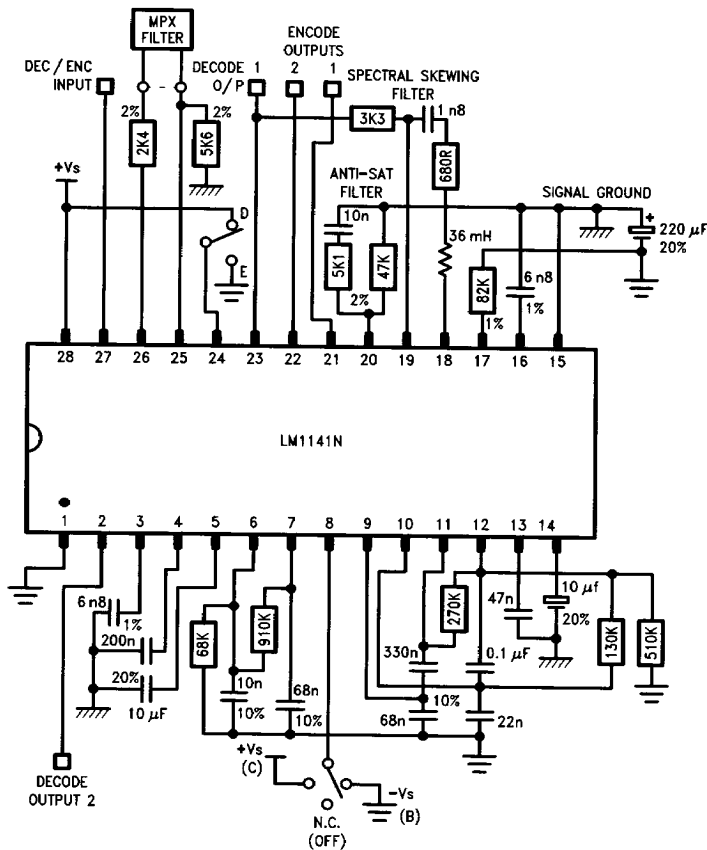
In encode mode the boost characteristics are controlled by the variable impedances of the sidechains in conjunction with external capacitors and a resistor forming a variable high pass filter.

The capacitors and the resistor (on pin 17 and common to both sidechains) must be accurate and of high stability (a tolerance of 1% is recommended).

Typical Connection Diagram for 5V to 9V Supply

(All external components 5% unless otherwise stated.)

*MPX Filter, See note 4 in General Notes.



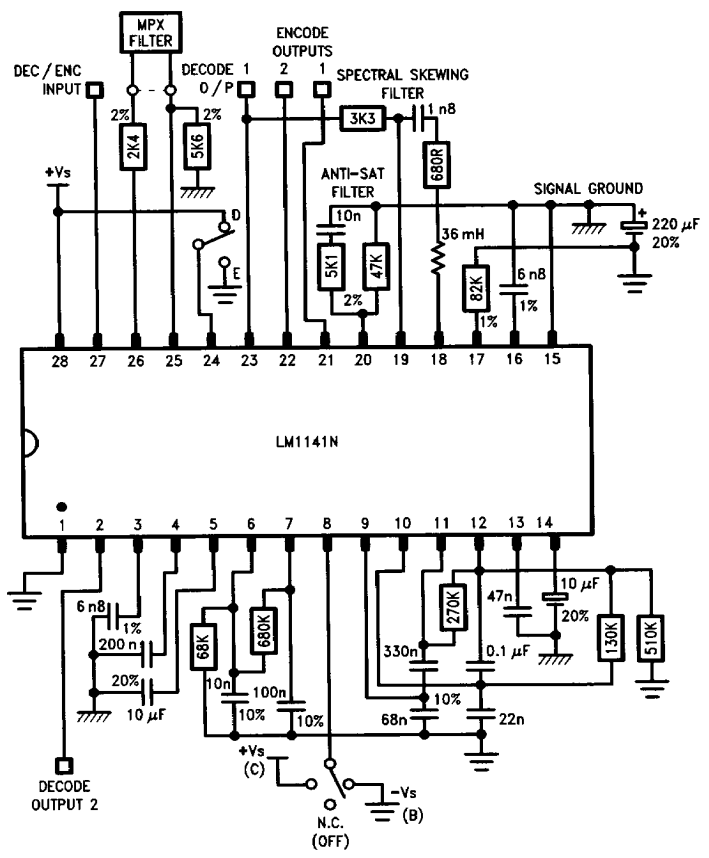
Device also available in 28 pin quad chip carrier package.

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Typical Connection Diagram for 8V to 16V Supply

(All external components 5% unless otherwise stated.)

*MPX Filter, See note 4 in General Notes.



Device also available in 28 pin quad chip carrier package.

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