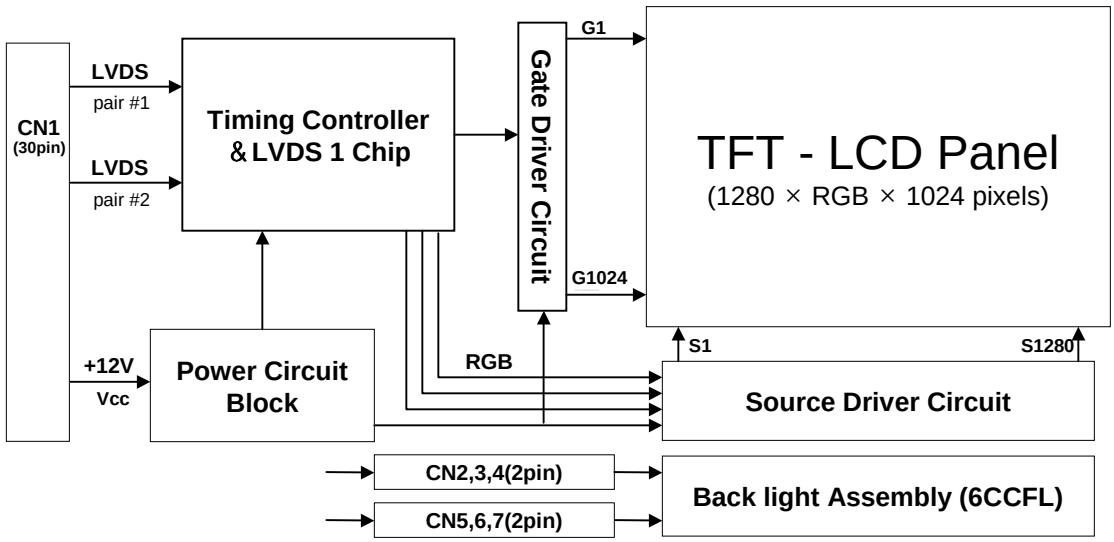
1. General Description

The LM181E06-A4M1 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element.
It is a transmissive type display operating in the normally black mode. This TFT-LCD has a 18.1 inch diagonally measured active display area with SXGA resolution(1024 vertical by 1280 horizontal pixel array).
Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes.
Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,777,216 colors.
The LM181E06-A4M1 has been designed to apply the interface method that enables low power, high speed,low EMI. FPD Link must be used as a LVDS(Low Voltage Differential Signaling) chip.
The LM181E06-A4M1 is intended to support applications where thin thickness, wide viewing angle, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LM181E06-A4M1 characteristics provide an excellent flat panel display for office automation products such as monitors.



General Features

Active screen size	18.1 inches (459.74mm) diagonal
Outline Dimension	389.0(H) x 317.2(V) x 27.0(D) mm(Typ.)
Pixel Pitch	0.2805 mm x 0.2805 mm
Pixel Format	1280 horizontal By 1024 vertical Pixels RGB stripe arrangement
Color depth	8-bits, 16,777,216 colors
Luminance, white	250 cd/m^2(Typ. Center 1 point)
Power Consumption	Total 29.52 Watt(Typ.), (4.32Watt @Vcc, 25.2 Watt @250cd/㎡ [Lamp=7mA])
Weight	3100g (Typ.)
Display operating mode	Transmissive mode, normally black
Surface treatments	Hard coating (3H), Anti-glare treatment of the front polarizer

2. Electrical Specifications

The LM181E06-A4M1 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

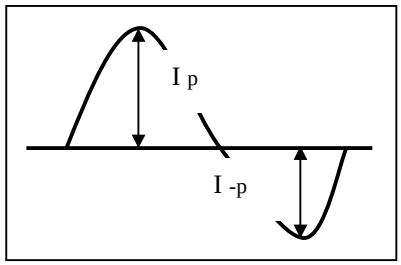
Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
MODULE :						
Power Supply Input Voltage	V_{CC}	11.4	12.0	12.6	V(DC)	
Power Supply Input Current	I_{CC}	–	0.36	0.45	A	1
Differential Impedance	Zm	90	100	110	Ohm	2
Power Consumption	P_C	–	4.32	5.4	Watts	1
Rush Current	I_{RUSH}	–	--	4	A	3
LAMP :						
Operating Voltage	V_{BL}	550(8.0)	600(7.0)	725(3.0)	V_{RMS}	4
Operating Current	I_{BL}	3.0	7.0	8.0	mA_{RMS}	
Established Starting Voltage	V_S					5
at 25℃		–	–	–	1,000	V_{RMS}
at 0℃		–	–	–	1,300	V_{RMS}
Operating Frequency	F_{BL}	45	55	65	KHz	6
Discharge Stabilization Time	T_S	–	–	3	Minutes	7
Power Consumption(6CCFL's)	P_{BL}	–	25.2	27.7	Watts	8
Life Time	–	40,000	–	–	Hrs	9

Note : **The design of the inverter must have specifications for the lamp in LCD Assembly.**
The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter(no lighting, flicker, etc) never occurs. When you confirm it, the LCD Assembly should be operated in the same condition as installed in you instrument.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp.

It shall help increase the lamp lifetime and reduce its leakage current.
a. The asymmetry rate of the inverter waveform should be 10% below;
b. The distortion rate of the waveform should be within $\sqrt{2}$ ±10%;
c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

1. The specified current and power consumption are under the V_{CC}=12.0V, 25°C, f_V=60Hz condition, Typical supply current is measured at the condition of 8 X 6 chess pattern(white & black)
2. This impedance value is for impedance matching between LVDS T_X and the mating connector of the LCD.
3. The duration of rush current is about 1ms.
4. The variance of the voltage is ± 10%.
5. The voltage above V_{BS} should be applied to the lamps for more than 1 second for start-up. Otherwise, the lamps may not be turned on.
6. The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave.
   Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
7. Let's define the brightness of the lamp after being lighted for 5 minutes as 100%.
   T_S is the time required for the brightness of the center of the lamp to be not less than 95%.
   The used lamp current is the lamp typical current.
8. The lamp power consumption shown above does not include loss of external inverter.
   The used lamp current is the lamp typical current.
9. The life time is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2°C.

Typical life time shall be defined that remained rate maintains over 50% of total amount at the life test.

◈ Do not attach a conductive tape to lamp connecting wire.
If the lamp wire attach to a conducting tape, TFT-LCD Module has a low luminance and the inverter has abnormal action. Because leakage current is occurred between lamp wire and conducting tape.

3. Interface Connections

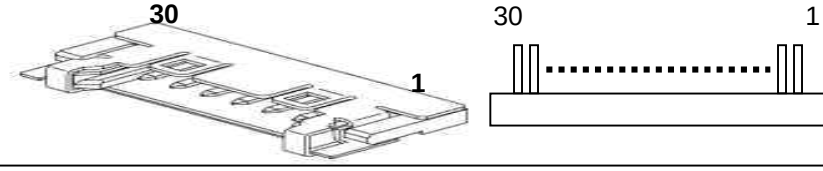
Interface chip must be used LVDS, part No. DS90CF383MTD(Transmitter) made by Nation Semiconductor. Or used the compatible interface chips(TI:SN75LVDS83, Thine).
This LCD employs seven interface connections, a 30-pin connector is used for the module electronics interface. Six 2-pin connectors are used for the integral back-light system.
The electronics interface connector is a model 55177-3091 manufactured by MOLEX. The pin configuration for the connector is shown in the table 3.

Table 3. MODULE CONNECTOR PIN CONFIGURATION(LVDS)

Pin	Symbol	Description	
1	Vcc	Supply voltage for LCD module	
2	Vcc	Supply voltage for LCD module	
3	Vcc	Supply voltage for LCD module	
4	Vcc	Supply voltage for LCD module	
5	GND	Ground	
6	GND	Ground	
7	SR0M	Minus signal of even channel 0 (LVDS)	Second data
8	SR0P	Plus signal of even channel 0 (LVDS)	
9	SR1M	Minus signal of even channel 1 (LVDS)	
10	SR1P	Plus signal of even channel 1 (LVDS)	
11	SR2M	Minus signal of even channel 2 (LVDS)	
12	SR2P	Plus signal of even channel 2 (LVDS)	
13	SCLKINM	Minus signal of even clock channel (LVDS)	
14	SCLKINP	Plus signal of even clock channel (LVDS)	
15	SR3M	Minus signal of even channel 3 (LVDS)	
16	SR3P	Plus signal of even channel 3 (LVDS)	
17	GND	Ground	
18	GND	Ground	
19	FR0M	Minus signal of odd channel 0 (LVDS)	First data
20	FR0P	Plus signal of odd channel 0 (LVDS)	
21	FR1M	Minus signal of odd channel 1 (LVDS)	
22	FR1P	Plus signal of odd channel 1 (LVDS)	
23	FR2M	Minus signal of odd channel 2 (LVDS)	
24	FR2P	Plus signal of odd channel 2 (LVDS)	
25	FCLKINM	Minus signal of odd clock channel (LVDS)	
26	FCLKINP	Plus signal of odd clock channel (LVDS)	
27	FR3M	Minus signal of odd channel 3 (LVDS)	
28	FR3P	Plus signal of odd channel 3 (LVDS)	
29	GND	Ground	
30	GND	Ground	

Connector pin arrangement

P/N, Maker :
55177-3091, Molex



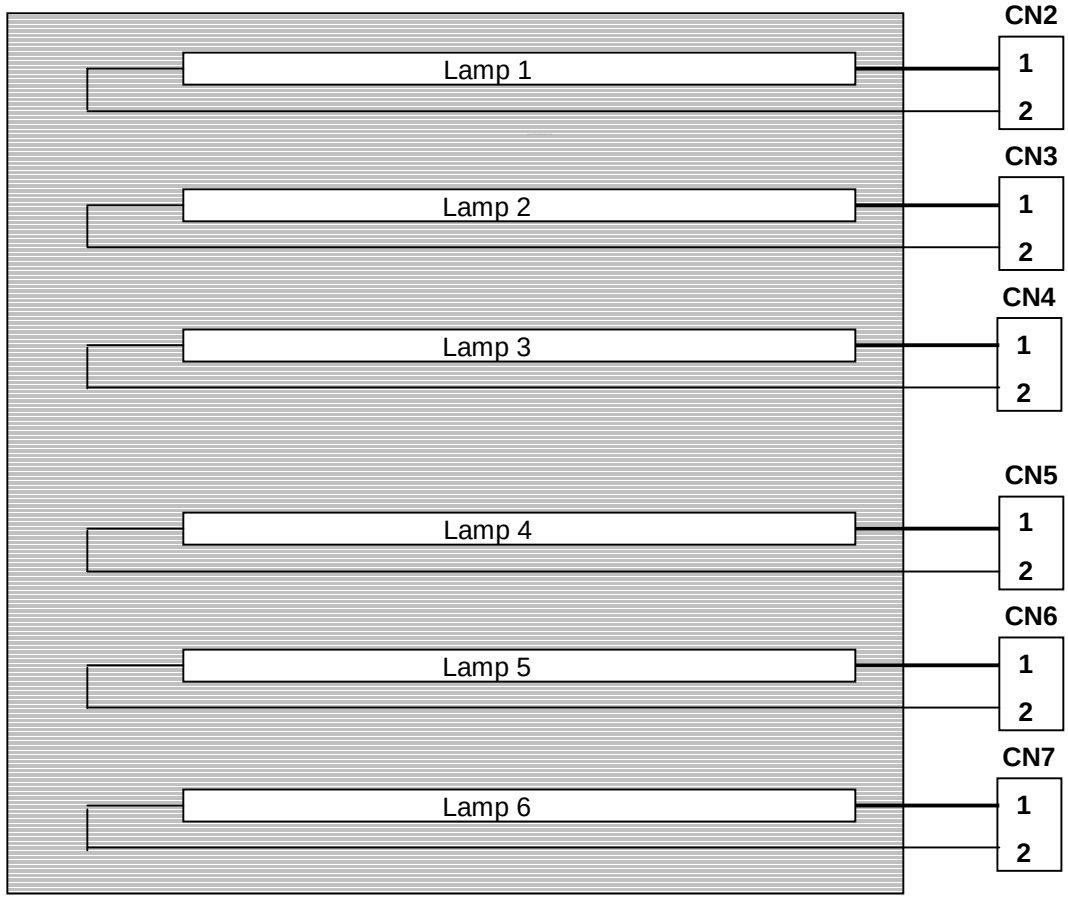
The backlight interface connector is a model BHSR-02VS-1, manufactured by JST. The mating connector part number is SM02B-BHS-1 or equivalent.
The pin configuration for the connector is shown in the table 4.

Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION

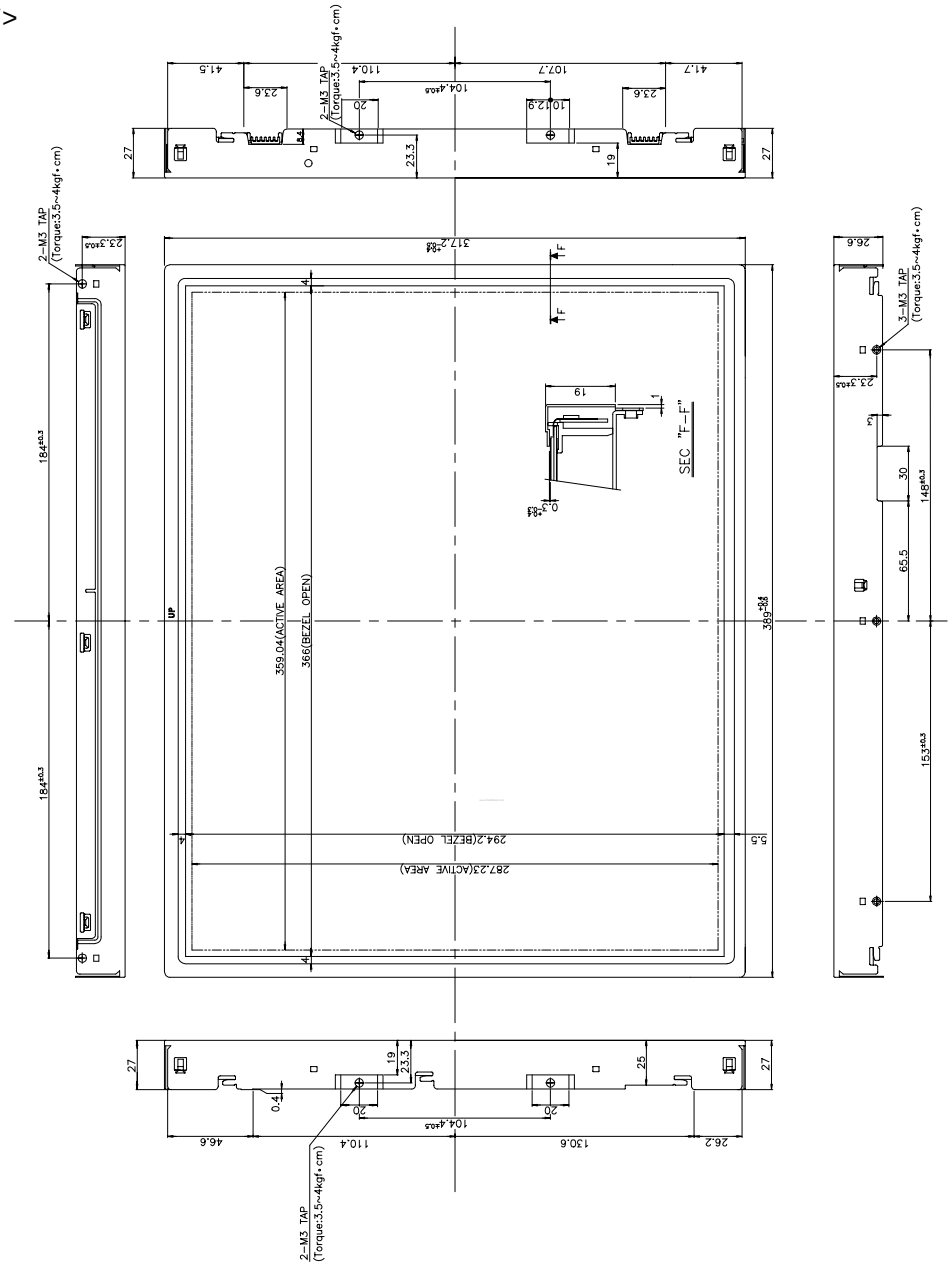
No.	Pin	Symbol	Description	Notes
CN2,3,4,5,6,7	1	HV	Power supply for lamp (High voltage side)	1
	2	LV	Power supply for lamp (Low voltage side)	2

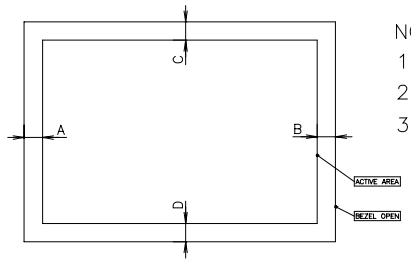
Note : 1. The high voltage side terminal is colored Pink & Blue & Gray.
2. The low voltage side terminal is all White

The below is block diagram for pin configuration of lamp connector.



<FRONT VIEW>



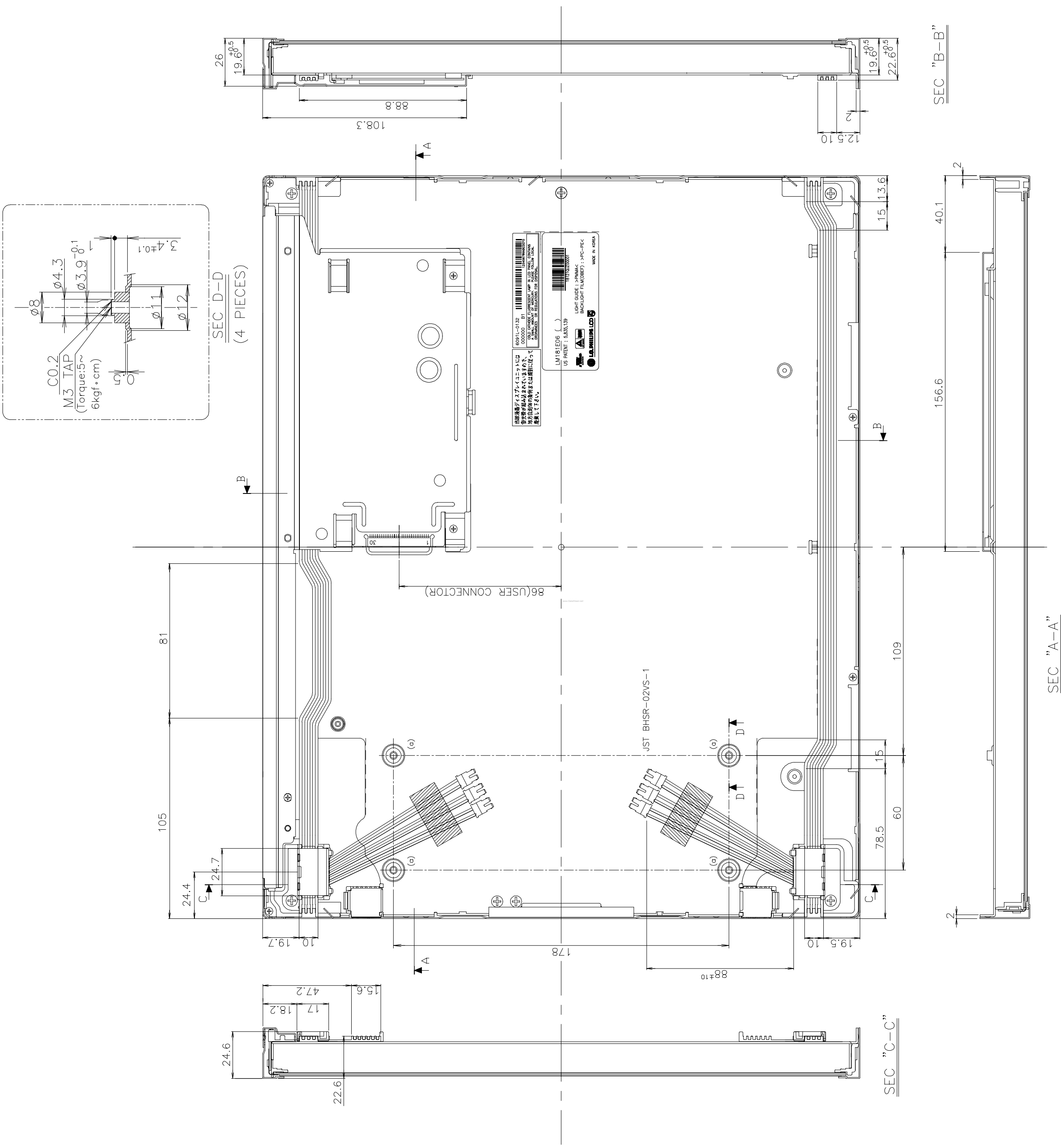


NOTE

1. UNSPECIFIED TOLERANCE IS ±0.5 mm
2. GAP BETWEEN TOP CASE AND GLASS IS $0.2^{+0.5}_{-0.2}$
3. TILT AND A PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA ARE AS FOLLOW.
   1) X-DIRECTION : | A-B | ≤ 1mm
   1) Y-DIRECTION : | C-D | ≤ 1mm

Product Specification

<REAR VIEW>



4. PRECAUTIONS

The LCD Products listed on this documents are not suitable for use of Military, Industry, Medical etc. System
If customers intend to use these LCD products for above application, Please contact sales people In advance.