



深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

# LM192160BCW

## LCD Module User Manual

Prepared by:  <b>Lin</b>  Date: 2011-09-21	Checked by:    Date:	Approved by:    Date:
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Rev.	Descriptions	Release Date
0.1	Preliminary release	2010-7-11
0.2	Refine /WR, /RD description	2011-09-21

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# 1. Basic Specifications

## 1.1 Display Specifications

- 1) LCD Display Mode : FSTN, Positive, Transflective
- 2) Display Color : Display Data = "1" : Dark Gray (\*1)  
: Display Data = "0" : Light Gray (\*2)
- 3) Viewing Angle : 6H
- 4) Driving Method : 1/160 duty, 1/12 bias
- 5) Back Light : White LED backlight

Note:

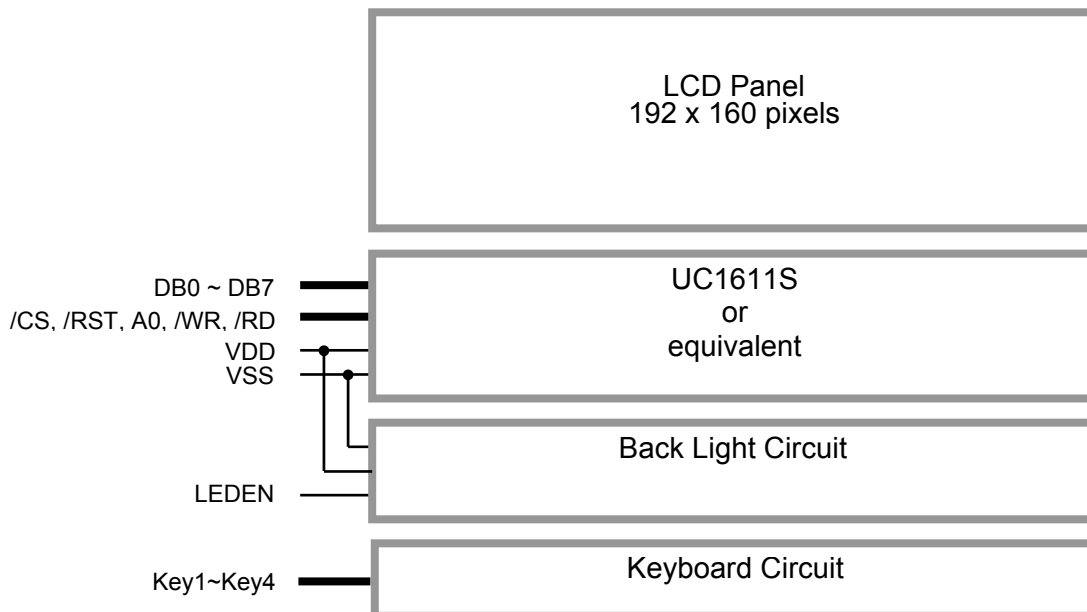
\*1. Color tone may slightly change by Temperature and Driving Condition.

\*2. The Color is defined as the inactive / background color

## 1.2 Mechanical Specifications

- 1) Outline Dimension : 85.4 x 84.6 x 11.5 MAX  
(See attached Outline Drawing for details)

## 1.3 Block Diagram



## 1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions		
			8-bit parallel 8080 mode	Serial mode	I <sup>2</sup> C mode
1	VSS	Power	0V Supply, Ground (0V)		
2	A0	Input	Register Select A0=H: data on DB0 to DB7 is display data A0=L: data on DB0 to DB7 is control data	Not use, connect to VSS	
3	/WR	Input	/WR=H, /RD=L; Data or Status read form the LCD module /WR=L→H, /RD=H; Data or Instruction latch into the LCD module	Not use, connect to VSS	
4	/RD	Input		Not use, connect to VSS	
5	/CS	Input	Chip Select /CS=L : Data IO is enabled	Not use, connect to VSS	
6	/RST	Input	Reset: /RST=L: Initialization is executed /RST=H: Normal		
7	VDD	Power	Positive Power Supply		
8	DB0(SCL)	I/O	8-bit Data bus; Three state I/O terminal for display data or instruction data when /CS =H, DB0~DB7=High Impedance	Serial clock input(DB0)	
:	:			Not use, connect to VDD or VSS	
11	DB3(SDA)			Serial data input(DB3)	
:	:			Not use, connect to VDD or VSS	
15	DB7				
16	NC	-	-		
17	LEDEN	Input	Backlight Control Input;		
18	NC	-	-		
19	NC	-	-		
20	NC	-	-		
21	Key4	-	Keyboard Circuit		
22	Key3	-			
23	Key2	-			
24	Key1	-			

### Interface setting:

Setting	8080 mode(Default)	SPI mode	I <sup>2</sup> C mode *
JP1	OPEN	OPEN	CLOSE
JP2	CLOSE	CLOSE	OPEN
JP3	OPEN	CLOSE	CLOSE
JP4	CLOSE	OPEN	OPEN
JP5	OPEN	OPEN	CLOSE
JP6	CLOSE	CLOSE	OPEN
JP7	OPEN	CLOSE	CLOSE
JP8	OPEN	CLOSE	CLOSE
JP9	OPEN	OPEN	CLOSE
JP10	OPEN	OPEN	CLOSE

Note:

\*1. In I<sup>2</sup>C Interface setting, R2 and R3 should be setup (10kΩ).

## 2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	$V_{DD}$	-0.3	+4.0	V	$V_{SS} = 0V$
Input Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	V	$V_{SS} = 0V$
Operating Temperature	$T_{OP}$	-20	+70	°C	No Condensation
Storage Temperature	$T_{ST}$	-30	+80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## 3. Electrical Characteristics

### 3.1 DC Characteristics

$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	$V_{DD}$	3.0	3.3	3.6	V	VDD
Input High Voltage	$V_{IH}$	$0.8 \times V_{DD}$	-	$V_{DD}$	V	/RST, /CS, RS, /WR, /RD, DB0~DB7
Input Low Voltage	$V_{IL}$	0	-	$0.2 \times V_{DD}$	V	
Operating Current	$I_{DD}$	-	1.5	7.0	mA	VDD

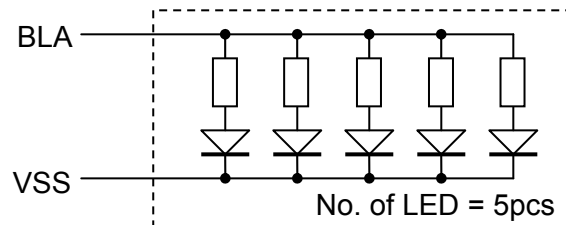
### 3.2 LED Backlight Circuit Characteristics

$V_{SS}=0V, I_{f_{BLA}}=100mA, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	$V_{f_{BLA}}$	-	3.3	-	V	BLA
Forward Current	$I_{f_{BLA}}$	-	100	110	mA	BLA

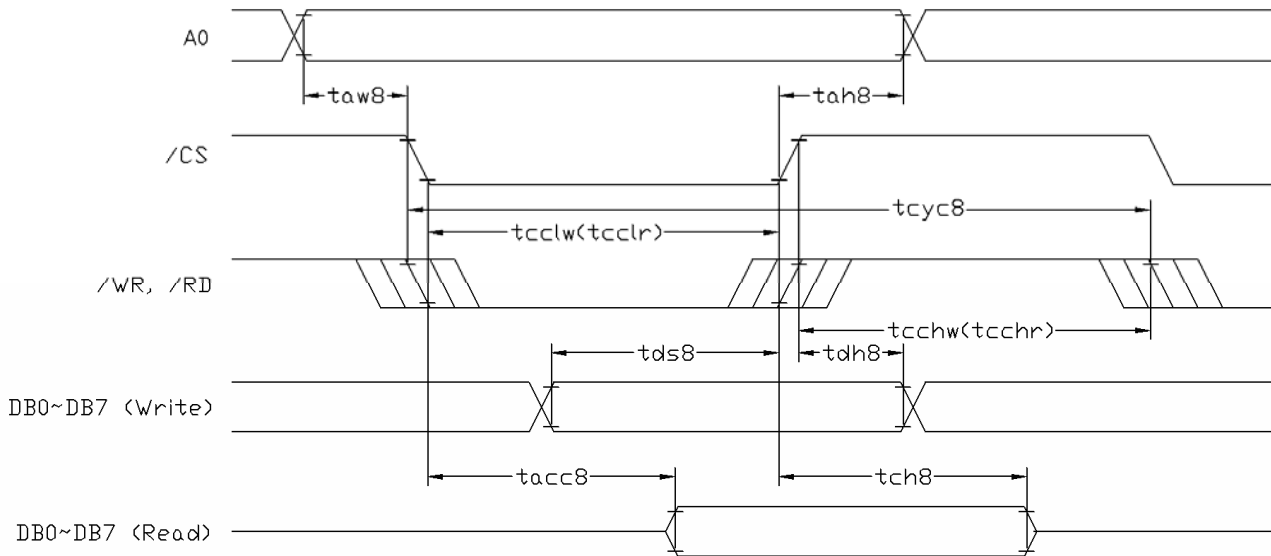
Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



**3.3 AC Characteristics**

**3.3.1 8080 Mode System Bus Timing**



$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

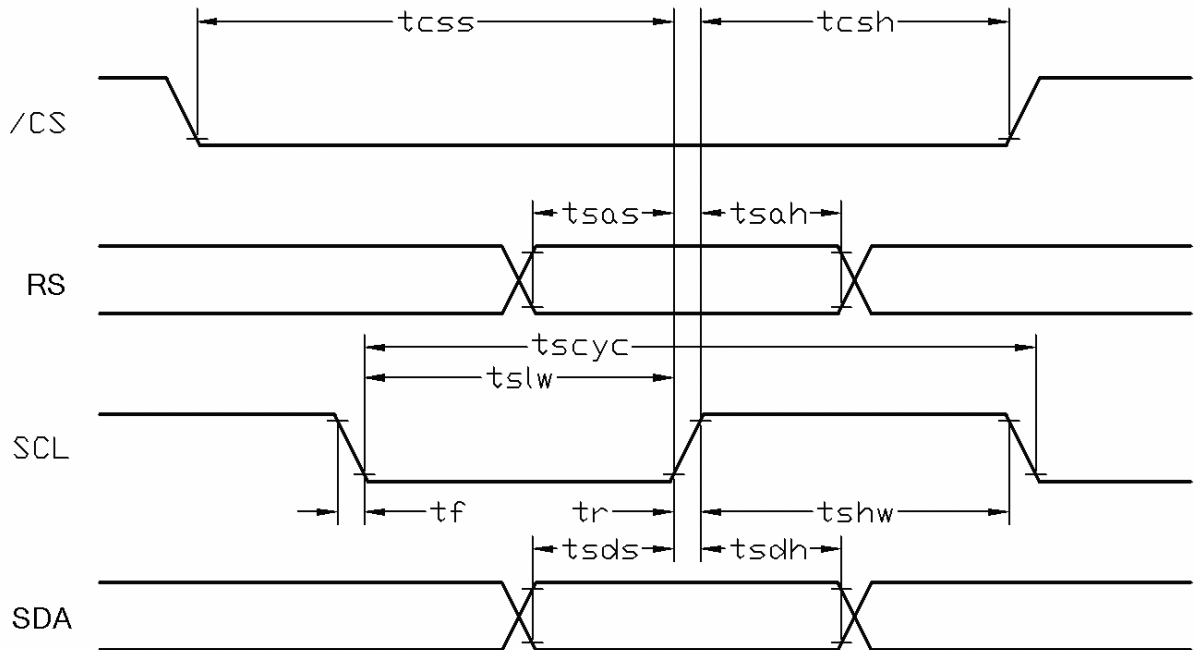
Item	Symbol	MIN.	TYP.	MAX.	Unit
System cycle time	tcyc8	150	-	-	ns
Address setup time (A0)	taw8	0	-	-	ns
Address hold time (A0)	tah8	0	-	-	ns
Control LOW pulse width (/WR)	tcclw	95	-	-	ns
Control LOW pulse width (/RD)	tcclr	95	-	-	ns
Control HIGH pulse width (/WR)	tcchw	95	-	-	ns
Control HIGH pulse width (/RD)	tcchr	95	-	-	ns
Data setup time	tds8	40	-	-	ns
Data hold time	tdh8	0	-	-	ns
/RD access time (*2)	tacc8	-	-	57	ns
Output disable time (*2)	tch8	-	-	38	ns

Note:

\*1. Input signal rise/fall time should be less than 12ns

\*2. CL=100pF

**3.3.2 Serial Mode Interface**



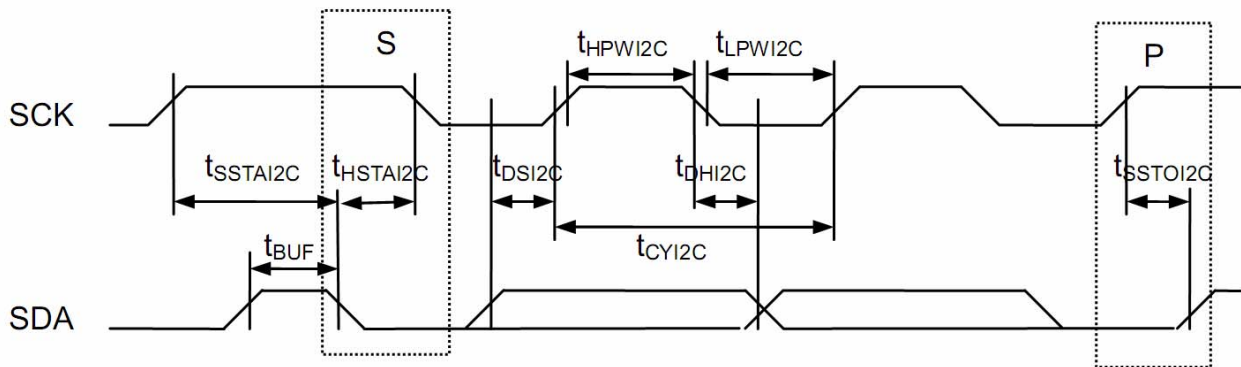
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Serial Clock Period	tscyc	51	-	-	ns
Address setup time (A0)	tsas	10	-	-	ns
Address hold time (A0)	tsah	10	-	-	ns
SCL "H" pulse width	tshw	26	-	-	ns
SCL "L" pulse width	tslw	26	-	-	ns
Data setup time	tsds	21	-	-	ns
Data hold time	tsdh	10	-	-	ns
CS-SCL time	tcss	10	-	-	ns
CS-SCL time	tcsh	10	-	-	ns

Note:

\*1. Input signal rise/fall time should be less than 12ns

3.3.3 I<sup>2</sup>C mode Interface



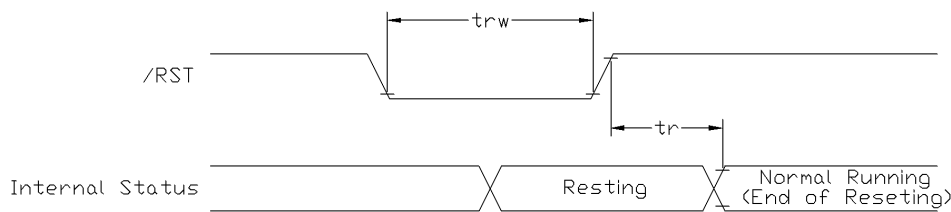
V<sub>SS</sub>=0V, V<sub>DD</sub>=3.3V, T<sub>OP</sub>=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
SCK cycle time	t <sub>CY12C</sub>	580	-	-	ns
Low pulse width	t <sub>LPWI2C</sub>	290	-	-	ns
High pulse width	t <sub>HPWI2C</sub>	290	-	-	ns
Data setup time	t <sub>DS12C</sub>	33	-	-	ns
Data hold time	t <sub>DH12C</sub>	11	-	-	ns
START Setup time	t <sub>SSTAI2C</sub>	28	-	-	ns
START Hold time	t <sub>HSTAI2C</sub>	50	-	-	ns
STOP setup time	t <sub>SSTOI2C</sub>	28	-	-	ns
Bus Free time	t <sub>BUF</sub>	165	-	-	ns

Note:

\*1. Input signal rise/fall time should be less than 12ns

3.4 Reset Timing



V<sub>SS</sub>=0V, V<sub>DD</sub>=3.3V, T<sub>OP</sub>=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset time	tr	-	-	15	ms
Reset LOW pulse width	trw	5	-	-	μs

Note:

\*1. Input signal rise/fall time should be less than 12ns

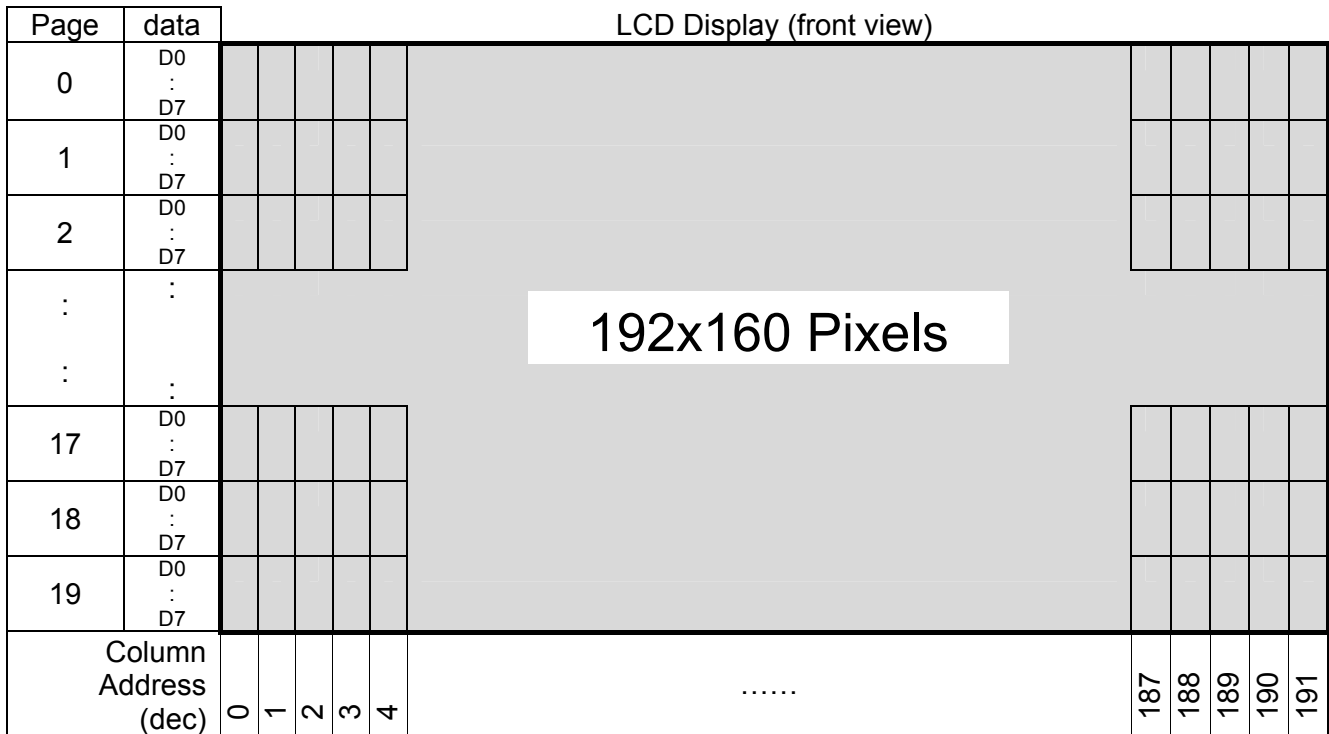


## 4. Function Specifications

### 4.1 Resetting the LCD module

The LCD module should be initialized by using /RST terminal.  
 While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level. After the power supply stabilized, release the reset terminal (/RST=HIGH)

### 4.2 Display Memory Map



Pixel mapping (Top View)

Note:

- \*1. Based on the top view of the LCD module,
- \*2. The above is memory map based on:  
 On/Off mode setting, DC[5:3]=100 (1bpp), the Page value range: 0~19  
 LC[0]=MSF=0  
 LC[1]=MX=1  
 LC[2]=MY=0  
 SL=0
- \*3. For 4,8 and 16 Gray-shade operation please refer to UC1611 datasheet.

**4.3 Commands**

**4.3.1 Register Table**

Name	Bits	Default	Description
SL	8	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – FL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed lines. The first (FLx2) lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CA	8	00H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	7	00H	Display Data RAM Page Address (Used in Host for Display Data RAM access) When DC[5:3] = 100b, PA[6:5] : used to select Write Pattern 0~3. PA[4:0] : set SRAM page address
BR	2	2H	Bias Ratio. The ratio between $V_{LCD}$ and $V_{BIAS}$ . 00b: 5                      01b: 10 10b: 11                     11b: 12
TC	2	0H	Temperature Compensation (per °C). 00b: -0.05%              01b: -0.10% 10b: -0.15%              11b: 0.00%
PM	8	EAH	Electronic Potentiometer to fine tune $V_{BIAS}$ and $V_{LCD}$
PMO	6	00H	PM offset. the effective PM value, $PMV = PM - PMO[4:0]$ when $PMO[5]=1$ the effective PM value, $PMV = PM + PMO[4:0]$ when $PMO[5]=0$
PC	4	FH	Pump Control. PC[1:0]: Panel Loading 00b: LCD: $\leq 33nF$ <b>11b: <math>33nF \leq LCD \leq 55nF</math></b> PC[3:2]: Pump Control 00b: External $V_{LCD}$ <b>11b: Internal <math>V_{LCD}</math> (11x charge pump)</b> (Setting to 01 or 10 will be invalid and default value will be used instead.)
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default <b>1:ON</b> ) AC[1]: Auto-Increment order 0: <b>Column (CA) first</b> 1: Page (PA) first AC[2]: PID: PA (page address) auto increment direction ( <b>0:+1</b> , 1:-1) AC[3]: Window Program Mode 0 : <b>Inside Mode</b> : Write to SRAM within the window defined by (WPC0,WPP0), (WPC1,WPP1) 1 : <b>Outside Mode</b> : Write to SRAM but skip the window defined by (WPC0,WPP0), (WPC1,WPP1)

**Register Table (continue)**

Name	Bits	Default	Description																									
DC	8	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default <b>0:OFF</b> ) DC[1]: APO: All Pixels ON (Default <b>0:OFF</b> ) DC[2]: Display ON/OFF (Default <b>0:OFF</b> ) DC[4:3]: Gray-shade Modulation mode. 00 : On/Off mode                      01: 8-shade Mode 10 : 4-shade Mode <b>11: 16-shade mode</b> DC[5]: Input Type of On/Off Mode (enable only when DC[4:3]=00b) <b>0: 4-bit per 1-pixel</b> 1: 1-bit per 1-pixel DC[7:6]: Display Pattern Selection (enable only when DC[5:3]=100b) <b>00: Pattern0</b> 01: Pattern1 10: Pattern2                              11: Pattern3																									
LC	10	020H	LCD Control: LC[0]: MSF: MSB First mapping Option (Default: <b>0:OFF</b> ) LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: <b>0:OFF</b> ) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: <b>0:OFF</b> ) LC[3]: Enable FL lines in partial display mode.(Default: <b>0:OFF</b> ) LC[5:4]: Line Rate (= Frame-Rate x Mux-Rate) <table border="1" style="margin-left: 40px;"> <thead> <tr> <th></th> <th>LC[5:4]=00b</th> <th>01b</th> <th><b>10b</b></th> <th>11b</th> </tr> </thead> <tbody> <tr> <td><b>16-shade</b></td> <td>20.0 Klps</td> <td>24.0</td> <td><b>28.0</b></td> <td>32.0</td> </tr> <tr> <td>8-shade</td> <td>14.1</td> <td>16.9</td> <td><b>19.7</b></td> <td>22.5</td> </tr> <tr> <td>4-shade</td> <td>13.3</td> <td>16.0</td> <td><b>18.7</b></td> <td>21.4</td> </tr> <tr> <td>On/Off mode</td> <td>5.9</td> <td>7.1</td> <td><b>8.2</b></td> <td>9.4</td> </tr> </tbody> </table> <p style="text-align: right;">( Klps: Kilo-Line-per-second )</p> LC[7:6] : Reserved (Default : <b>00b</b> ) LC[9:8] : Partial Display Control <b>0xb: Disable</b> Mux-rate = CEN+1 (DST and DEN are not used.) 11b: Enabled      Mux-rate = DEN-DST+1+LC[3]xFLx2		LC[5:4]=00b	01b	<b>10b</b>	11b	<b>16-shade</b>	20.0 Klps	24.0	<b>28.0</b>	32.0	8-shade	14.1	16.9	<b>19.7</b>	22.5	4-shade	13.3	16.0	<b>18.7</b>	21.4	On/Off mode	5.9	7.1	<b>8.2</b>	9.4
	LC[5:4]=00b	01b	<b>10b</b>	11b																								
<b>16-shade</b>	20.0 Klps	24.0	<b>28.0</b>	32.0																								
8-shade	14.1	16.9	<b>19.7</b>	22.5																								
4-shade	13.3	16.0	<b>18.7</b>	21.4																								
On/Off mode	5.9	7.1	<b>8.2</b>	9.4																								
NIV	7	00H	N-Line Inversion NIV[5:0] : <b>000000b : Disable N-line Inversion</b> NIV[6] : <b>0b: no-XOR</b> 1b: XOR																									
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning ENd (the last COM with full line cycle, 0-based index) Display STart (the first COM with active scan pulse, 0-based index) Display EDd (the last COM with active scan pulse, 0-based index) Please maintain the following relationship: CEN = (the actual number of pixel rows on the LCD) – 1 CEN ≥ DEN ≥ DST+ 9																									
ISOF	4	1H	Set the ISOLation clock in Front of COM pulse.																									
ISOB	4	0H	Set the ISOLation clock in Back of COM pulse.																									
WPC0	8	00H	Window program starting column address. Value range: 0 ~255.																									
WPP0	6	00H	Window program starting row address. Value range: 0~79. When DC[5:3]=100b, value range: 0~19																									
WPC1	8	FFH	Window program ending column address. Value range: 0~255.																									
WPP1	6	4FH	Window program ending row address. Value range: 0~79. When DC[5:3]=100b, value range: 0~19																									

**Register Table (continue)**

Name	Bits	Default	Description
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command <b>000</b> : <b>Idle</b> 001 : Read 010 : Erase                    011 : Program 1xx : For UltraChip debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore <b>1: Use</b>
MTPM	6	00H	MTP Write Mask.. 0: no action 1: program
APC	1	N/A	Advanced Product Configuration. For UltraChip only. Please do not use.
<b>Status Registers</b>			
OM	2	–	Operating Modes (Read Only) 00b: Reset      01b: (Not used) 10b: Sleep      11b: Normal
MD	1	–	MTP option flag. 0 : for non-MTP version.      1 : for MTP version
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded

**4.4 Command Table**

The following setting should be issue to LCD module after hardware reset.  
(It is an example only; it could be adjusted if necessary.)

	Command	A0	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default			
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A			
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A			
3.	Get Status	0	1	Ver	MX	MY	WA	DE	WS	MD	MS	Get Status	N/A			
				ID[1:0]			PMO[5:0]									
				Product Code				0	0	0	EF					
4.	Set Column Addr. LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0			
	Set Column Addr. MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0			
5.	Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C			
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC [1:0]	11b: 33~55 nF			
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC [3:2]	11b			
8.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0] R = 0~3	N/A			
				#	#	#	#	#	#	#	#					
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0			
	Set Scroll Line MSB			0	1	0	1	#	#	#	#	Set SL[7:4]	0			
10.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0			
	Set Page Address MSB			0	1	1	1	0	#	#	#	Set PA[6:4]	0			
11.	Set Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	PM=EAH			
				#	#	#	#	#	#	#	#					
12.	Set Isolation Clock Front	0	0	1	0	0	0	0	0	1	0	Set ISOF[3:0]	1H			
				0	0	0	1	0	0	1	1					
				-	-	-	-	#	#	#	#					
13.	Set Isolation Clock Back	0	0	1	0	0	0	0	0	1	0	Set ISOB[3:0]	0H			
				0	0	0	1	0	1	0	0					
				-	-	-	-	#	#	#	#					
14.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable			
15.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b			
16.	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0			
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[5:4]	10b:28kfps			
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0			
19.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0			
20.	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b			
21.	Set LCD Mapping Control (double-byte command)	0	0	1	1	0	0	0	0	0	0	Set LC[3:0]	0			
				0	0	0	0	#	#	#	#					
22.	Set N-line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H			
				-	#	#	#	#	#	#	#					
23.	Set Display Pattern	0	0	1	1	0	1	0	#	#	#	Set DC[7:5]	000b			
24.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A			
25.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A			
26.	Set test control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A			
				#	#	#	#	#	#	#	#					
27.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11			
28.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	159			
		0	0	#	#	#	#	#	#	#	#					
29.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0			
		0	0	#	#	#	#	#	#	#	#					
30.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159			
		0	0	#	#	#	#	#	#	#	#					

Note:  
Please refer to UC1611 data sheet for details  
R/W=0 means it is a write function, R/W=1 means it is a read function  
RS=0 means it is a control data, RS=1 means it is a display data

## Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping from high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free from twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module