

SPECIFICATION FOR APPROVAL

() Pr	elimin	ary S	pec	ificatio	n

(?) Final Specification

Title	20.1" UXGA TFT LCD					
BUYER		SUPPLIER	LG.Philips LCD CO., Ltd.			
MODEL		*MODEL	LM201U04			
		SUFFIX	A3			

^{*}When you obtain standard approval, please use the above model name without suffix

SIGNATURE	DATE
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RECORD OF REVISIONS

Revision No	Date	Page	Description
1.0	June. 05. 2003		Final specification

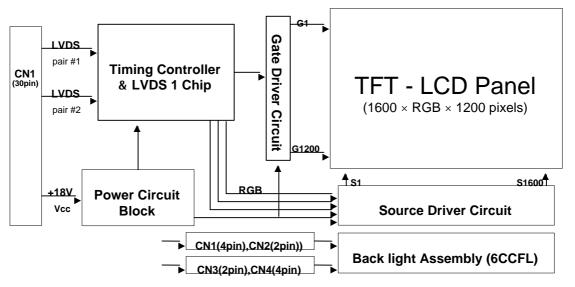


1. General Description

The LM201U04-A3 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has a 20.1 inch diagonally measured active display area with UXGA resolution(1200 vertical by 1600 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,777,216 colors.

The LM201U04-A3 has been designed to apply the interface method that enables low power, high speed,low EMI. FPD Link must be used as a LVDS(Low Voltage Differential Signaling) chip.

The LM201U04-A3 is intended to support applications where thin thickness, wide viewing angle, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LM201U04-A3 characteristics provide an excellent flat panel display for office automation products such as monitors.



General Features

Active screen size	20.1 inches (510.54mm) diagonal
Outline Dimension	432.0(H) x 331.5(V) x 25.0(D) mm(Typ.)
Pixel Pitch	0.255 mm x 0.255 mm
Pixel Format	1600 horizontal By 1200 vertical Pixels RGB stripe arrangement
Color depth	8-bits, 16,777,216 colors
Luminance, white	250 cd/m ² (Typ. Center 1 point)
Power Consumption	Total 35.1 Watt(Typ.), (4.5Watt @Vcc, 30.6 Watt @250cd/? [Lamp=7.5mA])
Weight	3200g (Typ.)
Display operating mode	Transmissive mode, normally black
Surface treatments	Hard coating (3H), Anti-glare treatment of the front polarizer

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2. Absolute Maximum Ratings

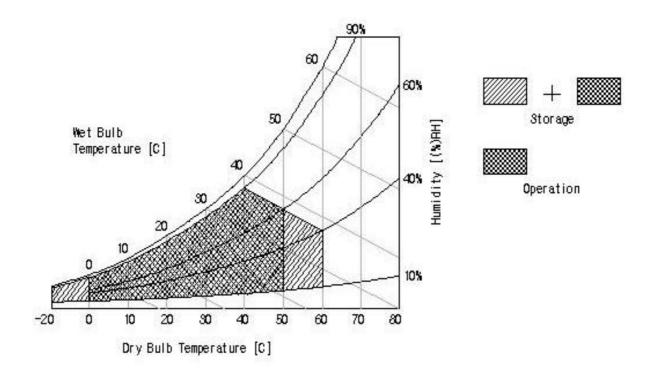
The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

_	Values					
Parameter	Symbol	Min.	Max.	Units	Notes	
Power Input Voltage Operating Temperature Storage Temperature Operating Ambient Humidity Storage Humidity	V _{CC} T _{OP} T _{ST} H _{OP} H _{ST}	- 0.3 0 - 20 10 10	+ 21 + 50 + 60 + 90 + 90	V _{dc} ? ? %RH %RH	at 25? 1 1 1 1	

Note: 1. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °C Max, and no condensation of water.



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3. Electrical Specifications

3-1. Electrical Characteristics

The LM201U04-A3 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

		Values				
Parameter	Symbol	Min.	Тур.	Max.	Units	Notes
MODULE: Power Supply Input Voltage Power Supply Input Current Power Consumption Differential Impedance Rush Current	V _{AA} I _{AA} P _c Zm I _{Rush}	17V	18V 0.25 4.5 100	19V 0.35 6.3	Vdc A W Ohm A	1 1 2 3
LAMP (each CCFL) Operating voltage Operating Current Established Starting Voltage at 25? at 0? Operating Frequency Power Consumption (6 CCFL's) Discharge Stabilization Time Life time	V _{BL} I _{BL} Vs F _{BL} P _{BL} Ts	650(8mA) 3.0 - - 40 - 40000	680 7.5 - - 50 30.6 -	815(3mA) 8.0 1250 1550 60 33.7 3	V _{RMS} mA V _{RMS} V _{RMS} KHZ Watts Minutes Hours	4 5 6 7 8 9

- Notes :1. The specified current and power consumption are under the V_{CC} =18.0V, 25°C, f_V =60Hz condition, Typical supply current is measured at the condition of 8 X 6 chess pattern(white & black)
 - 2. This impedance value is for impedance matching between LVDS T_X and the mating connector of the LCD.
 - 3. The duration of rush current is about 1ms.
 - 4. Operating voltage is measured at 25°C. The variance of the voltage is ±10%.
 - 5. The output voltage at the transformer in the inverter must be high considering to the loss of the ballast capacitor in the inverter. The voltage above V_S should be applied to the lamps for more than 1 second for start-up. Otherwise, the lamps may not be turned on.
 - 6. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
 - 7. The lamp power consumption shown above does not include loss of external inverter at 25°C. The used lamp current is the lamp typical current.
 - Let's define the brightness of the lamp after being lighted for 5 minutes as 100%.
 T_S is the time required for the brightness of the center of the lamp to be not less than 95%.
 The used lamp current is the lamp typical current.
 - 9. The life time is defined as the time at which brightness of lamp is 50% compare to that of initial value at the typical lamp current on condition of continuous operating at 25?2?C.

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Note. Do not attach a conducting tape to connecting wire.

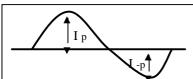
If the lamp wire attach to a conducting tape, TFT-LCD Module has a low luminance and the inverter has abnormal action. Because leakage current is occurred between lamp wire and conducting tape.

The design of the inverter must have specifications for the lamp in LCD Assembly. The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter(no lighting, flicker, etc) never occurs. When you confirm it, the LCD – Assembly should be operated in the same condition as installed in you instrument.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp.

It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter current and voltage waveform should be 10% below;
- b. The distortion rate of the current and voltage waveform should be within $v2 \pm 10\%$;
- c. The ideal sine current and voltage waveform shall be symmetric in positive and negative polarities.



- * Asymmetry rate = $|I_p I_{-p}| / I_{rms}$ * 100%
- * Distortion rate = I_p (or I_{-p}) / I_{rms}



3-2. Interface Connections

Interface chip must be used LVDS, part No. DS90CF383MTD(Transmitter) made by National Semiconductor. Or used the compatible interface chips(TI:SN75LVDS83).

This LCD employs seven interface connections, a 30-pin connector is used for the module electronics interface. Six 2-pin connectors are used for the integral back-light system.

The electronics interface connector is a model FI-XB30SRL-HF11 manufactured by JAE or used the connector MDF76RAW-30S-1H manufactured by HIROSE

The mating connector part number FI-X30M(JAE) or equivalent.

The pin configuration for the connector is shown in the table 3.

Table 3. MODULE CONNECTOR PIN CONFIGURATION(LVDS)

Symbol Vcc Vcc Vcc GND GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR1P SR1M SR0P SR0M	Supply voltage for LCD module Ground Ground Plus signal of even channel 3 (LVDS) Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Minus signal of even channel 0 (LVDS) Plus signal of even channel 0 (LVDS) Minus signal of even channel 0 (LVDS)	Second data
Vcc Vcc SND GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR1P SR1M SR0P SR0M	Supply voltage for LCD module Supply voltage for LCD module Supply voltage for LCD module Ground Ground Plus signal of even channel 3 (LVDS) Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
Vcc Vcc GND GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Supply voltage for LCD module Supply voltage for LCD module Ground Ground Plus signal of even channel 3 (LVDS) Minus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Minus signal of even channel 0 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
Vcc GND GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Supply voltage for LCD module Supply voltage for LCD module Ground Ground Plus signal of even channel 3 (LVDS) Minus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Minus signal of even channel 0 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
GND GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Ground Ground Plus signal of even channel 3 (LVDS) Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Minus signal of even channel 0 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
GND SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Ground Plus signal of even channel 3 (LVDS) Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Minus signal of even channel 0 (LVDS)	Second data
SR3P SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Plus signal of even channel 3 (LVDS) Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SR3M SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Minus signal of even channel 3 (LVDS) Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SCLKINP SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Plus signal of even clock channel (LVDS) Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SCLKINM SR2P SR2M SR1P SR1M SR0P SR0M	Minus signal of even clock channel (LVDS) Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SR2P SR2M SR1P SR1M SR0P SR0M	Plus signal of even channel 2 (LVDS) Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SR2M SR1P SR1M SR0P SR0M	Minus signal of even channel 2 (LVDS) Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SR1P SR1M SR0P SR0M	Plus signal of even channel 1 (LVDS) Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	Second data
SR1M SR0P SR0M	Minus signal of even channel 1 (LVDS) Plus signal of even channel 0 (LVDS)	
SR0P SR0M	Plus signal of even channel 0 (LVDS)	
SR0M		
	Minus signal of even channel 0 (LVDS)	
	ivilias signal of event originate of (EvDo)	
GND	Ground	
GND	Ground	
FR3P	Plus signal of odd channel 3 (LVDS)	
FR3M	Minus signal of odd channel 3 (LVDS)	
FCLKINP	Plus signal of odd clock channel (LVDS)	
FCLKINM	Minus signal of odd clock channel (LVDS)	
FR2P	Plus signal of odd channel 2 (LVDS)	First data
FR2M	Minus signal of odd channel 2 (LVDS)	
FR1P	Plus signal of odd channel 1 (LVDS)	
FR1M	Minus signal of odd channel 1 (LVDS)	
FR0P	Plus signal of odd channel 0 (LVDS)	
FR0M	Minus signal of odd channel 0 (LVDS)	
GND	Ground	
GND	Ground	
or pin arrangement er: BRL-HF11, JAE	30 1	
	GND GND FR3P FR3M FCLKINP FCLKINM FR2P FR2M FR1P FR1M FR0P FR0M GND GND r pin arrangement	GND GND GROUND FR3P FR3M FCLKINP FCLKINM FCLKINM FR2P FR2M FR2M FR2M FR2M FR2M FR2M FR1P FR1P FR1M FR1M FR1M FR1M FR1M FR1M FR1M FR1M

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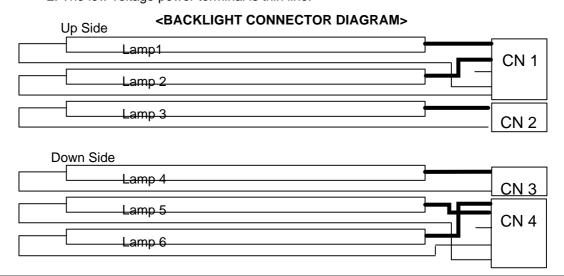
The backlight interface connector is a model BHSR-02VS-1(CN2/CN3) and BHR-05VS-1 (CN1/CN4) manufactured by JST. The mating connector part number are SM02B-BHSS-1-TB(2pin), SM04(9-E2)B-BHS-1-TB or equivalent. The pin configuration for the connector is shown in the table below.

Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION

No	Pin	Symbol	Description	Notes	
	11	HV	Power supply for lamp 1(High voltage side)	1	
CN1	2	HV	Power supply for lamp 2(High voltage side)	1	
	3 NC NC				
	4	LV	Power supply for lamp 1(Low voltage side)		
	5	LV	Power supply for lamp_2(Low voltage side)		
2015	11	HV	Power supply for lamp 3(High voltage side)	1	
CN2	2	LV	Power supply for lamp 3(Low voltage side)		
	1	HV	Power supply for lamp 4(High voltage side)	1	
CN3	2	LV	Power supply for lamp 4(Low voltage side)		
ON 4	1	HV	Power supply for lamp 6(High voltage side)	1	
CN4	2	HV	Power supply for lamp 5(High voltage side)	1	
3 NC NC		NC			
	4	LV	Power supply for lamp 6(Low voltage side)		
	5	LV	Power supply for lamp 5(Low voltage side)		

Notes: 1. The high voltage power terminal is thick line.

2. The low voltage power terminal is thin line.



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3-3. Signal Timing Specifications

This is the signal timing required at the input of the LVDS Transmitter. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

Table 5. Timing Table

ITEM		SYMBOL	Min	Тур	Max	Unit	Note
DCLK	DCLK Period		16.26	16.00	15.74	ns	
	Frequency	fclk	61.5	62.5	63.5	MHz	2pixel/clk
Hsync	Period	tHP	832	840	868		1
	Width-Active	twn	16	16	16	tCLK	2
Vsync	Period	tvp	1230	1240	1240	tHP	
	Frequency	fv	59	60	61	Hz	3
	Width-Active	twv	3	3	3	tHP	4
Data	Horizontal Valid	tн∨	800	800	800		
Enable	Horizontal Back Porch	tHBP	8	16	16	tCLK	
	Horizontal Front Porch	tHFP	8	8	36		
	Horizontal Blank	-	32	40	68		twn+ thbp+ thfp
	Vertical Valid	tvv	1200	1200	1200		
	Vertical Back Porch	t∨BP	25	35	35		
	Vertical Front Porch	tvfp	2	2	2	tHP	
	Vertical Blank	-	30	40	40		twv+ tvbp+ tvfp

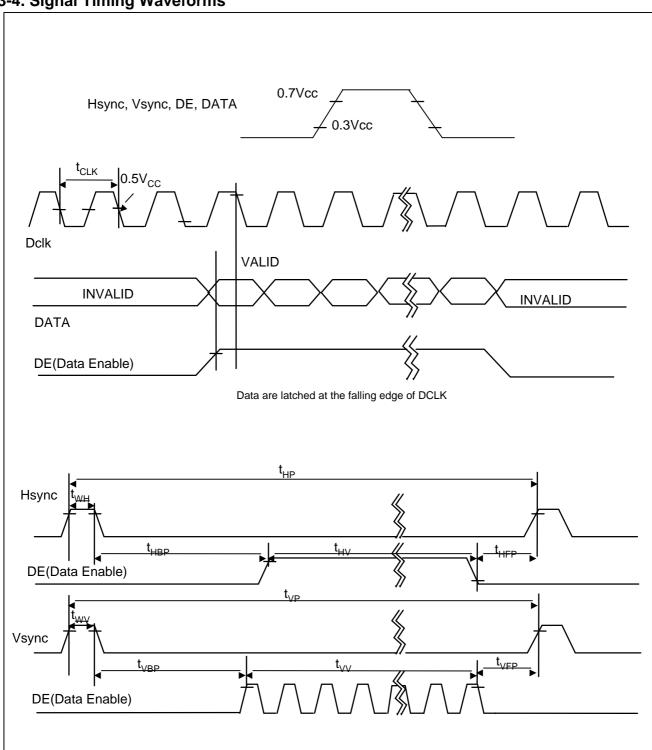
Notes: 1. Hsync period shall be a double number of 8

- 2. Horizontal sync shall be active high.
- 3. Vertical frequency should be keep the above specification when the resolution & mode are changed.
- 4. Vertical sync shall be active high.

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3-4. Signal Timing Waveforms





3-5. Color Input Data Reference

The brightness of each primary color(red,green and blue) is based on the 8-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Input Color Data																									
	Color				Re	ed							Gre	en							Bl	ue			
	Coloi	N	ISE	<u> </u>	ı			LS	B	N	ISB	-	ı	ı	ı	<u>LS</u>	<u>B</u>	N	ISB	<u> </u>	ı	ı	ı -	LS	В
	,	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	<u>G5</u>	<u>G4</u>	<u>G3</u>	<u>G2</u>	<u>G1</u>	<u>G0</u>	В7	<u>B6</u>	<u>B5</u>	<u>B4</u>	<u>B3</u>	<u>B2</u>	B1	B0
Basic Color	Black Red (255) Green (255) Blue (255) Cyan Magenta Yellow White	0 1 0 0 1 1 1	0 1 0 0 1 1	0 1 0 1 0 1	0 0 1 1 1 0																				
Red	Red(000) Dark Red(001) Red(002) Red(253) Red(254) Red(255) Bright	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 1 - 0 1	0 1 0 - 1 0 1	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0	0 0 0 - - 0 0
Green	Green(000) Dark Green(001) Green(002) Green(253) Green(254) Green(255) Bright	0 0 0 - 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0	0 0 0 - 0 0 0	0 0 0 0 0 0	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 1 - 0 1	0 1 0 - 1 0 1	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0	0 0 0 - - 0 0
Blue	Blue(000) Dark Blue(001) Blue(002) Blue(253) Blue(254) Blue(255) Bright	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 - 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	000 000	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 0 - 1 1	0 0 - - 1 1	0 0 1 - 0 1	0 1 0 - 1 0 1



3-6. Power Sequence

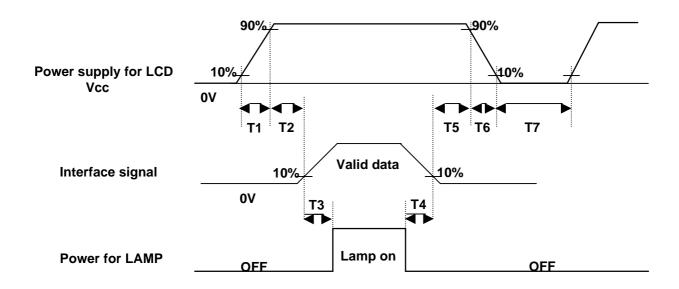


Table 7. POWER SEQUENCE

_				
Parameter	Min.	Тур.	Max.	Units
T 1	-	-	10	ms
T 2	0	-	50	ms
T 3	200	-	-	ms
T 4	200	-	-	ms
T 5	0	-	50	ms
T 6	-	-	10	ms
T 7	400	-	-	ms

Notes: 1. Please avoid floating state of interface signal at invalid period.

- When the interface signal is invalid, be sure to pull down the power supply for LCD V_{CC} to 0V. Invalid signal with Vcc for a long period of time, causes permanent damage to LCD panel.
- 3. Lamp power must be turn on after power supply for LCD and interface signals are valid.

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4. Optical Specifications

Optical characteristics are determined after the unit has been 'ON' for 30 minutes in a dark environment at 25 °C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of ? and ? equal to 0 °.

FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

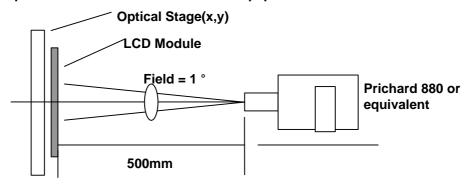


Table 8. OPTICAL CHARACTERISTICS (Ta=25 °C, V_{CC}=18.0V, f_V=60Hz Dclk=125MHz, I_{BL}=7.5mA)

Б			Values		11.5	N
Parameter	Symbol	Min	Тур	MAx	Units	Notes
Contrast Ratio	CR	250	400			1
Surface Luminance, white	LL _{WH}	200	250		cd/m ²	2
Luminance Variation.	? ₩HFT E	65			%	3
Luminance Uniformity (T.CO.99)	L _R			1.7		4
Response Time	Tr		1.6	25	ms	5
.Rise Time	Tr _R		9			
Decay Time	Tt _D		7			
Color Coordinates						
.RED	RX	802.0	0.638	0.668		
	RY	0.312	0.342	0.372		
.GREEN	GX	Q.263	0.293	0.323		
	GY	0.579	0.609	0.639		
.BLUE	BX	Q.117	0.147	0.17.7		
	BY	0.038	820.0	0.098		
.WHITE	WX	0.283	0.313	0.343		
	W.Y	0.299	0.329	Q.359		
Viewing Angle						
x axis, right(?=0°).	?r	85	88		degree	6
.x.axis, left (?=180°)	<u>?l</u>	85	88		<u> </u>	
.y.axis, up (?=90°).	?u	85	88			
y axis, down (?=270°).	?d	85	88			
Crosstalk		.		1.8%		7
Gray Scale Value			2.2			8

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Notes: 1. Contrast Ratio(CR) is defined mathematically as:

Surface Luminance with all white pixels

Contrast Ratio =

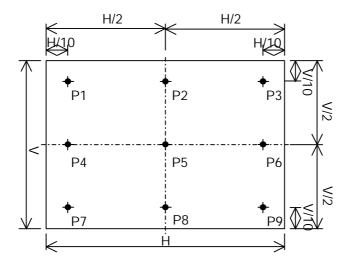
Surface Luminance with all black pixels

Contrast ratio shall be measured at the center of the display (Location P1).

- 2. Surface Luminance (L_{WH}) is measured at the center point (location P1) with all pixels displaying white
- 3. The variation in surface luminance, dWHITE is defined as :

dWHITE =
$$\frac{\text{Minimum } (P_1, P_2,P_9)}{\text{Maximum } (P_1, P_2,P_9)}$$
? 100(%)

Where P1 to P9 are the luminance with all pixels displaying white at 9 locations.

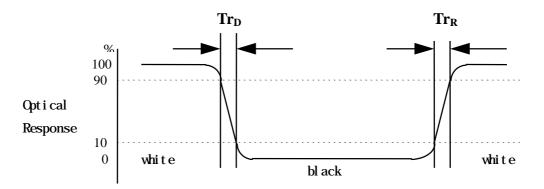


4. TCO'99 Certification Requirements and test methods for environmental labeling of display [flat] Report No.2 (×1.5.2. Luminance Uniformity)
LR = (LMAX.+ 30deg. / LMIN.+ 30deg.) + (LMAX.- 30deg. / LMIN. - 30deg.)) / 2

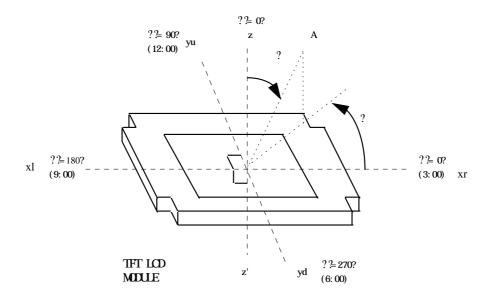
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5. The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

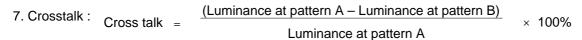


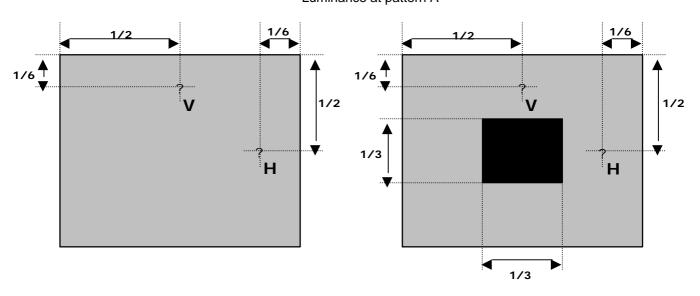
6. Viewing angle is the angle at which the contrast ratio is greater than 10.



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Pattern : A (Background : 127-Gray or White)

Pattern : B (Window : Black) (Background : 127-Gray or White)

8. Gray Scale

Gray Level	Relative Luminance (%) Typ.
	71
0	0.3
31	1.1
63	4.57
95	11.3
127	21.4
159	35.2
191	52.8
223	74.4
255	100



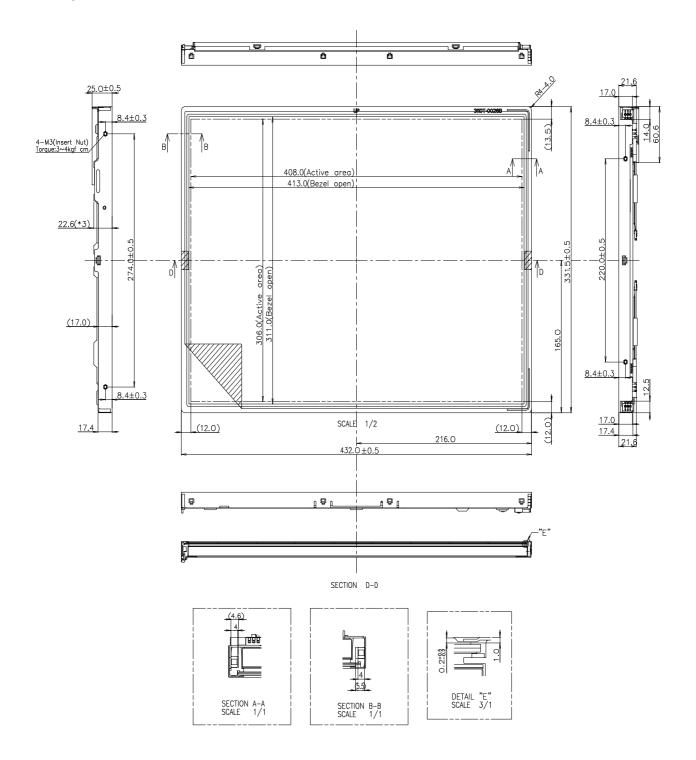
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LM201U04-A3 . In addition, the figures in the next page are detailed mechanical drawing of the LCD.

	Horizontal	432.0 ± 0.5 mm					
Outside dimensions	Vertical	331.5 ± 0.5 mm					
	Depth	25.0 ± 0.5 mm					
	Horizontal	413.0 mm					
Bezel area	Vertical	311.0 mm					
	Horizontal	408.0 mm					
Active display area	Vertical	306.0 mm					
Weight (approximate)	3,200g (Typ.)						
Surface Treatment	Hard coating (3H) Anti-glare treatment of the front polarizer Haze (25%)						

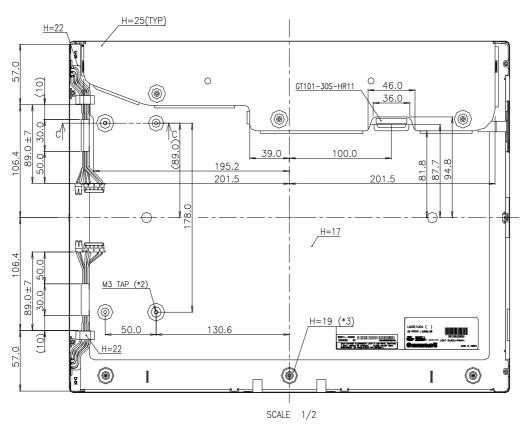


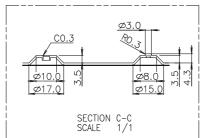
<FRONT VIEW>





<REAR VIEW>





- NOTES

 1. Unspecified tolerances are to be ±0.5mm.

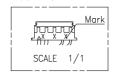
 2. Both backlight wires and contraction tubes are excluded from outline dimensions.

 3. Tilt and partial disposition tolerance of display area are as following.

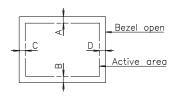
 (1) Y—Direction: IA—BI ≤1.0mm

 (2) X—Direction: IC—DI ≤1.0mm

 4. Lamp(CCFL) lot No.is marked at backlight connector.









6. Reliability

Environment test condition

No.	Test Item	Conditions					
1	High temperature storage test	Ta= 60°C 240h					
2	Low temperature storage test	Ta= -20°C 240h					
3	High temperature operation test	Ta= 50°C 60%RH 240h					
4	Low temperature operation test	Ta= 0°C 240h					
5	Vibration test (non-operating)	Waveform : Random Vibration level : 1.0G RMS Bandwidth : 10 ~ 500Hz Duration : X,Y,Z 10min One time each direction					
6	Shock test (non-operating)	Shock level : 100G Waveform: half sine wave, 2ms Direction : ±X, ±Y, ±Z One time each direction					
7	Altitude storage / shipment operating	0 - 40,000 feet(12,192m) 0 - 12,000 feet (3657.6m)					

[{] Result Evaluation Criteria }

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

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7. International Standards

7-1. Safety

a) UL 60950, Third Edition, Underwriters Laboratories, Inc., Dated Dec. 11, 2000.

Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment.

b) CAN/CSA C22.2, No. 60950, Third Edition, Canadian Standards Association, Dec. 1, 2000.

Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment.

c) EN 60950 : 2000, Third Edition

IEC 60950: 1999, Third Edition

European Committee for Electrotechnical Standardization(CENELEC)

EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7-2. EMC

- a) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. "American National Standards Institute(ANSI), 1992
- b) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special Committee on Radio Interference.
- c) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization.(CENELEC), 1998 (Including A1: 2000)



8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A B C D E F G H I J K L

A,B,C: Inch
D: Year
E: Month
F: Panel Code
G: Factory Code
H: Assembly Code
I,J,K,L,M: Serial No

Note

1. Year

- 1	. 1 Oui											
	Year	97	98	99	2000	2001	2002	2003	2004	2005	2006	2007
	Mark	7	8	9	0	1	2	3	4	5	6	7

2. Month

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	Α	В	С

3. Panel Code

Panel Code	P1 Factory	P2 Factory	P3 Factory	P4 Factory	P5 Factory	Hydis Panel
Mark	1	2	3	4	5	Н

4. Factory Code

T. I actory Code	,	
Factory Code	LPL Gumi	LPL Nanjing
Mark	K	C

5. Serial No

Serial No.	1 ~ 99,999	100,000 ~
Mark	00001 ~ 99999	A0001 ~ A9999, , Z9999

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module. This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box: 5 pcs

b) Box Size : $530mm \times 307mm \times 453mm$



9. PRECAUTIONS

Please pay attention to the following when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force(ex. Twisted stress) is not applied to the module.
 - And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach a transparent protective plate to the surface in order to protect the polarizer.

 Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not describe because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are determined to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
 And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can not be operated its full characteristics perfectly.

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9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.

 It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) The protection film is attached to the bezel with a small masking tape When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

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APPENDIX 1. REQUIRED SIGNAL ASSIGNMENT FOR FlatLink(TI:SN75LVDS83) Transmitter

Pin #	Pin Name	Require Signal	Pin #	Pin Name	Require Signal
1	vcc	Power Supply for TTL Input	29	GND	Ground pin for TTL
2	D5	TTL Input (R7)	30	D26	TTL Input (DE)
3	D6	TTL Input (R5)	31	T _X CLKIN	TTL Level clock Input
4	D7	TTL Input (G0)	32	PWR DWN	Power Down Input
5	GND	Ground pin for TTL	33	PLL GND	Ground pin for PLL
6	D8	TTL Input (G1)	34	PLL VCC	Power Supply for PLL
7	D9	TTL Input (G2)	35	PLL GND	Ground pin for PLL
8	D10	TTL Input (G6)	36	LVDS GND	Ground pin for LVDS
9	VCC	Power Supply for TTL Input	37	TxOUT3+	Positive LVDS differential data output 3
10	D11	TTL Input (G7)	38	TxOUT3-	Negative LVDS differential data output 3
11	D12	TTL Input (G3)	39	T _X CLKOUT+	Positive LVDS differential clock output
12	D13	TTL Input (G4)	40	T _X CLKOUT-	Negative LVDS differential clock output
13	GND	Ground pin for TTL	41	T _X OUT2+	Positive LVDS differential data output 2
14	D14	TTL Input (G5)	42	T _X OUT2-	Negative LVDS differential data output 2
15	D15	TTL Input (B0)	43	LVDS GND	Ground pin for LVDS
16	D16	TTL Input (B6)	44	LVDS VCC	Power Supply for LVDS
17	VCC	Power Supply for TTL Input	45	T _X OUT1+	Positive LVDS differential data output 1
18	D17	TTL Input (B7)	46	T _X OUT1-	Negative LVDS differential data output 1
19	D18	TTL Input (B1)	47	T _X OUT0+	Positive LVDS differential data output 0
20	D19	TTL Input (B2)	48	T _X OUT0-	Negative LVDS differential data output 0
21	GND	Ground pin for TTL Input	49	LVDS GND	Ground pin for LVDS
22	D20	TTL Input (B3)	50	D27	TTL Input (R6)
23	D21	TTL Input (B4)	51	D0	TTL Input (R0)
24	D22	TTL Input (B5)	52	D1	TTL Input (R1)
25	D23	TTL Input (RSVD)	53	GND	Ground pin for TTL
26	VCC	Power Supply for TTL Input	54	D2	TTL Input (R2)
27	D24	TTL Input (HSYNC)	55	D3	TTL Input (R3)
28	D25	TTL Input (VSYNC)	56	D4	TTL Input (R4)

Notes: Refer to LVDS Transmitter Data Sheet for detail descriptions.