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DEVICE SPECIFICATION FOR

Dot Matrix LCD Unit
(20-character/2-line Display
STHC gray type)

MODEL No.

LM20A21

☐ CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

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LM20A21

1. Overview

The **LM20A21**, dot-matrix LCD unit consists of a 5 x 7-dot 20-character 2-line dot-matrix LCD panel, LCD driver and controller LSI fabricated on a single PCB. Incorporating mask **ROM-based** character generator and display data **RAM** in the controller LSI, the unit can efficiently display the desired characters under microprocessor control.

(Features)

- (1) The LCD of the unit is **STHC (Super Twisted High Contrast)** gray type.
 - (2) Low power consumption with the dot-matrix LCD panel and CMOS LSI.
 - (3) Thin, lightweight design permits easy installation in a **variety** of equipment.
 - (4) Allowing for being connected at general-purpose CMOS signal level, the unit can be easily interfaced to a microprocessor with common 4-bit and 8-bit parallel inputs and outputs.
 - (5) Built-in character generator **ROM** and RAM, and display data RAM:
 - Character **generator ROM**
 - 160 different 5 x 7 dot-matrix character patterns
 - (Alphanumeric and symbols)
 - Character generator **RAM**
 - 8 different user programmed 5 x 7 dot-matrix patterns
 - Display data **RAM**
 - 80 x 8 bits
 - (6) Numerous instructions
 - Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift
 - (7) Built-in reset circuit is triggered at power ON.
(For the operating conditions, refer to the separate user's manual "Dot-Matrix LCD Units with built-in controllers".)
 - (8) The unit operates from a single 5V power supply.
- * As to the **packing**, refer to the separate "COMMON PACKING SPECIFICATION FOR LM20255 series".

SHARP**2. Construction and Outline**

Construction : 5 x 7 dots + cursor, 20-character 2-line dot-matrix display unit

Outline : See Fig. 7.

Interface signals : See Table 5.

Character pattern details : See Fig. 7.

Character codes : See Table 8.

There shall be no scratches, stains, chips, distortions and other external **drawbacks** that may affect the display function.

Rejection criteria shall be noted in Inspection Standard (S-U- 009).

3. Mechanical SpecificationsTable 1

Parameter	Specification	Unit
Outline dimensions	115 (W) X 36(H) X11 MAX (D)	mm
Effective display area	83(W) X 18.6(H)	mm
Display format	20 characters X 2 lines	
Character format	5 X 7 dots with cursor	
Character size	3.2(W) X 4.85 (H) (5 X 7 dots)	mm
Dot size	0.6(W) X 0.65(H)	mm
Dot spacing	0.05	mm
Character color *	Dark blue	
Background color*	Gray	
Weight	Approx. 40	g

* Due to the characteristics of the LC Material, the colors vary with environmental temperature.

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4. Electrical Specifications

4.1 Absolute maximum ratings

Table 2

Parameter	Symbol	Hin.	Max.	Unit	Remark
Supply voltage(Logic)	$V_{DD} - V_{SS}$	-0.3	+6.5	V	
Supply voltage (LCD drive)	$V_O - V_{SS}$	0	+6.5	v	$V_{DD} > V_O$
Input voltage	V_{IN}	-0.3	$V_{DD} + 0.3$	V	
Storage temperature	Tstg	-25	+70	“C	
Operating temperature	Topr	0	+50	“C	

4.2 Electrical characteristics

Table 3

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	flax.	Unit	Condition
Supply voltage (Logic)		$V_{DD} - V_{SS}$	4.75	5.0	5.25	v	
Supply voltage (LCD drive)		$V_O - V_{SS}$		0.5		v	$V_{DD} = 5.0V$
Input voltage	" L "	V_{IL}	-0.3	-	0.6	v	
	" H "	V_{IH}	2.2	-	V_{DD}	v	
Output voltage	" L "	V_{OL}			0.4	v	$I_{OL} = 1.2mA$
	" H "	V_{OH}	2.4	-	-	v	$-I_{OH} = 0.205mA$
Input leakage current		I_{IL}			1	μA	
Internal oscillating frequency		fosc		250		KHz	
Supply current		I_{DD}		1.8	2.5	mA	$V_{DD} = 5V$ $V_O = 0V$
Power dissipation		Pd		9	12.5	mW	

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4.3 Timing characteristics

Table 4

 $V_{DD}=5.0V \pm 5\%$ $T_a = 0 \sim 50^\circ C$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cycE}	1000	-	-	ns
Enable pulse width	PW_{EH}	450	-	-	ns
Enable rise/fall time	t_{Er}, t_{Ef}	-		25	ns
RS, R/W setup time	t_{AS}	140	-	-	ns
Address hold time	t_{AH}	10	-	-	ns
Data setup time	t_{DSW}	195	-	-	ns
Data delay time	t_{DDR}			320	ns
Data hold time (write)	t_H	10	-		ns
Data hold time (read)	t_{DHR}	20	-	-	ns

Timing chart: See Fig. 1.

4.4 Interface signals

Table 5

Pin No.	Symbol	Description	Connection
1	V_{SS}	Ground potential	GND : 0V
2	V_{DD}	Power supply	+5V
3	V_0	Contrast adjustment voltage	Adjust the contrast by changing the supply voltage from 0V to 5V.
4	RS	Register select signal	Control signal inputs (For details, see section 6 and 7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	DB_0	Code I/O data LSB	Data bus line · DB_7 may also be used to check the busy flag. · Lines $DB_0 \sim DB_3$ are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
8	DB_1	Code I/O data 2nd bit	
9	DB_2	Code I/O data 3rd bit	
10	DB_3	Code I/O data 4th bit	
11	DB_4	Code I/O data 5th bit	
12	DB_5	Code I/O data 6th bit	
13	DB_6	Code I/O data 7th bit	
14	DB_7	Code I/O data MSB	

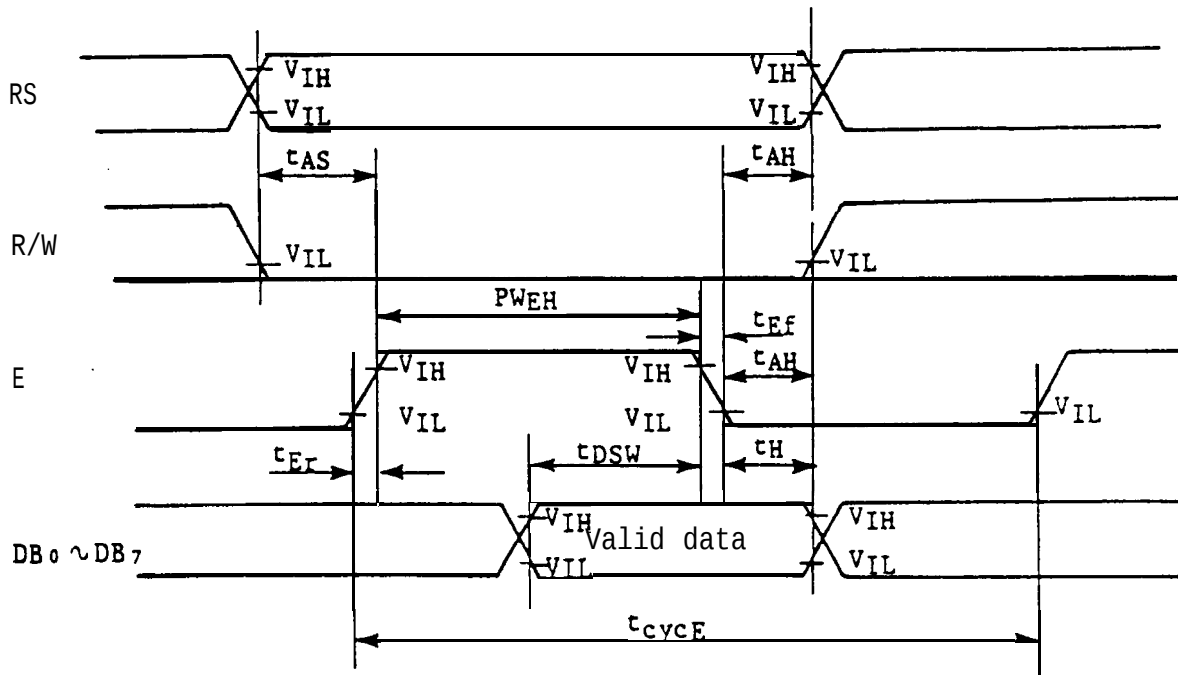
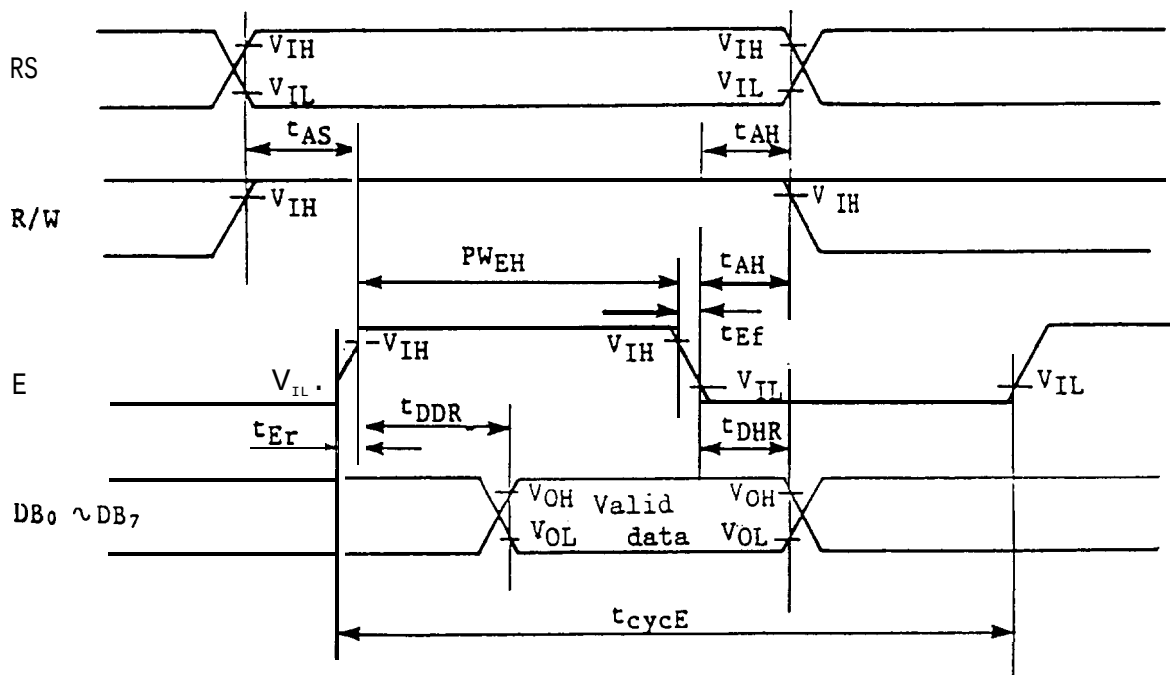
SHARPWrite OperationRead Operation

Fig. 1 Timing Chart

SHARP5. Optical Characteristics

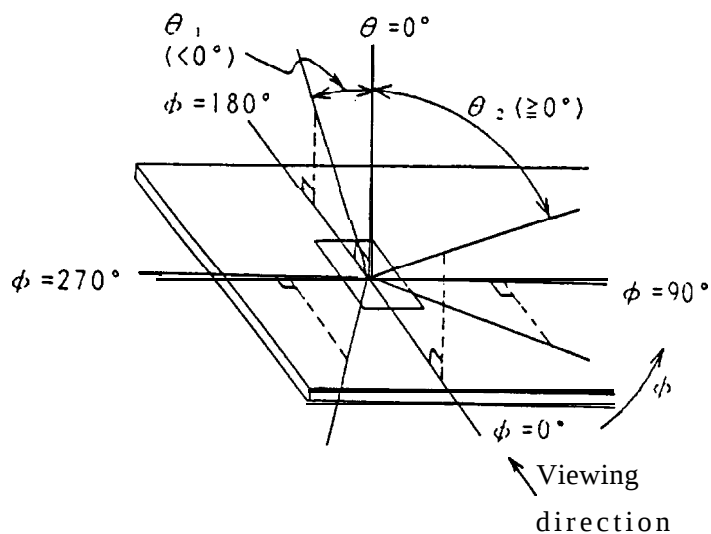
Table 6 shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in $\theta = 0^\circ$.

Table 6

(Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	$\theta_2 - \theta_1$	$\phi = 0^\circ$ $C_0 \geq 2.0$	60	-	-	dgr.	Note 1
	θ_1	$\theta_1 < \theta_2$ $C_0 = 2.0$	-	-	-25	dgr.	Note 1
	θ_2		25	-	-		
	$\theta_2 - \theta_1$	$\phi = 45^\circ$ $C_0 \geq 2.0$	60	-	-	dgr.	Note 1
	θ_1	315" $C_0 = 2.0$	-	-	-25	dgr.	Note 1
	θ_2		25	-	-		
Contrast ratio	C_0	$\theta = 0^\circ, \phi = 0^\circ$	3.0	5.0	-		Note 2
Response time	Rise	$e = 0''$, $\phi = 0^\circ$	-	150	250	ms	Note 3
	Decay	$\theta = 0''$, $\phi = 0^\circ$	-	150	250	ms	Note 3

Note 1) The viewing angle range is defined as shown below.



* Angles θ_1 , θ_2 and ϕ shall fall within the range over which the displayed character can be read.

Fig.2 Definition of viewing angle

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Note 2) Contrast ratio is defined **as** follows:

When input signal is applied to the unit to select (turn on) the LCD dots **(pixels)** to be measured in the optical characteristics test method as defined in Fig. 3.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

Measurement wave length $\lambda = 580\text{nm}$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig. 3. The response characteristics of the photo-detector output are measured as shown in Fig. 4.

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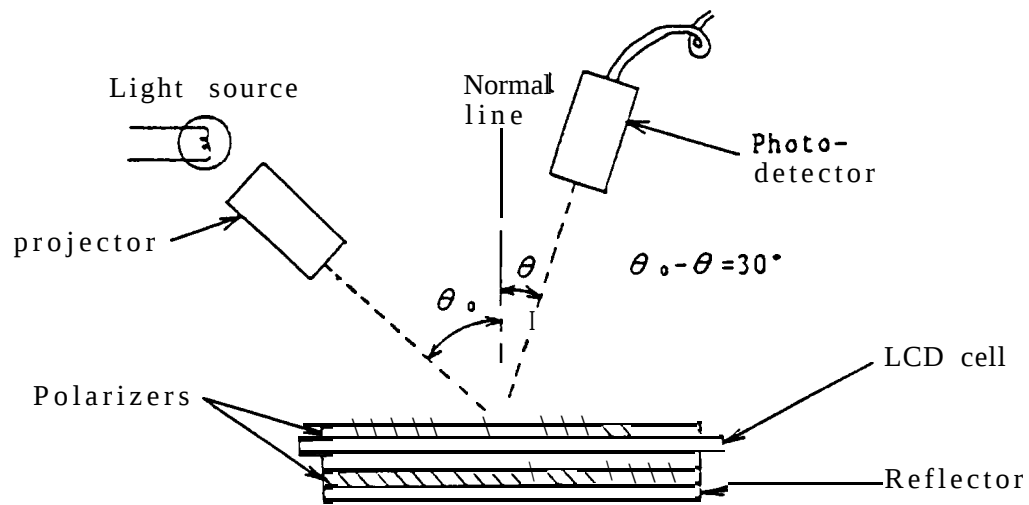


Fig. 3 Optical Characteristics Test Method

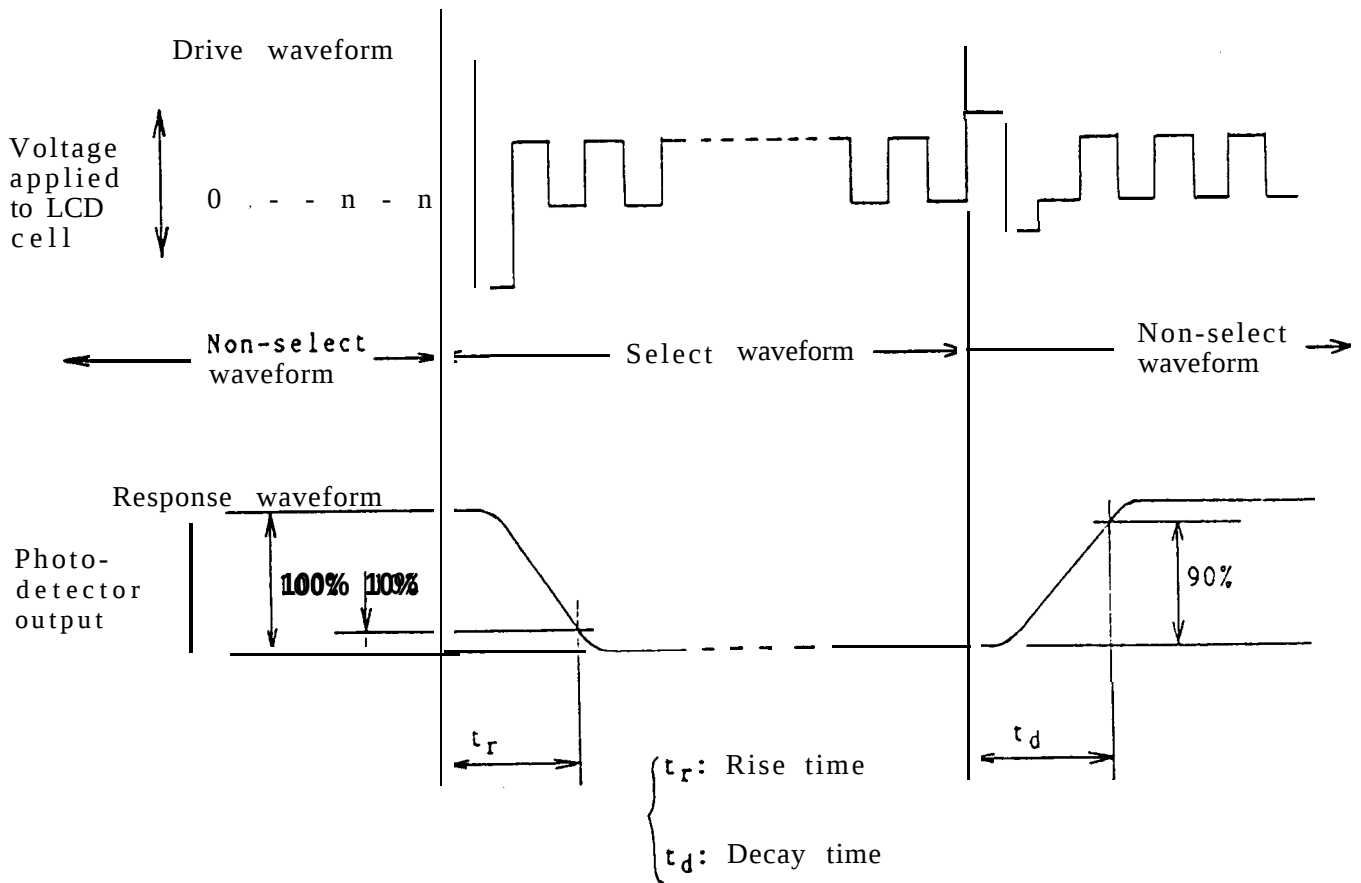


Fig. 4 Definition of Response Time



6. Pin Description

1) V_{DD} and V_{SS} Pins

V_{DD} and V_{SS} pins are for power supply. V_{SS} pin is "grounded, and V_{DD} pin is supplied with +5V. Each voltage necessary to drive LCD is generated in the unit.

2) RS Pin

The controller LSI has two 8-bit registers; an instruction register (IR) and a data register (DR). RS signal selects these registers.

IR stores instruction codes such as display clear, shift, etc. and also stores address information for the display data RAM (DD RAM), character generator RAM (CG RAM); DR is used for temporarily storing data to be written into DD RAM and CGRAM.

“ 0 “ :Instruction register (when writing)

Busy flag register; address counter (when reading)

“ 1 “ :Data register (read/write)

3 R/W Pin

Read or write select signal pin.

“ 0 “ :Writing

“ 1 “ :Reading

4) E Pin

Data read or write operation enable signal pin.

5) $DB_0 \sim DB_7$ Pins

Data bus with three-state, bidirectional function for use in data transactions with MPU. DB_7 may also be used to check the busy flag.

$DB_0 \sim DB_3$ are not used when interfacing with a 4 - bit microprocessor.

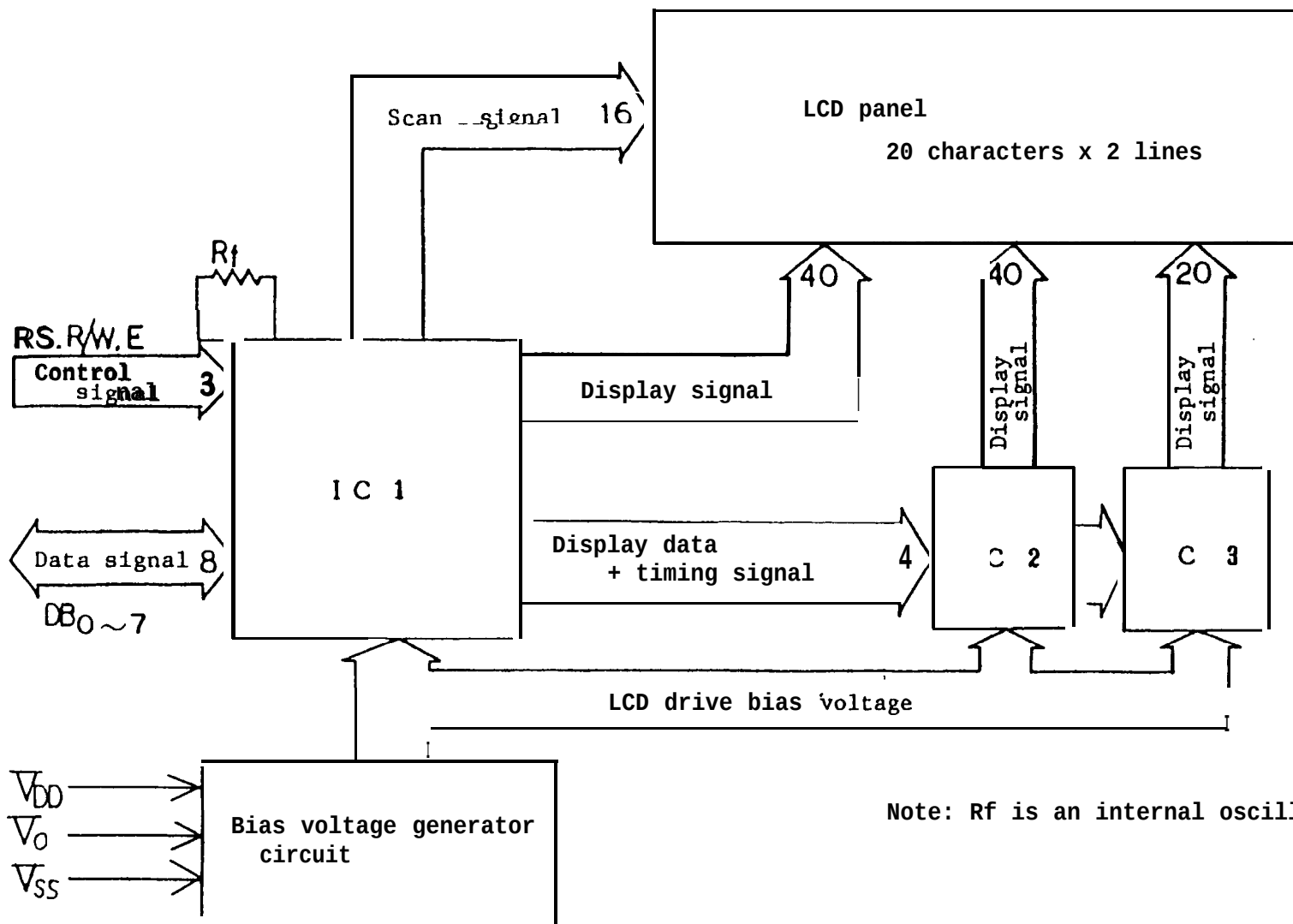
6) V_0 Pin

Viewing angle is varied and contrast is adjusted by changing voltage between +5V $\sim$ 0V by applying bias voltage to the LCD driver.

7. Instruction Set

Table 7

Instruction	Cod e										Function	
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀		
Display clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H.	
Display/cursor home	0	0	0	0	0	0	0	0	1	0	Restore display from shift and load address counter with DD RAM address 00H.	
Entry mode set	0	0	0	0	0	0	0	1	I/D	s	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.	
Display ON/OFF	0	0	0	0	0	0	1	D	c	B	specify activation of display (D), cursor(C), and blinking of character at cursor position (B).	
Display/cursor shift	0	0	0	0	0	1	S/C	R/L	0	*	Shift display or move cursor.	
Function set	0	0	0	0	1	DL	1	0	*	0	Set interface data length (DL).	
CGRAM address set	0	0	0	1	ACG						Load the address counter with a CC RAM address. Subsequent data is CC RAM data.	
DD RAM address set	0	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data is DD RAM data.	
Busy flag/address counter read	0	1	BF	AC							Read busy flag (BF) and contents of address counter (AC).	
CGRAM/DD RAM data write	1	0	Write data								Write data to CC RAM or DD RAM.	
CC RAM/DD RAM data read	1	1	Read data								Read data from CGRAM or DD RAM.	
I/D - I: increment, S = 1: Shift display, D = 1: Display ON, c = 1: Cursor ON, B = 1: Character at cursor position blinks. I/D - O: Decrement S - O: Freeze display D - O: Display OFF c = 0: Cursor OFF B - O: Character at cursor position unblinks SIC - I: Shift display, R/L - I: Shift right, DL = 1: 8-bit, BF = 1: During internal operation, S/C = 0: Move cursor R/L - O: Shift left DL - O: 4-bit BF - O: End of internal operation												



Note: R_f is an internal oscillating resistor.

Fig. 5 Block Diagram

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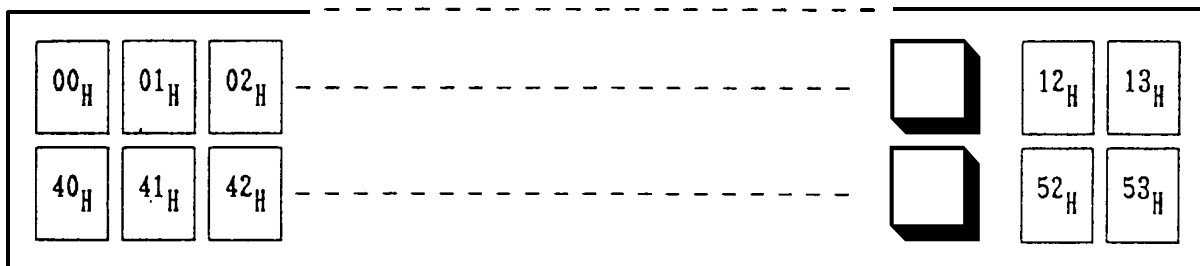


Fig.6 Display Address (When the display is not shifted)

Table 8 Input Code vs. Character Pattern

*1 *2 4bit 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												*
xxxx0001	(2)												*
xxxx0010	(3)												*
xxxx0011	(4)												*
xxxx0100	(5)												*
xxxx0101	(6)												*
xxxx0110	(7)												*
xxxx0111	(8)												*
xxxx1000	(1)												*
xxxx1001	(2)												*
xxxx1010	(3)												*
xxxx1011	(4)												*
xxxx1100	(5)												*
xxxx1101	(6)												*
xxxx1110	(7)												*
xxxx1111	(8)												*

Note 1. CG RAM Is character generator RAM in which user-definable character pattern are stored.

Note 2. Xmark: prohibition of input

*1 High-order *2 Low-order

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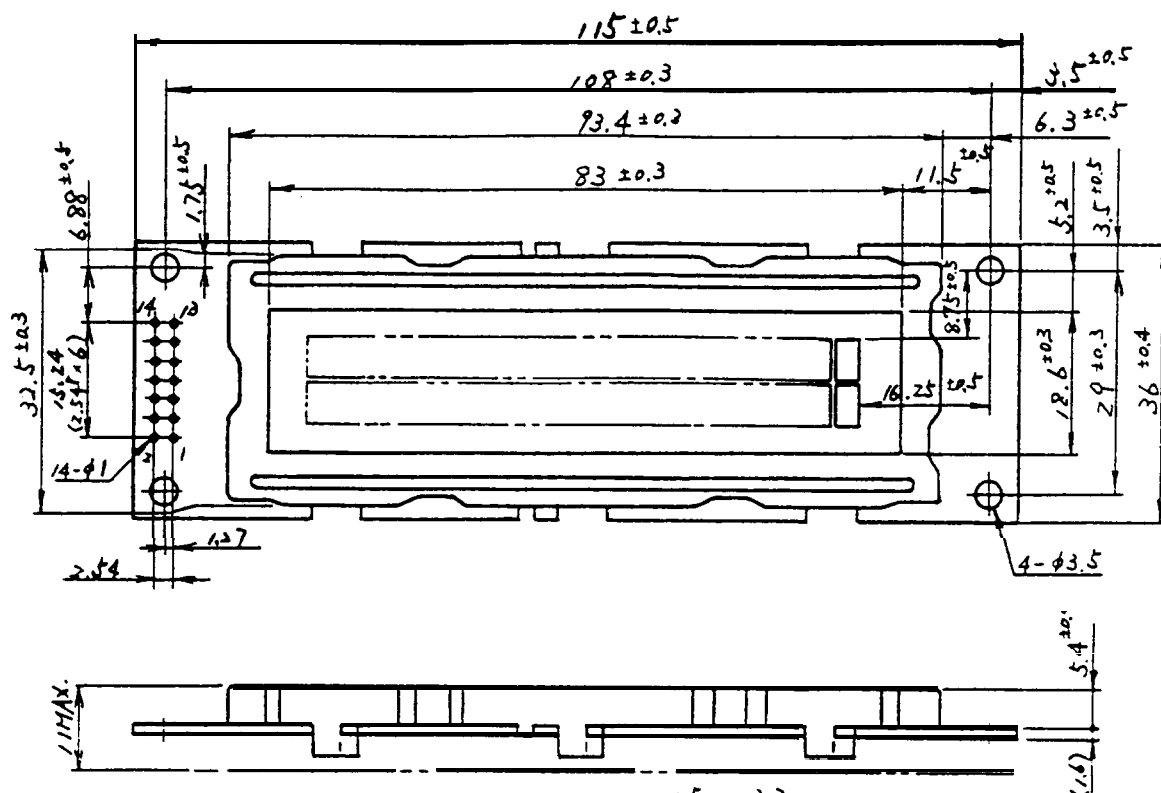
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設計通報
DRAWING INFO.連絡書
INFORMATION

No. () 号によ

新設・変更・書換
NEW CHANGE REPLACE. 図面

Fig.7 Unit Outline Dimensions and Pin Connections

Character Pattern
Details指示なき寸法公差は とする
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N No.	Sig.	PIN No.	Sig.
4	DB7	13	DB6
2	DB5	11	DB4
0	DB3	9	DB2
3	DB1	7	DB0
5	E	5	R/W
1	RS	3	V _o
1	V _{DD}	1	V _{SS}

19	19	LM20A21	名 称 NAME	Outline Dimensions and Pin Connections
年 月 日 DATE	訂 正 記 事 REVISE	投 通 号 PREPA	相 当 MODEL	記 号 SYMBOL
材 質 MATERIAL	板 厚 THICKNESS	仕 上 FINISH	尺 度 SCALE	部 品 コード PARTS CODE
1/1			1/1	作 成 日 付 DATE
1988	6	16	図 番 DRAWING No.	OD20A21-301C