LM211

- 480 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Recommendable control LSI HD61830 type (see page 76)

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 82H x 13D (max.) mm
Effective display area	240W x 38H mm
Number of dots	480W x 64H dot
Dot size	0.44W x 0.44H mm
Pitch	0.49W x 0.49H mm
Weight	about 180 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −9.0V ± 0.45 V

Input "high" voltage (Vi_H)	0.7 x V_{DD} V min.
Input "low" voltage (Vi_L)	0.3 x V_{DD} V max.
Clock frequency (f_{CL2})	610 kHz min.
	920 kHz typ.
	1200 kHz max.
Power supply current (I_{DD})	16 mA typ.
(I_{EE})	6 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Du=1/64	
at Ta = 0°C	13.3 V typ.
at Ta = 25°C	11.9 V typ.
at Ta = 40°C	10.6 V typ.
OPTICAL DATA	See page 8

INTERFACE TABLE

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H/L	The CL1 latches the serial data in the shift registers
5	CL2	H/L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

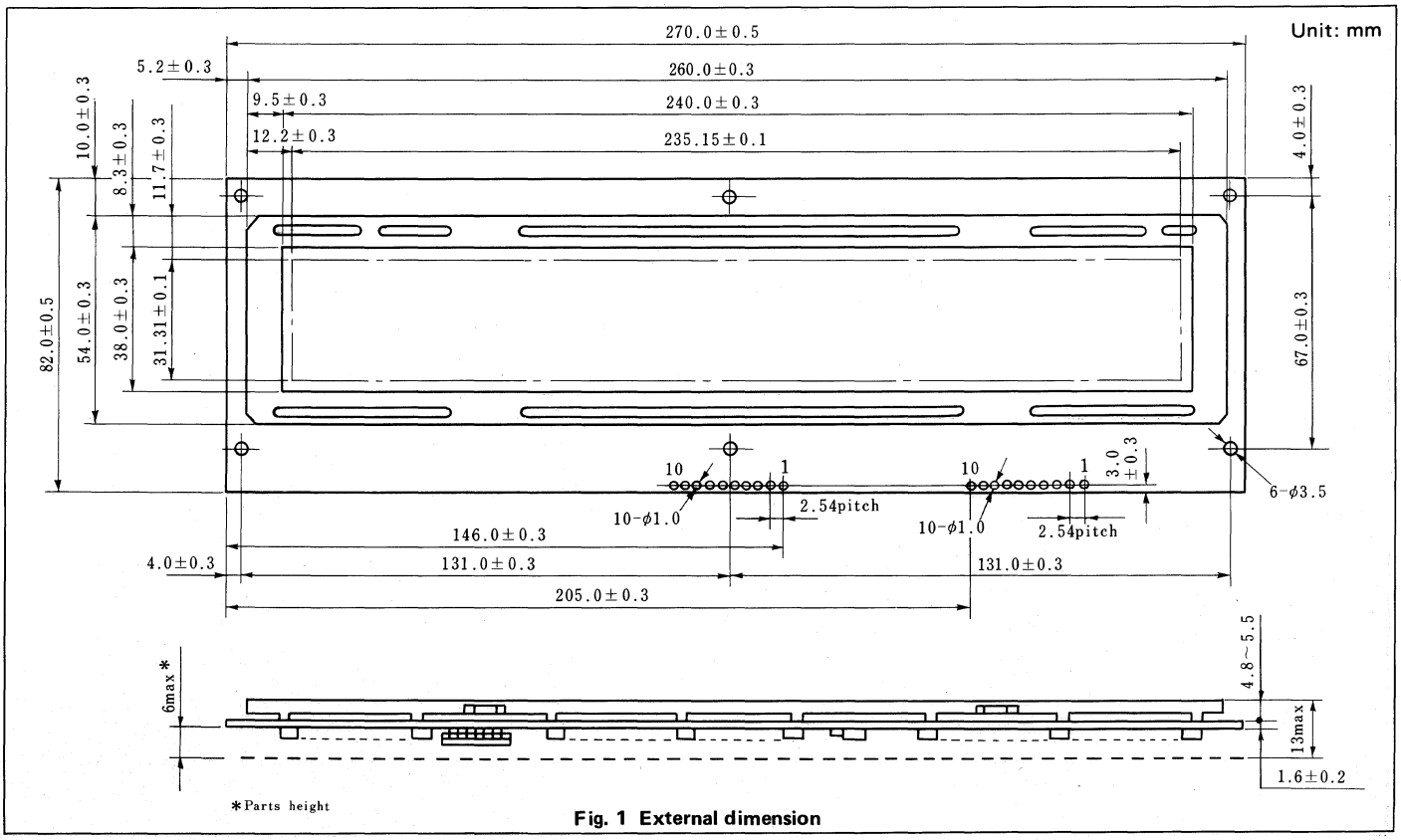


Fig. 1 External dimension

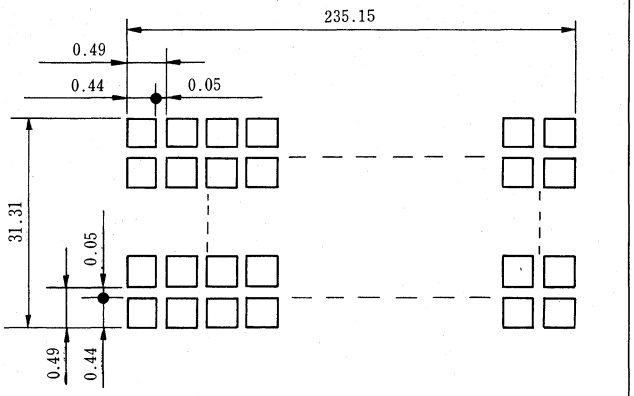


Fig. 2 Display pattern

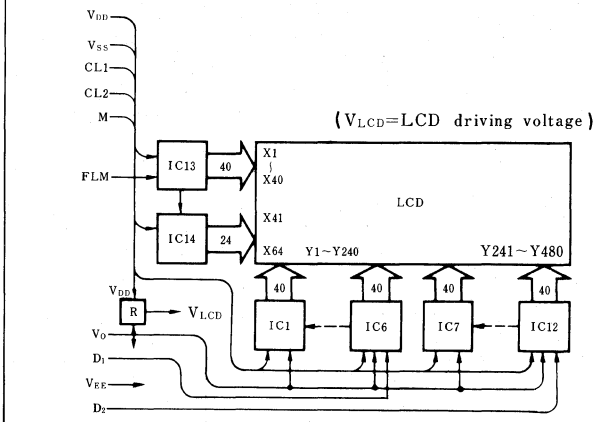
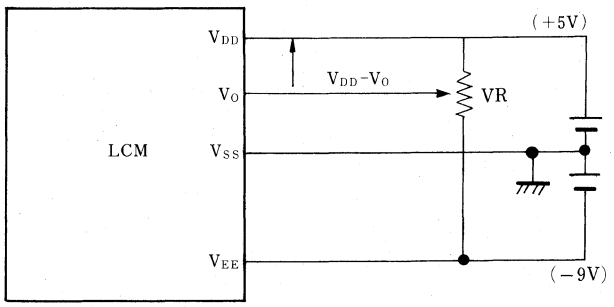


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply

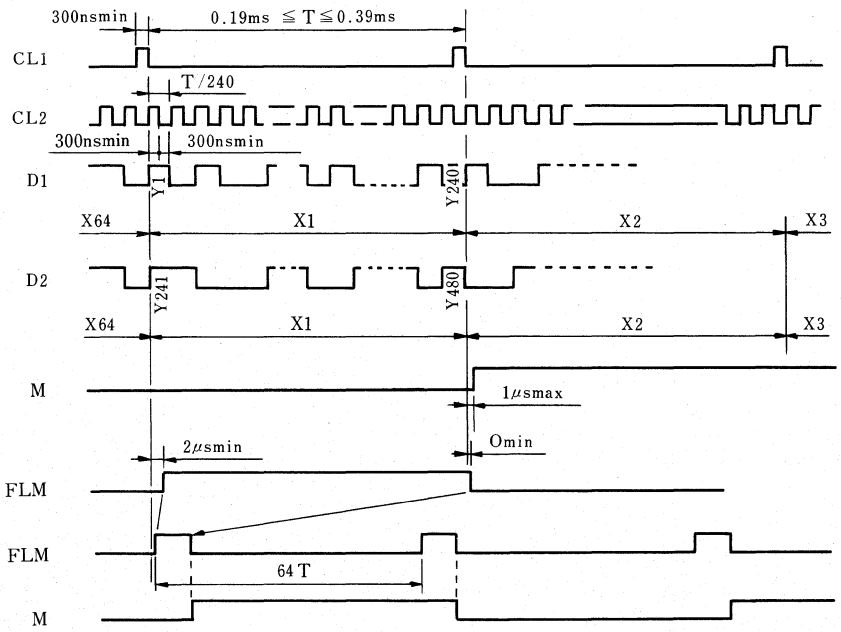


Fig. 5 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
Clock frequency	f_{CL2}	–	–	1200	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	300	–	–	ns
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	300	–	–	ns
Data set up time	t_{SU}	200	–	–	ns
FLM set up time	t_{FSU}	200	–	–	ns
M delay time	t_{DM}	–1000	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	200	–	–	ns

Note 1. Optimum frequency for the highest contrast is different by the type of module.
Note 2. Timing of M signal to CL1 may be in the range of ±1000 ns.
Note 3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

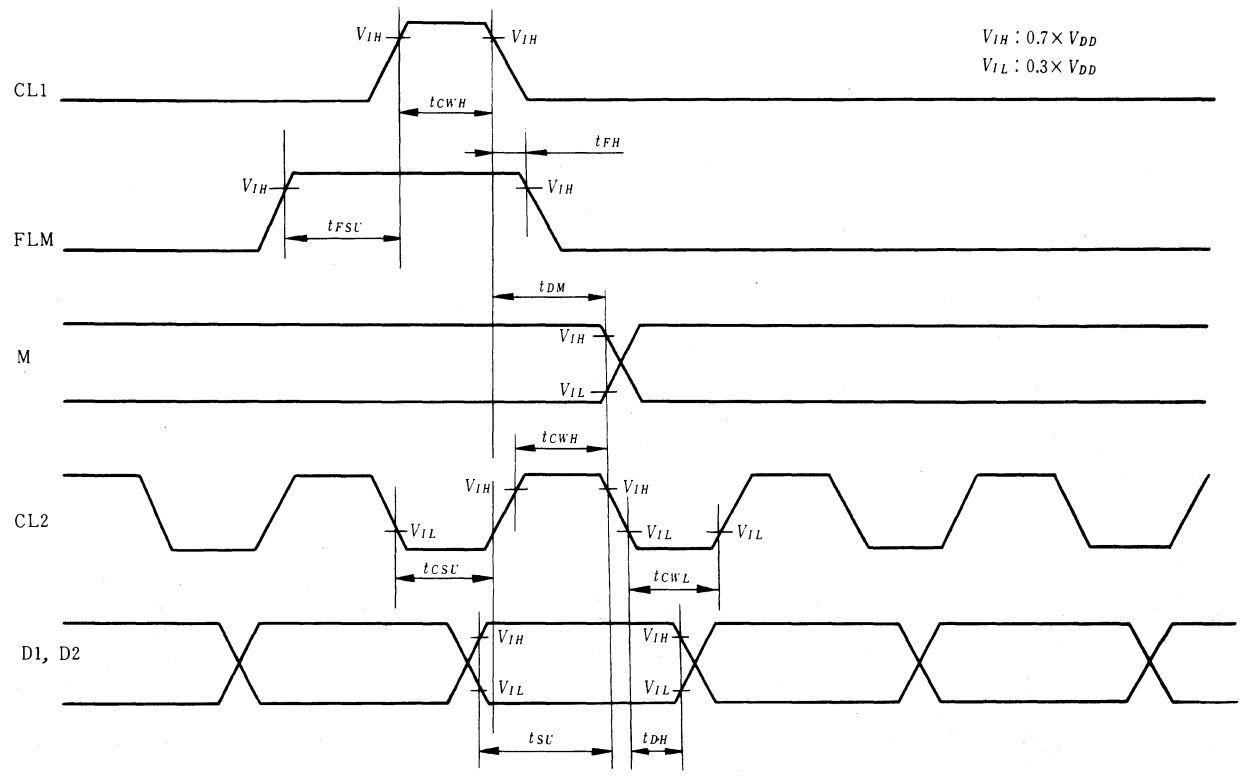


Fig. 6 Interface timing