LM212

- 640 dot(W) x 48 dot(H) graphic and alpha-numeric display
- Recommendable control LSI HD61830 type (see page 76)

OPTICAL DATA . . . . . See page 8

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 63H x 13.5D (max.) mm
Effective display area . . . . . 241W x 25H mm
Number of dots . . . . . 640W x 48H dot
Dot size . . . . . 0.32W x 0.38H mm
Pitch . . . . . 0.37W x 0.43H mm
Weight . . . . . about 175 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −10.0V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 0.7 x V_{DD} V min.
Input "low" voltage (Vi_L) . . . . . 0.3 x V_{DD} V max.
Clock frequency (f_{CL2}) . . . . . 1,075 kHz min.
1,152 kHz typ.
1,228 kHz max.
Power supply current (I_{DD}) . . . . . 10 mA typ.
(D_1, D_2 = GND, f_{CL2} = 1,152 kHz)
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Du=1/48
at Ta = 0°C . . . . . 12.5 V typ.
at Ta = 25°C . . . . . 11.0 V typ.
at Ta = 40°C . . . . . 9.7 V typ.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

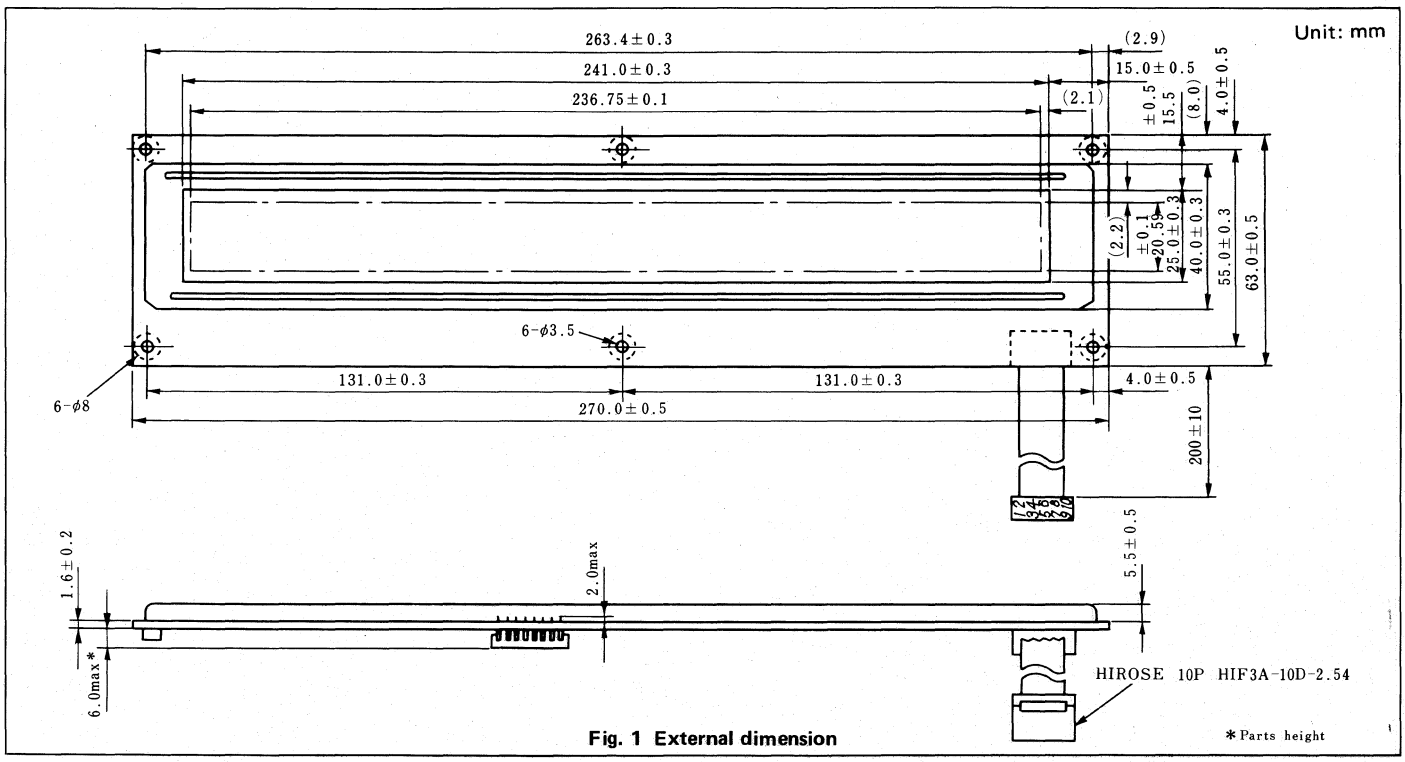


Fig. 1 External dimension

HITACHI

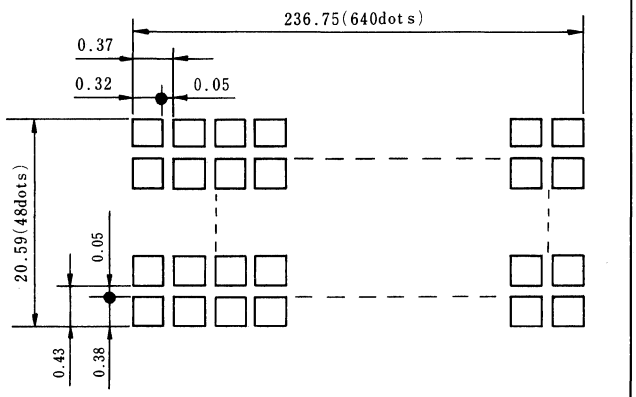


Fig. 2 Display pattern

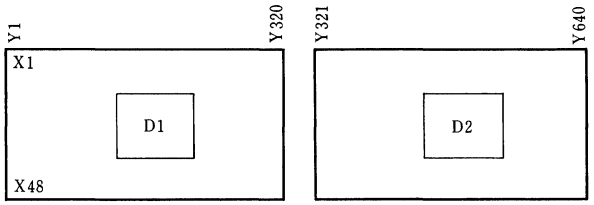
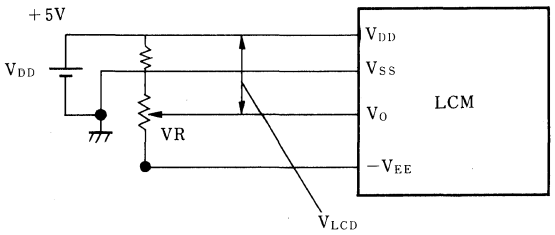
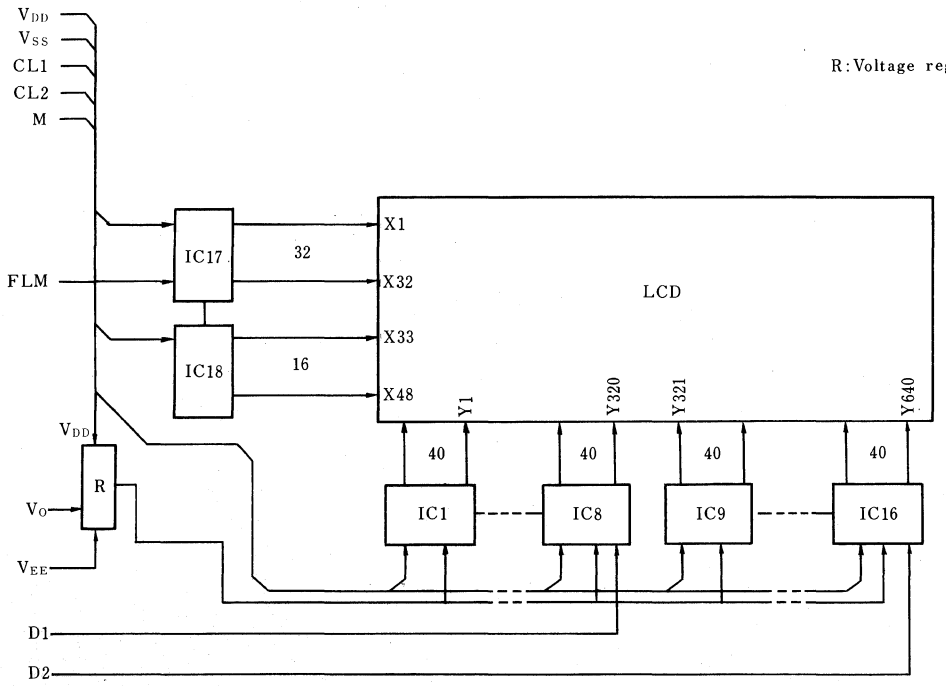


Fig. 3 Comparison of display and data



VLCD: Operating voltage for LC driving

Fig. 4 Power supply



R: Voltage regulator

Fig. 5 Block diagram

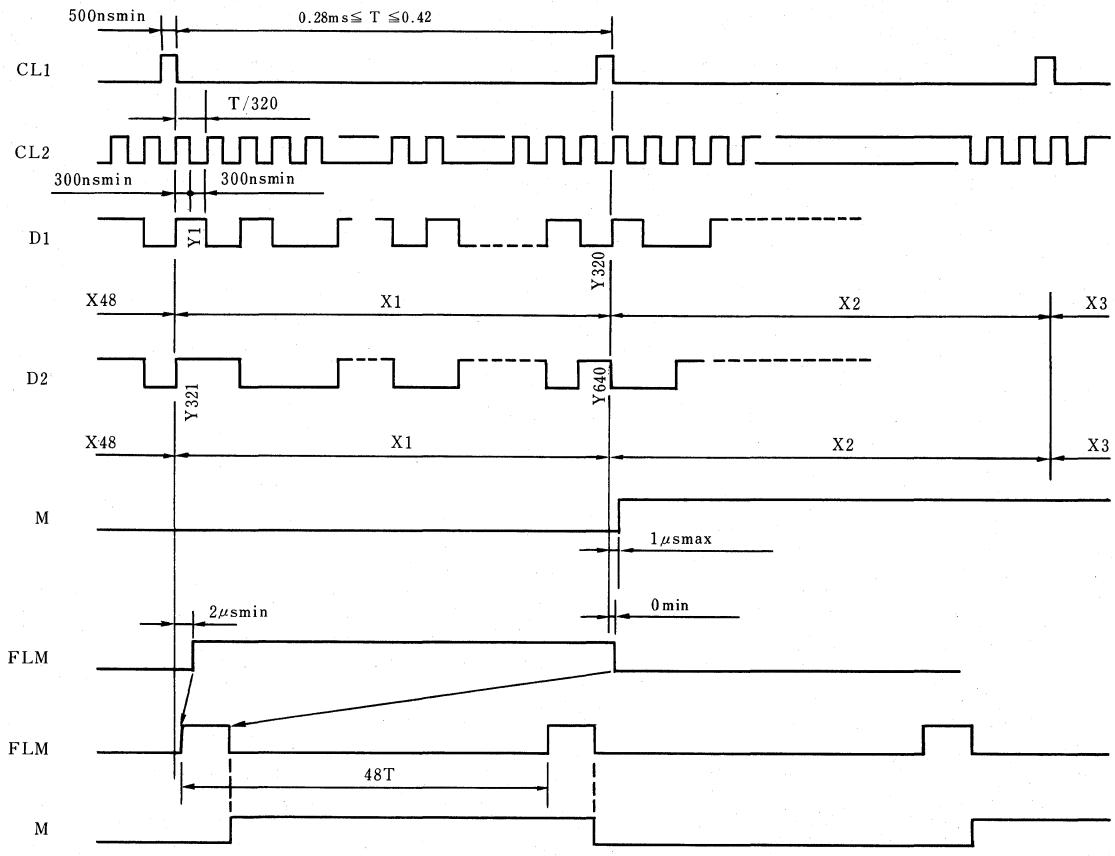


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
Clock frequency	f_{CL2}	–	–	1228	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	200	–	–	ns
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	40	–	–	ns
FLM set up time	t_{FSU}	100	–	–	ns
M delay time	t_{DM}	−1000	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	800	–	–	ns
Data hold time	t_{DH}	400	–	–	ns

Note 1. Optimum frequency for the highest contrast is different by the type of module.
Note 2. Timing of M signal to CL1 may be in the range of ± 1000 ns.
Note 3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ± 2 Hz or 60 Hz ± 2 Hz) to prevent LCD flicker.

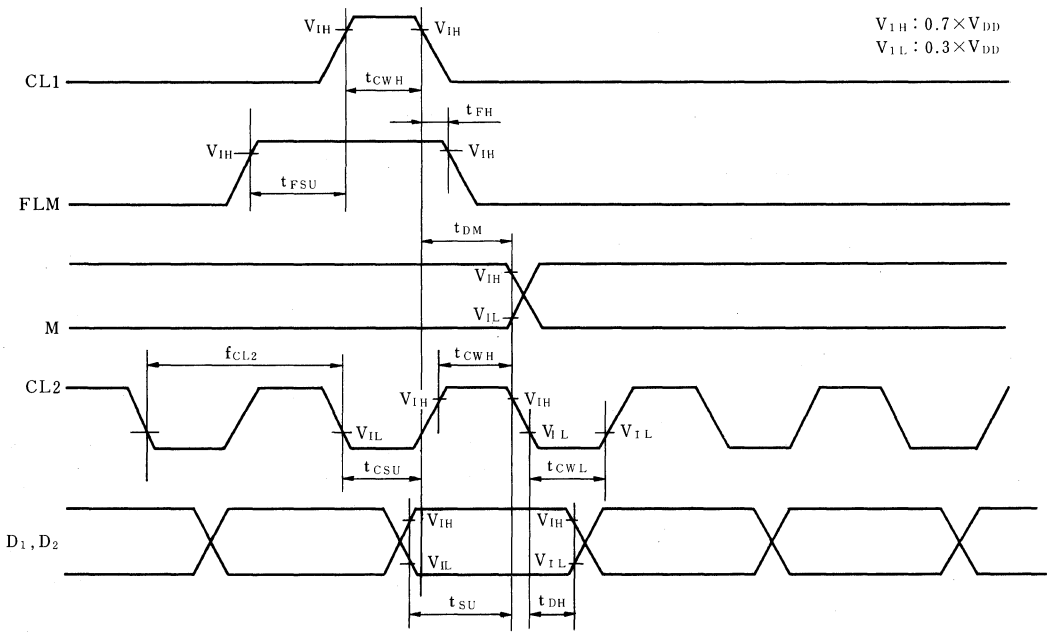


Fig. 7 Interface timing