National Semiconductor

LM21305

PRELIMINARY
June 8, 2010

5A Adjustable Frequency Synchronous Buck Regulator

General Description

The LM21305 is a full featured adjustable frequency synchronous buck regulator capable of delivering up to 5A of continuous output current. The device is optimized to work over the input voltage range of 3V to 18V making it suitable for wide variety of applications. The LM21305 provides 1% output-voltage accuracy and excellent line and fast load transient response for digital loads. The device offers flexible system configuration via programmable switching frequency and ability to synchronize switching frequency. The device also provides internal soft-start to limit in-rush current, cycle-by-cycle current limiting, and thermal shutdown.

The device features internal over voltage protection (OVP) and over current protection (OCP) circuits for increased system reliability. A precision enable pin and integrated UVLO allows the turn-on of the device to be tightly controlled and sequenced. Start-up inrush currents are limited by an internal Soft-Start circuit. Fault detection and supply sequencing are possible with the integrated power good circuit.

The frequency of this device can be adjusted from 300 kHz to 1.5 MHz through an external resistor. The LM21305 is offered in a 28-pin LLP package.

Key Specifications

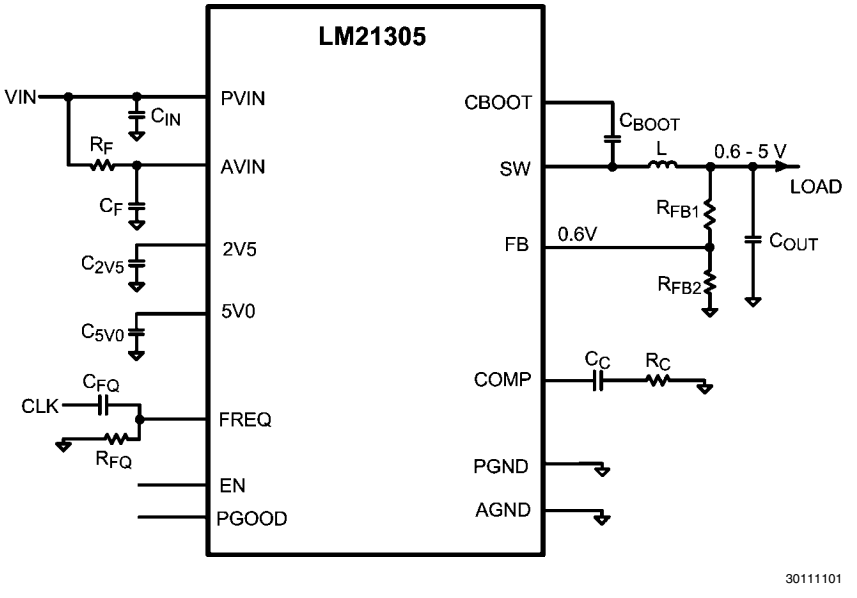
Features

- Single rail input voltage from 3V to 18V
- Feedback Voltage of 0.6V
- 1% typical output voltage accuracy
- High-efficiency switcher core
- Switching frequency range: 300 kHz to 1.5 MHz
- Resistor programmable switching frequency
- Ability to synchronize switching frequency
- Precision enable
- Internal soft-start to reduce in-rush current
- PGOOD function
- Under Voltage Lock Out (UVLO)
- Over Voltage Protection (OVP)
- Fast transient response
- Cycle-by-cycle current limiting
- Thermal shutdown
- LLP-28 package (5mm x 5mm x 0.8mm, 0.5mm pitch)

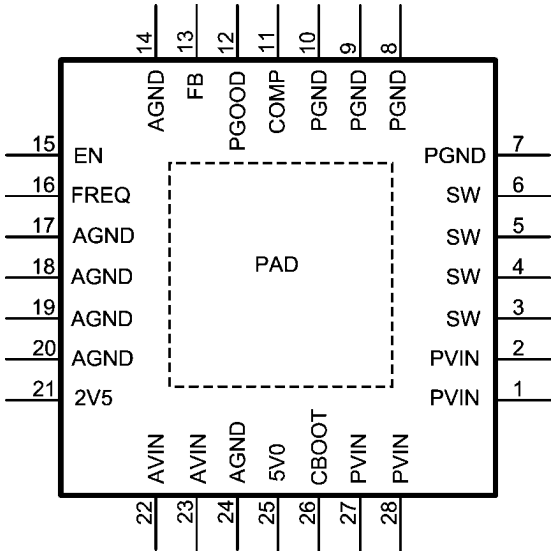
Applications

- Point of Load regulation from 3.3V, 5V, and 12V rails
- Power supply for DSPs, FPGAs, ASICs and Processors
- Broadband, Networking and Optical Communications Infrastructure

Typical Application Circuit



Connection Diagram



LLP-28 Package, Exposed Pad
NS Package Number SQA28B

Order Information

Order Number	NSC Package Drawing	Package Marking	Supplied As
LM21305SQ	SQA28B	21305SQ	1000 units, tape & reel
LM21305SQX			4500 units, tape & reel

Pin Descriptions

Number	Name	Type	Pad Description
1,2,27,28	PVIN	P	Input voltage to the power switches inside the device and delivers power to the output.
3,4,5,6	SW	P	Switch node output of the power switches, voltage swings from PVIN to GND on this pin, also delivers current to the external inductor.
7,8,9,10	PGND	G	Power ground for the internal power switches.
11	COMP	A	Compensation pin to connect to external compensation network.
12	PGOOD	OD	Power Good, open drain output. If high, indicates the output voltage is regulated within tolerance. A pull-up resistor (10 kΩ to 100 kΩ) is recommended for most applications.
13	FB	A	Voltage Feedback pin. This pin can be connected to the output voltage directly or through a resistor divider to set the output voltage range. Range of FB pin voltage is 0.6V to 1.0V.
14,17,18,19,20,24	AGND	G	Analog ground for the internal bias circuitry.
15	EN	I	Precision enable pin. An external divider can be used to set the device turn-on threshold. If not used, the EN pin should be connected to AVIN.
16	FREQ/SYNC	A	Frequency setting pin. This pin can be connected to a resistor to ground to set the internal oscillator frequency. It also can be connected to a external clock source via a capacitor, so that the switching action of the device is synchronized to the external clock.
21	2V5	P	2.5V output of internal regulator. This pin is only for bypass the internal LDO. Loading this pin is not recommended.

Number	Name	Type	Pad Description
22,23	AVIN	P	Analog power input. It powers the internal 2.5V and 5.0V LDO, which provide bias current and internal driver power. It can be connected to PVIN through a low pass RC filter, or can be supplied by a separate rail.
25	5V0	P	5.0V output of internal regulator. This pin is only for bypass the internal LDO. Loading this pin is not recommended.
26	CBOOT	A	Bootstrap pin to drive the high side switch. A Bootstrap capacitor should be connected between this pin to the SW pin.

P: Power A: Analog I: Digital Input I/O: Digital Input/Output OD: Open Drain G: Ground

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

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PVIN, AVIN, SW, EN, PGOOD to AGND	−0.3V to +20V
CBOOT to AGND	−0.3V to +26V
CBOOT to SW	−0.3V to +5.5V
5V0, FB, COMP, FREQ to AGND	−0.3V to +6V
2V5 to AGND	−0.3V to +3V
AGND to PGND	−0.3V to +0.3V
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	−65°C to 150°C
Maximum Continuous Power Dissipation P_{D-MAX}	Internally limited
Maximum Lead Temperature Lead-free compatible (*Note 3*)	260°C

ESD Ratings

All pins, Human Body Model (HBM)	±2kV
All pins, Machine Model (MM)	±150V
All pins, Charge Model (CDM)	±750V

Operating Ratings

PVIN to PGND, AGND	3V to 18V
AVIN to PGND, AGND	3V to 18V
Junction Temperature	−40°C to 125° C
Ambient Temperature	−40°C to 85°C
Junction-to-Ambient Thermal Resistance θ_{JA}	32.4° C/W

Electrical Characteristics (*Note 7*, *Note 8*)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to +125°C). Unless otherwise specified, $V_{IN} = V_{PVIN} = V_{AVIN}$ = 12V, I_{OUT} = 0 A.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
$V_{FB-default}$	Feedback pin factor-default voltage, registers in default state			0.6		V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 0.1 to 5A		0.02		%/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{PVIN} = 3 to 18V		0.01		%/V
$R_{DS-ON-HS}$	High Side Switch On Resistance			44		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance			22		mΩ
I_{CL-HS}	High Side Switch Current Limit	High side FET		6.5		A
I_{CL-LS}	LS Switch Current Limit	Low side FET		8		A
$I_{NEG-CL-LS}$	LS Switch Negative Current Limit	Low side FET		-3.8		A
I_{SD}		$V_{AVIN} = V_{PVIN}$ = 5V		0.5		µA
		$V_{AVIN} = V_{PVIN}$ = 18V		1		
I_Q	Quiescent current with switcher on, no load, DCM mode	$V_{AVIN} = V_{PVIN}$ = 18V		6.5		mA
I_{FB}	Feedback pin input bias current	V_{FB} = 0.6V		1		nA
Gm	Error Amplifier Transconductance			1592		µΩ
A_{VOL}	Error Amplifier Voltage Gain			445		V/V
V_{IH-OVP}	OVP Tripping Threshold	with respect to V_{FB} nom Output voltage rising		110		%
$V_{HYST-OVP}$	OVP Hysteresis Window	with respect to V_{FB} nom		–4		%
$V_{UVLO-HI-AVIN}$	AVIN UVLO rising threshold			2.88		V
$V_{UVLO-HYS-AVIN}$	AVIN UVLO hysteresis window			415		mV
V_{5V0}	Internal LDO1 output voltage measured at 5V0 pin			4.92		V
$C_{OUT-cap-5V0}$	Recommended C_{OUT} capacitance connected to 5V0 pin	Ceramic capacitor		100		nF
$I_{short-5V0}$	Short circuit current			30		mA

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
V_{2V5}	Internal LDO2 output voltage measured at 2V5 pin			2.47		V
$C_{OUT-cap-2V5}$	Recommended C_{OUT} capacitance connected to 2V5 pin	Ceramic capacitor		100		nF
$I_{short-2V5}$	Short circuit current			45		mA
$VF_{CBOOT-D}$	CBOOT diode forward voltage	Measured between 5V0 and CBOOT @ 10 mA		0.83		V
I_{CBOOT}	CBOOT Leakage Current	V_{CBOOT} = 5.5V, VEN = 5V		3.55		µA
$T_{startup-delay}$	Startup time from EN high to the starting of the internal soft-start (*Note 9*)			160		µs
SS	Internal soft-start (*Note 9*)			1		ms
OSCILLATOR						
$F_{OSC-nom}$	Oscillator Frequency, nominal measured at SW pin		300	750	1500	kHz
$F_{OSC-MAX}$	Maximum Oscillator Frequency measured at SW pin	R_freq = 30 kΩ		1500		kHz
$F_{OSC-MIN}$	Minimum Oscillator Frequency measured at SW pin	R_freq = 169 kΩ		300		kHz
$T_{OFF-MIN}$	Minimum Off Time measured at SW pin	Fs = 1.5 MHz, V_{IN} = 3.3V, V_{FB} = 1V, divider = 5.5		50		ns
T_{ON-MIN}	Minimum On Time measured at SW pin	Fs = 1.5 MHz, divider = 1		65		ns
LOGIC						
V_{IH-EN}	EN Pin Rising Threshold			1.2		V
$V_{HYST-EN}$	EN Pin Hysteresis Window			100		mV
I_{EN-IN}	EN Pin Input Current	VEN = 3.3V				
$V_{IH-UV-PGOOD}$	PGOOD UV Rising Threshold	with respect to V_{FB} nom		94		%
$V_{HYST-UV-PGOOD}$	PGOOD UV Hysteresis Threshold	with respect to V_{FB} nom		–4		%
$I_{OL-PGOOD}$	PGOOD sink current	VOL = 0.2V		2		mA
$I_{OH-PGOOD}$	PGOOD leakage current	VOH = 18V				nA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown			160		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis (*Note 9*)			10		°C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula $P = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. Internal thermal shutdown circuitry protects the device from permanent damage.

Note 3: For detailed soldering specifications, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187). http://www.national.com/an/AN/AN-1187.pdf

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin.

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP} = 125°C$), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.

Note 6: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer standard JEDEC thermal test board or 4LJEDEC is 4" x 3" in size, with a 3 by 3 array of thermal vias. The board has 2 imbedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz./1oz./1oz./2 oz. For LLP, thermal vias are placed between the die attach pad in the 1st. copper layer and 2nd. copper layer. Detailed description of the board can be found in JESD 51-7. Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W. The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{OUT}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note 1187: Leadless Leadframe Package (LLP).

Note 7: All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25°C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

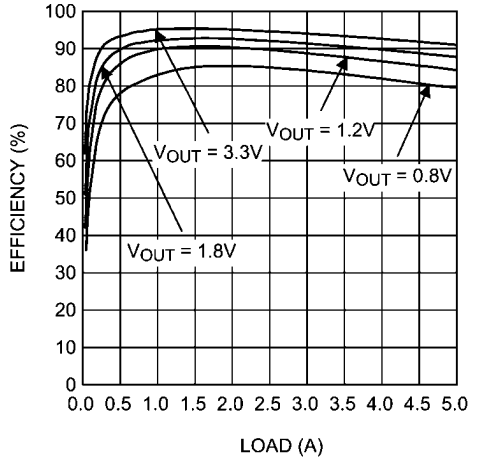
Note 8: Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

Note 9: Guaranteed by design.

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500 kHz, T_A = 25°C.

Efficiency with PVIN = AVIN = 5V, fs = 300 kHz



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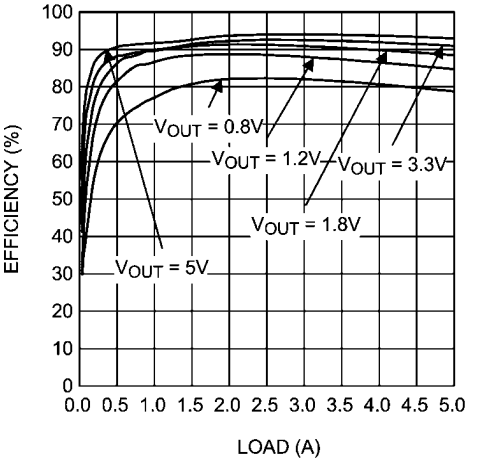
Efficiency with PVIN = 12V, AVIN = 5V, fs = 300 kHz



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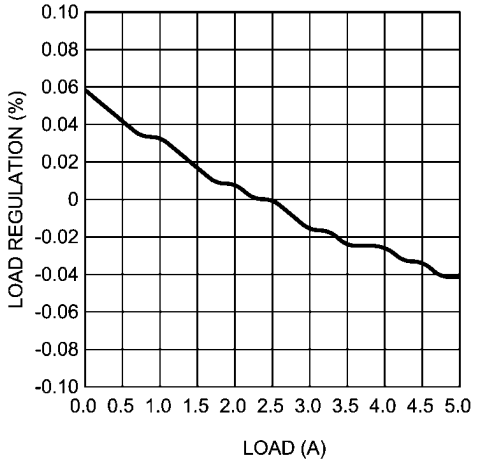
Load Regulation (%)



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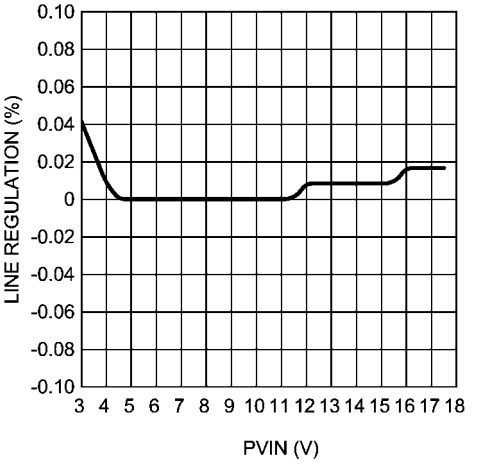
Line Regulation (%)



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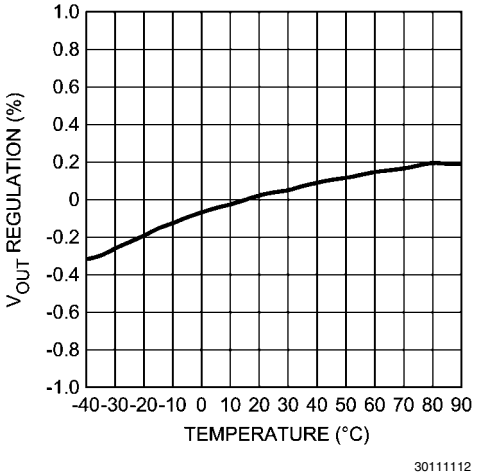
V_{OUT} Regulation (%) vs. Temperature



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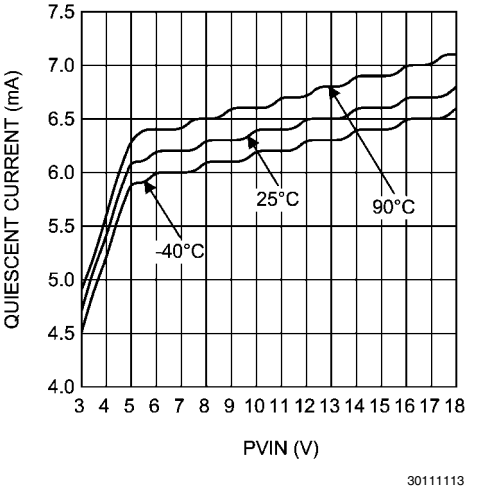
Quiescent Current (mA)



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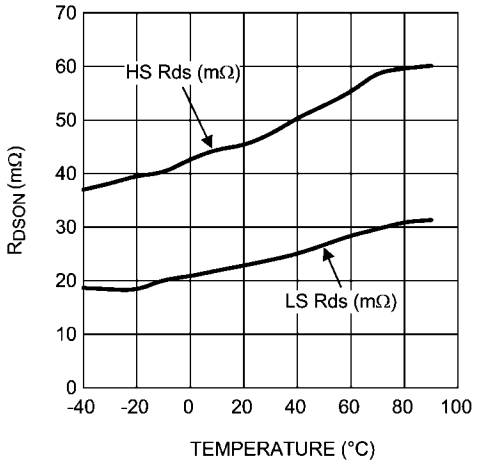
HS and LS MOSFET R_{DS_ON} Over Temperature



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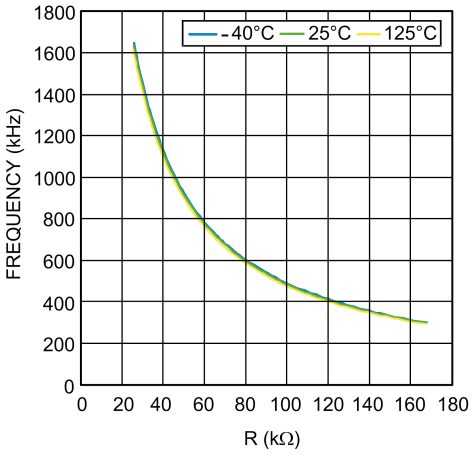
Switching Frequency vs. R_{FRQ}



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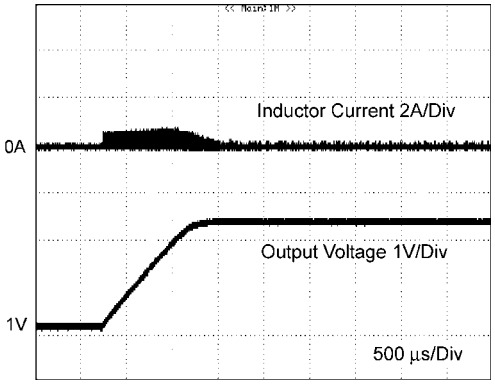
Soft Start with 1V Pre-Bias Voltage, No Load



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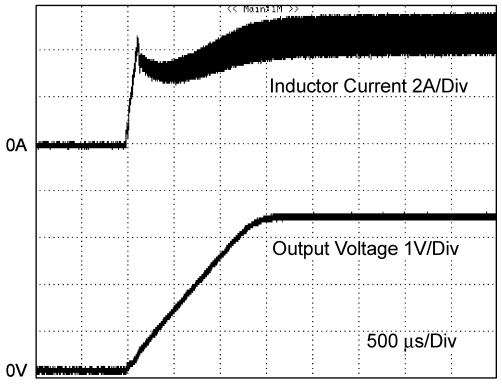
Soft Start with 5A, Load



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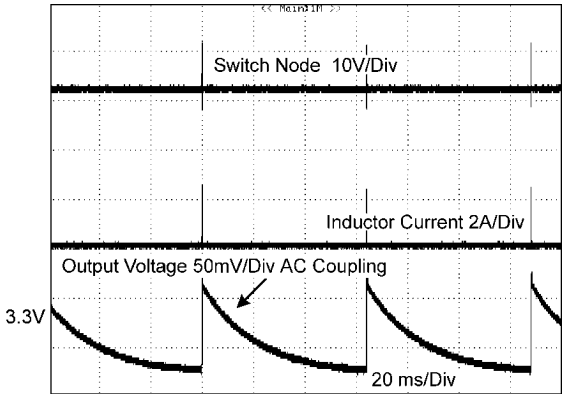
Switching Waveform with 0A, Load (DCM Mode)



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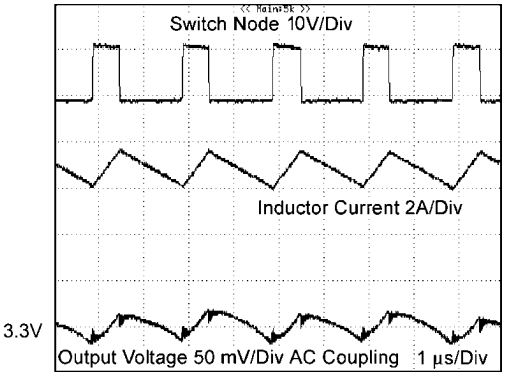
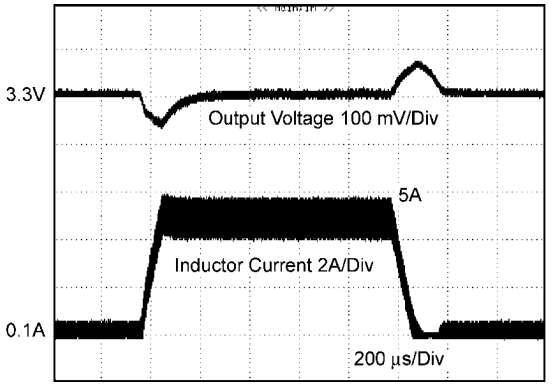
Switching Waveform with 5A, Load



30111194

Load Transient: 0.1A to 5A



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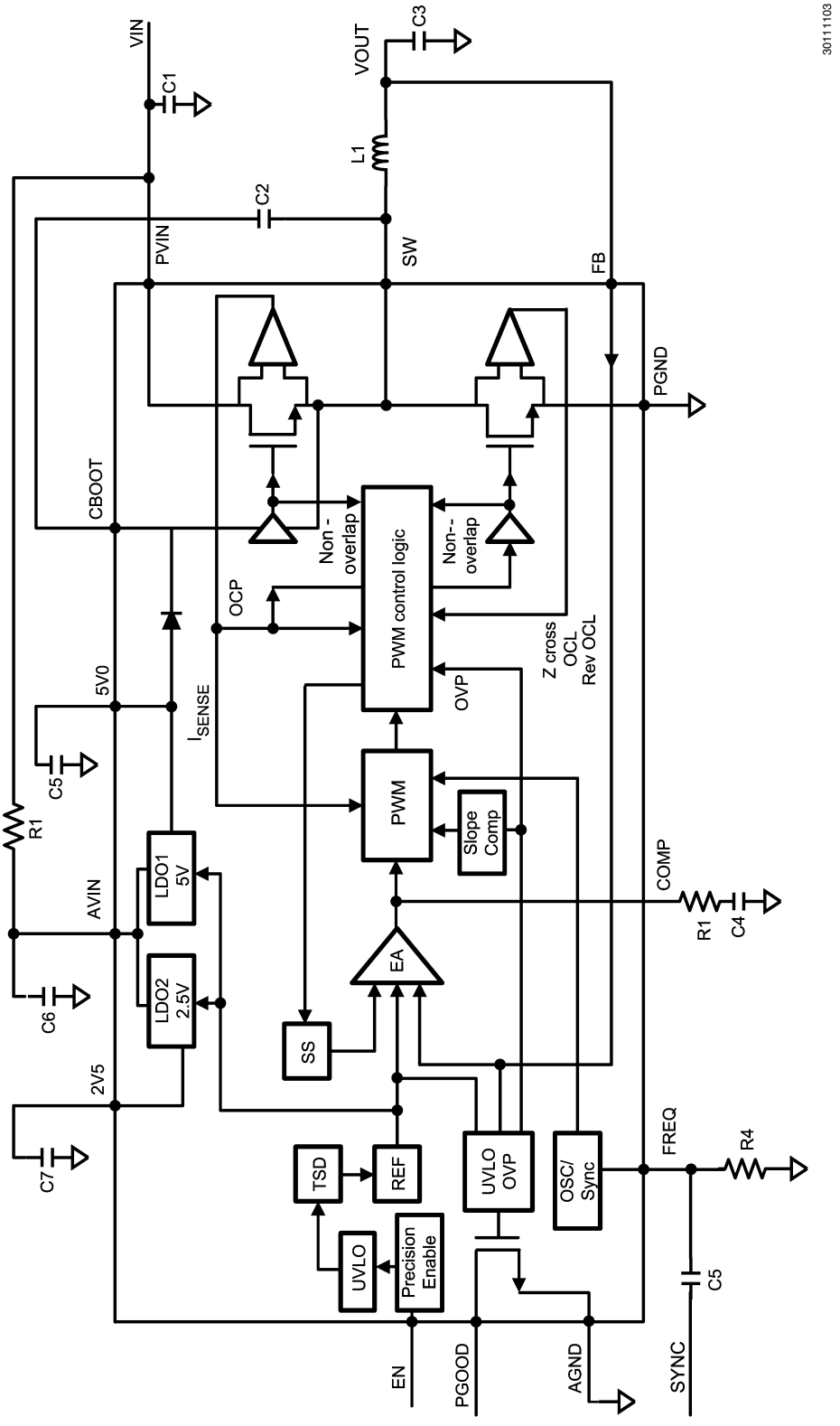
Block Diagram



Operation Description

The LM21305 employs peak current mode control. The 0.6V reference is compared to the feedback signal at the error amp. The PWM modulator block compares the on-time current sense information with the summation of the error amp output (control voltage) and slope compensation. The PWM modulator outputs on/off signals to the high side and low side drivers. Adaptive dead time control is applied to the PWM output such that no shoot through current exists. The drivers then amplify the PWM signals to control the integrated high side and low side MOSFETs.

SWITCHING REGULATOR

The LM21305 employs buck type (step down) architecture. It utilizes many advanced features to achieve excellent voltage regulation and efficiency. This easy to use regulator features two integrated switches and is capable of supplying up to 5A of continuous output current. The regulator utilizes peak current mode control with slope compensation scaled with switching frequency to optimize stability and transient response over the entire output voltage and switching frequency range. Peak current mode control also provides inherent line feed-forward, cycle-by-cycle current limiting and easy loop compensation. The switching frequency can be adjusted between 300 kHz and 1.5 MHz. The device can operate with a small external L-C filter and still provide very low ripple voltage. The precision internal voltage reference allows the output to be set as low as 0.6V. Using an external compensation circuit, the regulator bandwidth can be selected based on the switching frequency to provide fast load transient responses. The switching regulator is specially designed for high efficiency operation throughout the load range. Synchronous rectification yields high efficiency for low voltage and high load current situations, while optional DCM operation extends high efficiency conversion to lower load currents. Fault protection features include: high side and low side switch current limiting, negative current limiting on the low side switch, over voltage protection and thermal shutdown. The device is available in the LLP-28 package featuring an exposed pad to aid thermal dissipation. The LM21305 can be used in numerous applications to efficiently step-down from a wide range of rails: 3V to 18V.

PEAK CURRENT MODE CONTROL

In most applications, the peak current mode control architecture used in the LM21305 only requires two external components to achieve a stable design. The external compensation allows the user to set the crossover frequency and phase margin, thus optimize the transient performance of the device. For duty cycles above 50% all current mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This artificial linear ramp is commonly referred to as slope compensation. The amount of slope compensation in LM21305 will automatically change depending on the switching frequency: higher the switching frequency, larger the slope compensation. This allows smaller inductors to be used with high switching frequency and increase the power density.

SWITCHING FREQUENCY SETTING AND SYNCHRONIZATION

The switching regulator in LM21305 can operate at a frequency ranging from 300 kHz to 1.5 MHz. The switching frequency can be set / controlled by two ways. One is by selecting the external resistor attached to the FREQ pin to set the internal oscillator frequency, which controls the switching frequency. An external 100 pF capacitor CFRQ should also be connected from the FREQ pin to signal ground as a noise filter, as shown in *Figure 1*.

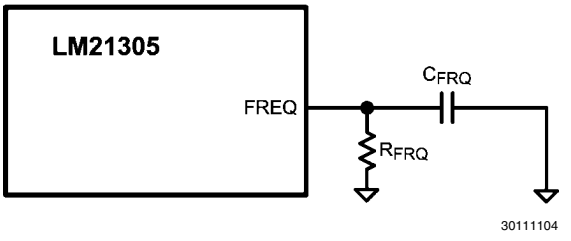


FIGURE 1. Switching Frequency Set by External Resistor

The other way is to synchronize the switching action to an external clock or other fixed frequency signals in the range of 300 kHz to 1.5 MHz. The external clock should be applied through a 100 pF coupling capacitor, CFRQ, as shown in *Figure 2*.

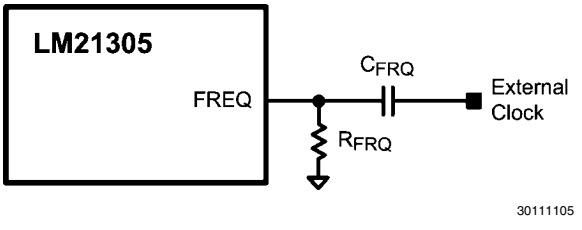


FIGURE 2. Switching Frequency Synchronized to External Clock

Circuits that use an external clock should still have a resistor, connected from the FREQ pin to signal ground. The resistor should be selected to match the external clock frequency. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails and the coupling capacitor on the clock side is grounded or pulled to logic high.

If the external clock fails low, timeout circuits will prevent the high-side FET from staying off for longer than 1.5 times the switching period (Switching period $T_S = 1/f_S$). At the end of this timeout period the regulator will begin to switch at the frequency set by R_{FRQ}.

If the external clock fails high, timeout circuits will again prevent the high-side FET from staying off longer than 1.5 times the switching period. After this timeout period, the internal oscillator takes over and switches at a fixed 1 MHz until the voltage on the FREQ pin has decayed to approximately 0.6V. This decay follows the time constant of C_{SYNC} and R_{FRQ}, and once it is complete the regulator will switch at the frequency set by R_{FRQ}.

LIGHT-LOAD OPERATION

The LM21305 offers increased efficiency at light loads by allowing Discontinuous Conduction Mode (DCM). When the load current is reduced to a point where half of the inductor ripple current is greater than the load current, the device will enter DCM preventing significant negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated by the following equation:

$$I_{BOUNDARY} = \frac{V_{OUT}\,(1 - D)}{2Lf_S}$$

where D is the duty cycle of the high side switch, equaling (high side switch on time / switching period). Please refer to 'Calculating the duty cycle' section under design guide for more details. Several diagrams are shown in *Figure 3* illustrating continuous conduction mode (CCM), Discontinuous Conduction Mode (DCM), and the boundary condition. It can be seen that in DCM, whenever the inductor current reaches zero the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground. At very light loads, usually below 100 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

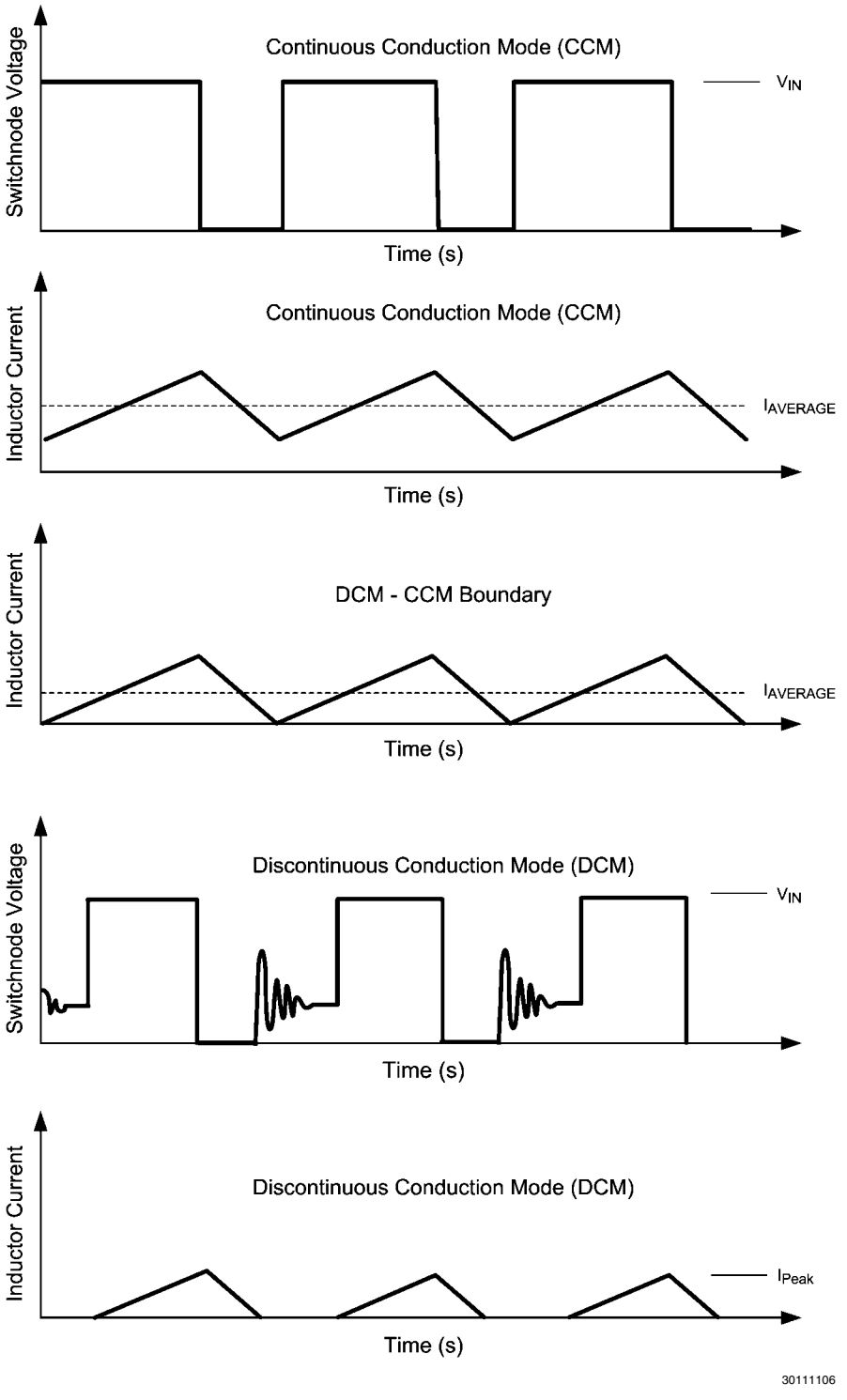


FIGURE 3. CCM and DCM Operation

PRECISION ENABLE

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.2V (typical). The EN pin has 100 mV (typical) of hysteresis and will disable the output when the enable voltage falls below 1.1V (typical). If the EN pin is not used, it should be pulled up to AVIN via a 10 kΩ resistor. Since the enable pin has a precise turn on threshold it can be used along with an external resistor divider network from AVIN to configure the device to turn on at a precise input voltage. The precision enable circuitry will remain active even when the device is disabled. The turn on voltage with a divider can be found by

$$V_{EN\text{-}EXT} = 1.2\left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

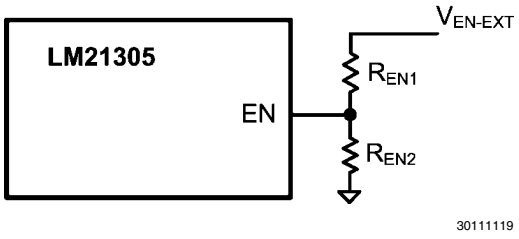


FIGURE 4. Use External Resistor to Set the EN Threshold

DEVICE ENABLE, SOFT START and PRE-BIAS STARTUP CAPABILITY

The device output can be turned off by turning off AVIN or pulling the EN pin low. To enable the device, EN pin must be high with the presence of AVIN and PVIN. Once enabled, the device engages the internal soft start and output voltage goes to its default value. The Soft-Start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling start up current.

Soft start of LM21305 is controlled internally. It typically takes 1ms to finish the soft start sequence. PGOOD will be high after soft start is finished.

The LM21305 is in a pre-biased state when the device starts up with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM21305 is a synchronous converter it will not pull the output low when a prebias condition exists. During start up the LM21305 will be in diode emulation mode with low side switch turned off when zero crossing is detected.

PEAK CURRENT PROTECTION AND NEGATIVE CURRENT LIMITING

The switching regulator in the device detects the peak inductor current and limits it to the value of 6.5A typical. To determine the average current limit from the peak current limit, the inductor size, input and output voltage, and switching frequency must be known. The average current limit can be found by :

$$I_{ave\text{-}limit} = I_{peak\text{-}limit} - \frac{V_{OUT}(1 - D)}{2 \times L \times f_S}$$

When the peak inductor current sensed from the high-side switch reaches the current limit threshold, an over current event is triggered and the internal high-side FET turns off and the low-side FET turns on allowing inductor current to ramp down until the next switching cycle. When the high side over current condition persists, the output voltage will be reduced by the reduced high side switch on time.

In such cases as when short circuit or minimum on time conditions are reached, high side switch current limiting is not sufficient to limit the inductor current. For these conditions, the LM21305 features an additional low-side switch current limit to prevent the current from running away. The low-side switch current limit is set to be higher than the high side current limit, 8A typical. When the low side detects a current higher than the limit event, PWM pulses will be skipped until the low side over current event is not detected. Normal PWM switching occurs afterward. High side and low side current protections result in a current limit that does not aggressively fold back for brief over-current events, while at the same time providing frequency and voltage fold back protection during hard short circuit conditions. The low side switch also has negative current sensing. If the negative current is below the limit, –3A typical, the low side switch will be turned off prematurely. The negative current will be forced to go through the high side switch body diode and will quickly reduce.

PGOOD AND OVER- / UNDER-VOLTAGE HANDLING

The PGOOD pin should be pulled high with an external resistor (10k – 100k recommended). When the FB voltage is within ±10% of the reference voltage, the PGOOD pin will be high. Otherwise, an internal open-drain pull down device will pull the PGOOD pin low.

The LM21305 has built in under and over voltage comparators that control the power switches. Whenever there is an excursion in output voltage above the set OVP threshold, the part will terminate the present on-pulse, turn-on the low-side FET, and pull the PGOOD pin low. The low-side FET will remain on until either the FB voltage falls back into regulation or the inductor current zero cross is detected which in turn tri-states the FETs. If the output reaches the UVP threshold the part will continue switching and the PGOOD pin will be asserted and go low. (To avoid false tripping during transient glitches the PGOOD pin has 16 µs of built in deglitch time to both rising and falling edges.)

UVLO

The LM21305 has a built-in under-voltage lockout (UVLO) protection circuit that keeps the device from switching until the AVIN voltage reaches 2.88V (typical). The UVLO threshold has 100 mV of hysteresis that keeps the device from responding to power-on glitches during start up.

INTERNAL REGULATORS

LM21305 contains two internal low dropout (LDO) regulators to produce internal driving voltages from AVIN. One produces 5V to power the internal drivers. The other produces 2.5V to power the internal bias circuitry. Both LDOs should be bypassed to ground through 5V0 pin and 2V5 pin with an external ceramic capacitor (0.1 µF recommended). Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to 5V0 or 2V5 pin is not recommended since it will degrade their driving capability to the internal circuitry, further push the LDOs into their RMS current ratings and increas power dissipation and die temperature.

The internal MOSFET drivers are powered by an internal LDO (5V0) stepped down from AVIN. LM21305 allows AVIN to be as low as 3V which makes voltage at 5V0 LDO lower than 5V. Low supply voltage at the MOSFET drivers can increase on-time resistance of HS and LS MOSFETs and reduce efficiency of the regulator. When AVIN is between 3V to 5V, the best practice is to short the 5V0 pin to AVIN to bypass the voltage loss on the internal LDO. However, the device can be damaged if the 5V0 pin is pulled to a voltage higher than 5.5V. For efficiency consideration, it would be the best to use AVIN = 5V if possible. When AVIN is above 5V, reduced efficiency can be observed at light load due to the power loss on the LDOs. When AVIN is close to 3V, increased MOSFET on-time resistance can reduce efficiency at large load.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, T_{ON-MIN}, is the smallest duration of time in which the high side MOSFET can be on. This time is typically 70 ns in LM21305. In CCM operation, the minimum on-time limit imposes a minimum duty cycle of

$$D_{MIN} = f_S \times T_{ON-MIN}$$

And thus limit the maximum allowed PVIN with a given V_{OUT}. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. With given switching frequency and desired output voltage, the maximum allowed PVIN can be approximated by

$$V_{PVIN-max} = \frac{V_{OUT}}{f_S} \times \frac{1}{T_{ON-MIN}}$$

Similarly, if the input rail is given, the maximum switching frequency without imposing minimum on-time can be found by:

$$f_{s-max} = \frac{V_{OUT}}{V_{PVIN-max}} \times \frac{1}{T_{ON-MIN}}$$

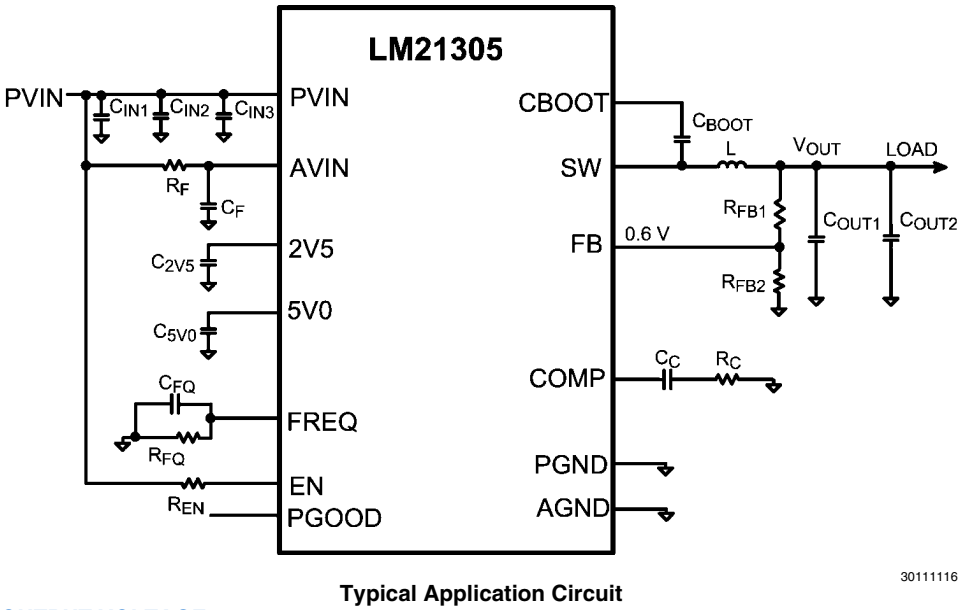
In rare cases the minimum duty cycle can be surpassed; the regulator will automatically skip cycles to keep V_{OUT} regulated, similar to light-load DCM operation.

THERMAL PROTECTION

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the LM21305 tri-states the power FETs and resets soft start. After the junction cools to approximately 150°C, the part starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating

Design Guide

This section walks the designer through the steps necessary to select the external components to build a fully functional efficient step-down power supply. As with any DC-DC converter, numerous tradeoffs are possible to optimize the design for efficiency, size, and performance. These will be taken into account and highlighted throughout this discussion. To facilitate component selection discussions the Typical Application Circuit shown below may be used as a reference. Unless otherwise indicated all formulas assume units of amps (A) for current, farads (F) for capacitance, henries (H) for inductance, volts (V) for voltages and Hertz (Hz) for frequencies.



Typical Application Circuit

SETTING THE OUTPUT VOLTAGE

The FB pin of the LM21305 can be connected to V_{OUT} directly or through a resistor divider. With an external resistor divider, the output voltage can be scaled up from the 0.6V FB voltage. *Figure 5* shows the connection of the divider and the FB pin.

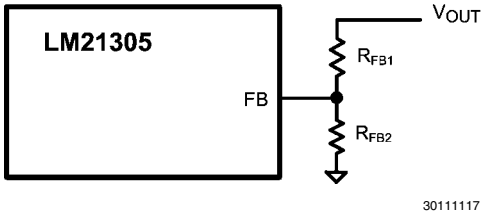


FIGURE 5. Setting the Output Voltage by Resistor Divider

The output voltage can be found by:

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times 0.6V$$

For example, if the desired output voltage is 1.2V, R_{FB1} = 10 kΩ, R_{FB1} = 10 kΩ can be used.

CALCULATING THE DUTY CYCLE

The first equation to calculate for any buck converter is duty cycle. In an ideal (no loss) buck converter, the ideal duty cycle can be found by:

$$D_{ideal} = \left(\frac{V_{OUT}}{V_{PVIN}}\right)$$

In an application with low output voltage (<1.2V) and high load current (> 3A), the losses should not be Ignored when calculation the duty cycle. Considering the effect of the conduction losses associated with the MOSFETs and inductor, the duty cycle can be approximated by:

$$D = \frac{V_{OUT} + R_{dson\text{-}LS} \times I_{OUT}}{V_{PVIN} + R_{dson\text{-}LS} \times I_{OUT} - R_{dson\text{-}HS} \times I_{OUT} - DCR \times I_{OUT}}$$

$R_{dson\text{-}HS}$ and $R_{dson\text{-}LS}$ are the on-time parasitic resistances of the high side and low side MOSFETs, respectively. DCR is the equivalent resistance of the inductor used in the power filter. Other parasitics, such as trace resistance, can be added to DCR if desired. Iout is the load current. It is also equal to the average inductor current. The duty cycle will increase slightly with the increase of load current.

SUPPLY POWER AND INPUT CAPACITORS

PVIN is the supply voltage for the switcher power stage. It is the supply that delivers the output power. The input capacitors on PVIN supplies the large AC switching current drawn by the switching action of the internal MOSFETs. The input current

of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle this current. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS\_CIN} = I_{OUT}\sqrt{\frac{V_{OUT}\,(V_{PVIN} - V_{OUT})}{V_{PVIN}}}\ (A)$$

The power dissipation in the input capacitor is given by: $P_{D\_CIN} = I^2_{RMS\_CINRSER\_CIN}$ (W) where RESR_CIN is the ESR of the input capacitor. This formula has a maximum at PVIN = $2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. A 0.1 µF or a 1µF ceramic bypass capacitor is also recommended to be placed right between the PVIN and PGND pins.

Please refer to the layout recommendation section.

AVIN FILTER

An RC filter should be added to prevent any switching noise on PVIN from interfering with the internal analog circuitry connected to AVIN. These can be seen on the schematic as components RF and CF. There is a practical limit to the size of the resistor RF as the AVIN pin will draw a short 60 mA burst of current during startup, and if RF is too large the resulting voltage drop can trigger the UVLO comparator. A recommended 1µF CF capacitor coupled with the 1Ω resistor provides roughly 16 dB of attenuation at the 1MHz switching frequency.

SWITCHING FREQUENCY SELECTION

LM21305 supports a wide range of switching frequencies: 300 kHz to 1.5 MHz. The choice of switching frequency is usually a compromise between efficiency and size of the circuit. Lower switching frequency usually means lower switching losses (including gate charge losses, transition IV loss etc.) and would result in a better efficiency most of the time. But higher switching frequency allows using smaller LC filters (more compact design). Smaller L also helps transient response and reduces the conduction loss by smaller DCR. The best switching frequency for efficiency needs to be determined case by case. It is related to the input voltage, the output voltage, the most frequent load level, external component choices, and circuit size requirement. The choice of switching frequency is also limited if an operation condition is possible to trigger T_{ON_MIN} and T_{OFF_MIN}. Please refer to the minimum on time consideration section.

The following equation or figure should be used to calculate the resistor value in order to obtain a desired frequency of operation:

$F[kHz] = 31000 \times R^{-0.9}[k\Omega]$.

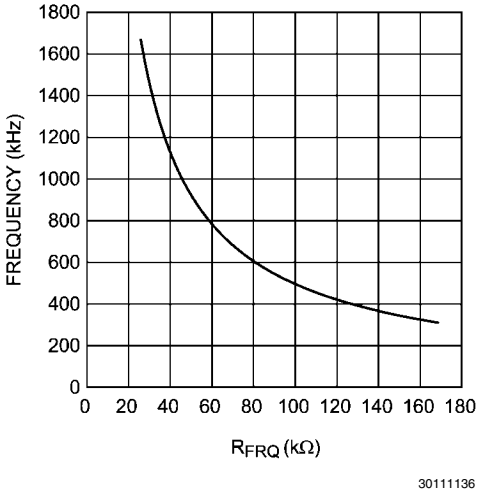


FIGURE 6. External Resistor Selection to Set the Switching Frequency

INDUCTOR

A general recommendation for the inductor in the LM21305 application is keeping a peak-to-peak ripple current between 20% and 40% of the maximum DC load current (5A). It also should have a high enough current rating and DCR as small as possible.

The peak-to-peak current ripple can be calculated by:

$$\Delta i_{Lp\text{-}p} = \frac{(1 - D) \times V_{OUT}}{f_S \times L} \approx \frac{V_{OUT}}{f_S \times L}\left(1 - \frac{V_{OUT}}{V_{PVIN}}\right)$$

The current ripple is larger with smaller inductance and/or lower switching frequency. In general, with a fixed V_{OUT}, the higher the PVIN, the higher the inductor current ripple. If PVIN is kept constant, the higher the V_{OUT}, the higher the inductor current ripple, as long as , otherwise, ripple will decrease with V_{OUT} increase. It is recommended to choose L such that:

$$\frac{(1-D)\times V_{OUT}}{f_S \times 0.4 \times I_{L(MAX)}} \le L \le \frac{(1-D)\times V_{OUT}}{f_S \times 0.2 \times I_{L(MAX)}}$$

The inductor should be rated to handle the maximum load current plus the ripple current:

$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)}/2$

An inductor with saturation current higher than the over current protection limit is a safe choice. It is desired to have small inductance in switching power supplies, because it usually means faster transient response, smaller DCR, and smaller size for more compact design. But too small inductance will generate too large inductor current ripple and it could falsely trigger over current protection at the maximum load. It also generates more conduction loss, since the RMS current is higher comparing to smaller ripple with the same DC current. Larger inductor current ripple generates larger output voltage ripple with the same output capacitors as well. With peak current mode control, it is not recommended to have too small inductor current ripple either, so that the peak current comparator has enough signal-to-noise ratio.

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses on DCR will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. The ‘hard’ saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

OUTPUT CAPACITOR

The device is designed to be used with a wide variety of LC filters. While it is generally desired to use as little output capacitance as possible to keep costs and size down. The output capacitors C_{OUT} should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during a load transient.

The output voltage ripple is composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors: $\Delta V_{OUT\text{-}ESR} = \Delta i_{Lp\text{-}p} * ESR$.

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \frac{\Delta i_{Lp\text{-}p}}{8 f_S C_{OUT}}$$

Figure 7 shows an illustration of two ripple components. Since the two components in the ripples are not in phase, the actual peak-to-peak ripple is smaller than the sum of the two peaks:

$$\Delta V_{OUT} < \Delta i_{Lp\text{-}p} \times \left(\frac{1}{8 f_S C_{OUT}} + ESR\right)$$

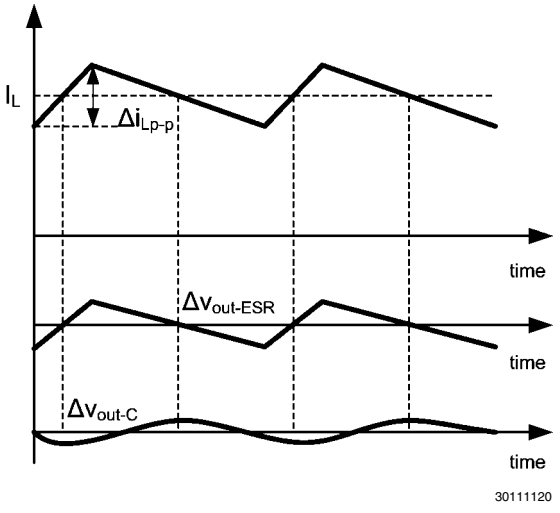


FIGURE 7. Two Components of V_{OUT} Ripple

Output capacitance is usually limited by transient performance if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load transient happens, output capacitors provide the charge before the inductor current catches up. The initial step is equal to the load current step multiplied by the ESR. V_{OUT} continues to droop until the control loop response increases or decreases the inductor current to supply the load. To maintain a small over- or undershoot during transient, small ESR and large capacitance are desired. But these also come with higher cost and size. The control loop should also be fast to reduce the voltage droop.

One or more ceramic capacitors are recommended because they have very low ESR and remain capacitive up to high frequencies. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. Other types of capacitors also can be used if large capacitance is needed, such as tantalum, poscap and OSCON. Such capacitors have lower $1/(2\pi ESR * C)$ frequency than ceramic capacitors. The lower RC frequency could affect the control loop if it is close to the crossover frequency. If high switching frequency and high crossover frequency are desired, all ceramic design is more appropriate.

EFFICIENCY CONSIDERATIONS

The efficiency of a switching regulator is defined as the output power divided by the input power times 100%. Efficiency also can be found by:

$$\eta = 1 - \frac{\text{Total Power Loss}}{\text{Input Power}}$$

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LM21305 circuits: 1) conduction losses, 2) switching and gate driving losses, 3) biasing losses. Conduction losses are the I^2R losses on parasitic resistances in the path of the output current, including on-time resistances of the internal switches (R_{DS-ON}), equivalent DC resistance of the inductor (DCR) and trace resistances R_{trace}. The conduction loss can be approximate by:

$$W_{cond-loss} = I^2_{OUT} \times (D \times R_{DS-ON-HS} + (1 - D) \times R_{DS-ON-LS} \times R_L + R_{trace})$$

The conduction loss can be reduced by reducing these parasitic resistances. For example, the LM21305 is designed to have low Rds-on internal switches. The inductor DCR should be small. The traces that conduct the current should be wide, thick and as short as possible. The conduction losses affect the efficiency more at heavier load. Switching losses include all the losses generated by the switching action of the two power MOSFETs. Each time the switch node swings from low to high or vice versa, charges are applied or removed from the parasitic capacitance from the SW node to GND. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge moves from 5V0 to ground. Each time a power MOSFET is turned on or off, a transition loss is generated if it is not soft switching. MOSFET parasitic diodes generate reverse recovery loss and dead time conduction loss. RMS currents going through the input and output capacitor ESR generates loss. All of these losses should be evaluated and carefully considered to design a high efficient switching power converter. Since these losses only happen during 'switching', reducing the switching frequency always helps to reduce the switching loss. The improvement is more pronounced at lighter load.

Since 5V0 is an LDO output from AVIN, the current drawn from AVIN is the same as i_{DRIVE} and the loss on AVIN is $V^{AVIN} * i_{drive}$. The other portion of AVIN power loss is the bias current through 2V5, equals to $V^{AVIN} * i_{bias}$. Powering AVIN from a 5V system rail provides the optimal tradeoff between bias power loss and switching loss (R_{DS-ON} loss).

COMPENSATION CIRCUIT

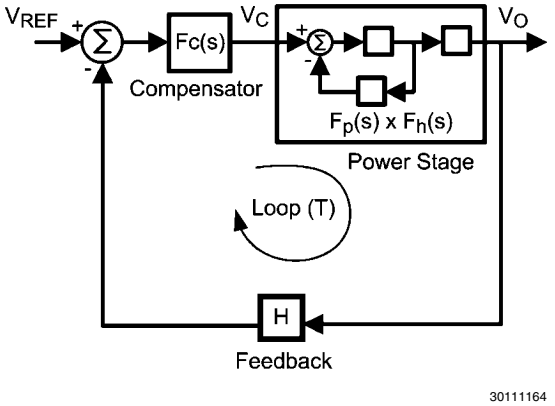


FIGURE 8. Control Block Diagram of a Current Mode Controlled Buck Converter

The LM21305 employs a current mode controller, therefore the control block diagram representation involves 2 feedback loops (see *Figure 8*). The inner feedback loop derives its feedback from the sensed inductor current, while the outer loop monitors the output voltage. This section will not give a rigorous analysis of current mode control, but rather a simplified but accurate method to determine the compensation network. The compensation network is designed around the power components, or the power stage. The compensation components needed by LM21305 are shown in *Figure 8*. The purpose of the compensator block is to stabilize the control loop and achieve high performance in terms of the transient response, audio susceptibility and output impedance. The LM21305 will typically require only a single resistor Rc and capacitor Cc1 for compensation, but depending on the power stage it could require a second capacitor for a high frequency pole.

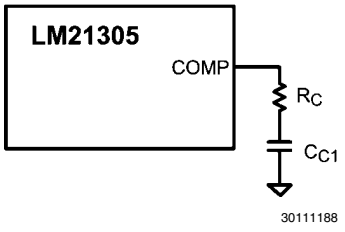


FIGURE 9. Compensation Network for LM21305

The overall loop transfer function is a product of the power stage transfer function, internal amplifier gains and the feedback network transfer function and can be expressed by:

$T = Gain_0 F_p(s) F_h(s) F_{comp}(s)$ where Gain0 includes all the DC gains in the loop, Fp(s) represents the power stage pole and zero (including the inner current loop), Fh(s) represents the sampling effect in such a switch mode converter and Fcomp (s) is the transfer function of the external compensator. shows an asymptote approximation plot of the loop gain.

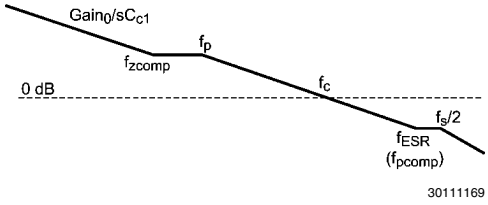


FIGURE 10. Asymptote Approximation of the Loop Gain in LM21305

The loop gain determines both static and dynamic performance of the converter. The power stage response is fixed by the selection of the power components, therefore the compensator is designed around the power stage response to achieve a good loop response. The goal is to design a loop gain with high crossover frequency and adequate phase margin under all operation conditions.

SELECT COMPENSATION COMPONTENTS

To select the compensation components, a desired cross over frequency need to be selected. It is recommended to select fc equal to or lower than 1/8 of the switching frequency. Then effect of Fh(s) can be ignored to simplify the design. The capacitor ESR zero is also assumed to be at least 3 times higher than fc. The compensation resistor can be found by:

$$R_c \approx \frac{1}{Gain_0} \times \frac{f_c}{f_p} = \frac{V_{OUT}}{V_{FB}} \times 197 \times fc \times C_{OUT}$$

Cc1 does not affect the crossover frequency fc, but it sets the compensator zero fzcomp and affects the phase margin of the loop. For a fast design, Cc1 = 10 nF gives adequate performance in most LM21305 applications. Larger Cc1 gives larger phase margin, while the lower Cc1 gives higher gain at lower frequency thus faster transient response. It is recommended to set the compensation zero no higher than fc/3 to ensure enough phase margin, meaning:

$$C_{c1} \geq \frac{3}{2\pi R_c f_c}$$

PLOT THE LOOP GAIN

The complete loop gain can be plotted to include the effect of Fh(s) and ESR zero in a software tool, such as Matlab. The components in the loop gain can by found as follows: The DC gain of the power stage can be found by:

$$Gain_0 = \frac{V_{FB}}{V_{OUT}} \times \frac{R_{OUT}}{1+\frac{R_{OUT}}{f_s L}(mcD' - 0.5)} \times 0.0315$$

where f_s is the switching frequency,

$$m_c = 1 + \frac{4 \times f_S \times L}{V_{IN} - V_{OUT}}$$

and $D' = 1 - D$.

Minimum R_{OUT} should be used in the calculation $R_{OUT} = V_{OUT}/I_{OUT}$.

Fp(s) can be expressed by:

$$F_p(s) = \frac{1 + sC_{OUT} * ESR}{1 + \frac{s}{2\pi f_p}}$$

where the power stage pole considering the slope compensation effect is:

$$f_p = \frac{1}{2\pi C_{OUT}}\left(\frac{1}{R_{OUT}} + \frac{1}{f_s L}(m_c D' - 0.5)\right)$$

The high frequency behavior Fh(s) can be expressed by:

$$F_h(s) = \frac{1}{1 + \frac{s}{w_n Q_p} + \frac{s^2}{w_n^2}}$$

where:

$$w_n = \pi f_s \text{ and } Q_p = \frac{1}{\pi(m_c D' - 0.5)}$$

The loop gain $T = Gain_0 F_p(s) F_h(s) F_{comp}(s)$ can be plotted with above equations and the more accurate crossover frequency and phase margin can be found.

HIGH-FREQUENCY CONSIDERATIONS

Fh(s) represents the additional magnitude and phase drop around fs/2 caused by the switching behavior of the converter. Fh(s) contains a pair of double poles with quality factor Qp at half of the switching frequency. It is a good idea to check that Qp is between 0.15 and 2, ideally around 0.5. If Qp is too high, the resonant peaking at fs/2 could become severe coinciding with subharmonic oscillations in the duty cycle and inductor current. If Qp is too low, the two complex poles split and the converter begins to act like a voltage mode converter and the compensation scheme used above should be changed.

Fp(S) also contains the ESR zero of the output capacitors :

$$f_{ESR} = \frac{1}{2\pi C_{OUT} ESR}$$

In a typical design, f_{ESR} should be at least 3 times higher than the desired crossover frequency fc. If f_{ESR} is lower than fs/2, an additional capacitor Cc2 can be added between the COMP pin to ground to give a high-frequency pole:

$$C_{c2} = \frac{1}{2\pi R_c f_{ESR}}$$

Cc2 should be much smaller than Cc1 to avoid affecting the compensation zero.

CBOOT CAP

A capacitor is needed between the CBOOT pin to the SW node to supply the gate drive charge when the high side is turning ON. The capacitor should be big enough to supply the charge without significant voltage drop. A 0.1 µF capacitor is recommended in the LM21305 application.

5V0 AND 2V5 OUTPUT CAPACITORS

5V0 and 2V5 pins are internal LDO outputs. The two LDOs are used for internal circuits only and should not be loaded.

Output capacitors are needed to stabilize the LDOs. Ceramic capacitors within a specified range should be used to meet stability requirements. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. Use the following table to choose a suitable output capacitor:

	Output Voltage NOMINAL	Output Capacitance Range (Recommended Typical Value)
5V0	5	0.1 µF ± 20%
2V5	2.5	

PCB LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DCDC converter and surrounding circuitry by contributing to EMI, ground bounce, resistive voltage loss in the traces and thermal problems. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability.

Good layout for LM21305 can be implemented by following a few simple design rules.

1. Provide adequate device heat sinking. Use 4-layer board with the copper thickness for the four layers, starting from the top one, 2 oz./1oz./1oz./2 oz. Use at least 3 by 3 array of thermal vias to connect the DAP to the power plane heat sink. The vias should be evenly distributed under the DAP.
2. The input capacitors should be placed as close as possible to the PVIN pins, the inductor should be placed as close as possible to the SW pins and output capacitors. This is to minimize the area of switching current loops and reduce the resistive loss of the high current path. For the LM21305 pinout, a 0.1 uF capacitor can be placed right by pin 1, 2 and pin 7, across the SW node trace, as an addition to the bulk input capacitors. Using a size 1206 capacitor allows enough copper width for the switch node to be routed underneath the capacitor for good conduction (see evaluation board layout).
3. The copper area of the switch node should be thick and short to both provide a good conduction path for the switch node current and minimize radiated EMI. This also requires the inductor be placed as close as possible to the SW pins.
4. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. It is recommended to route the feedback trace on a different layer than the inductor and SW node trace, such that there is a ground plane in between the feedback trace and inductor/SW node trace. This provides further cancelation of EMI on the feedback trace.
5. If voltage accuracy at the load is important, make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops along the traces and provide the best output accuracy. It is better to place the resistor divider closer to the FB node, rather than close to the load.
6. Make input and output power bus connections as wide and short as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Use copper plates on top to connect the multiple PVIN pins together and PGND pins together.
7. The capacitor connecting between the CBOOT pin and SW node should be placed as close as possible to the CBOOT pin.

THERMAL CONSIDERATIONS

The thermal characteristics of the LM21305 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θJA is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship: $T_J = P_D\theta_{JA} + T_A$ where P_D is the power dissipation of the device: $P_D = P_{IN}$ x (1 – Efficiency) – 1.1 * I_{OUT} * DCR, T_J is the junction temperature in °C, P_{IN} is the input power in Watts ($P_{IN} = V_{IN}$ x I_{IN}), θ_{JA} is the junction-to-ambient thermal resistance for the LM21305, T_A is the ambient temperature in °C, I_{OUT} is the output load current, and DCR is the inductor series resistance.

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 160°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs, it is a sign of inadequate heat-sinking or excessive power dissipation in the device. Board heat-sinking can be improved by using more thermal vias, larger board or more layers of the board.

APPLICATION EXAMPLE

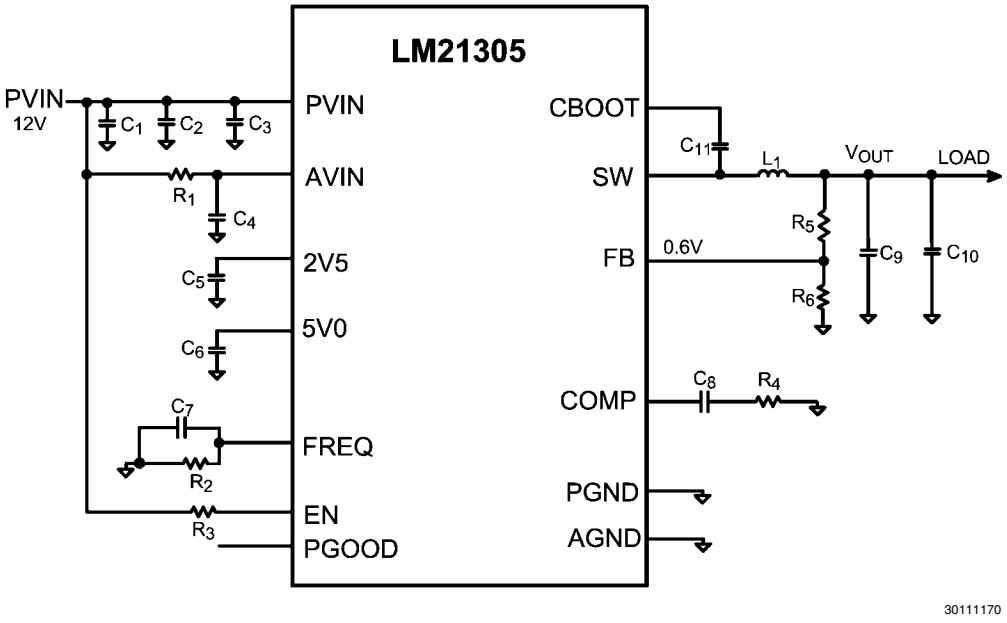
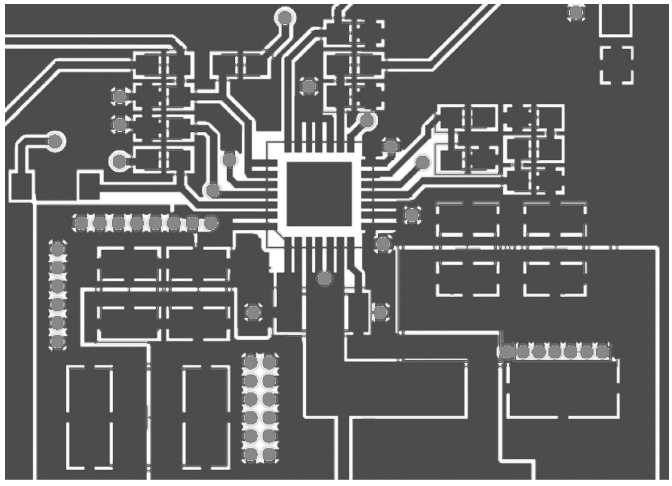


FIGURE 11. Example of Circuit for Application

BILL OF MATERIALS

V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V	Package
C1	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	CASE D
C2	10 µF 50V	10 µF 50V	10 µF 50V	10 µF 50V	10 µF 50V	1210
C3	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1206
C4	1.0 µF 35V	1.0 µF 35V	1.0 µF 35V	1.0 µF 35V	1.0 µF 35V	603
C5,C6,C11	0.1 µF 50V	0.1 µF 50V	0.1 µF 50V	0.1 µF 50V	0.1 µF 50V	603
C7	100 pF 100V	100 pF 100V	100 pF 100V	100 pF 100V	100 pF 100V	603
C8	10000 pF 25V	10000 pF 25V	4700 pF 25V	4700 pF 25V	4700 pF 25V	603
C9, C10	47µF X5R	47µF X5R	47µF X5R	47µF X5R	47µF X5R	1210
L1	1.2 µH	2.2 µH	2.2 µH	3.3 µH 9.0A	3.3 µH	SMD
R1	1Ω 1%	1Ω 1%	1Ω 1%	1Ω 1%	1Ω 1%	603
R2	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	603
R3, R6	10.0 kΩ 1%	10.0 kΩ 1%	10.0 kΩ 1%	10.0 kΩ 1%	10.0 kΩ 1%	603
R4	2.40 kΩ 1%	3.60 kΩ 1%	5.10 kΩ 1%	6.65 kΩ 1%	10.0 kΩ 1%	603
R5	10.0 kΩ 1%	20 kΩ 1%	31.6 kΩ 1%	45.3 kΩ 1%	73.2 kΩ 1%	603

PCB LAYOUT



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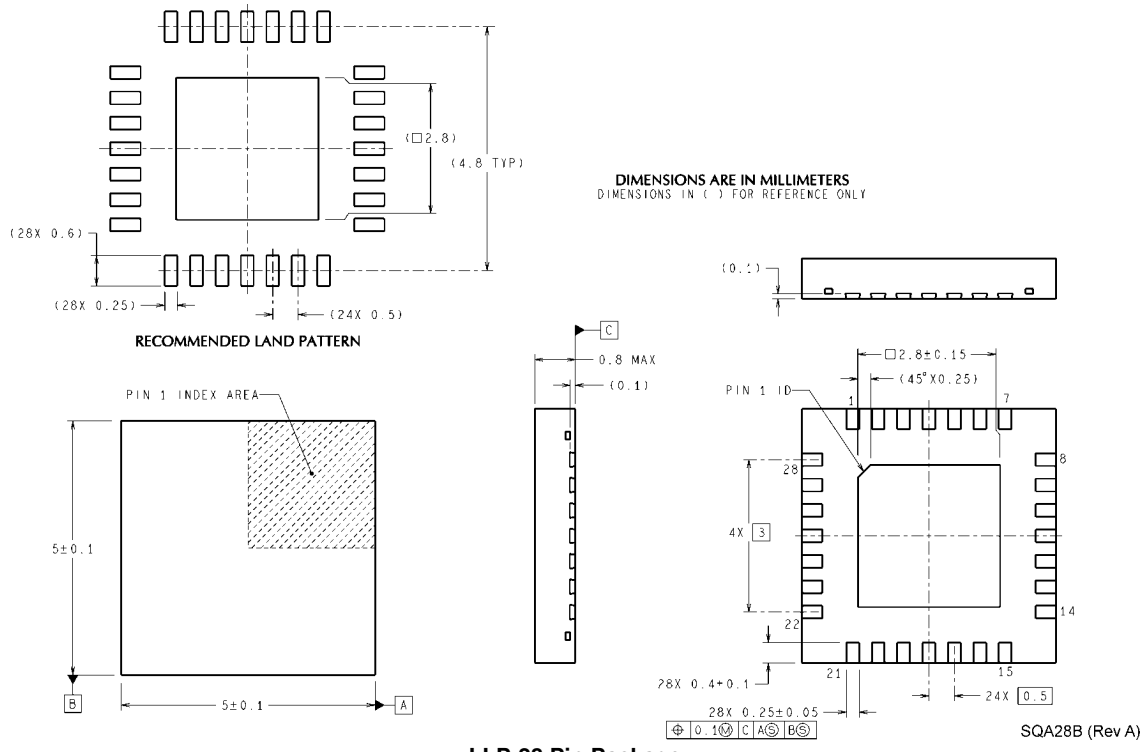
Physical Dimensions inches (millimeters) unless otherwise noted



LLP-28 Pin Package
NS Package Number SQA28B

Notes

Notes

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