SPECIFICATION
FOR
APPROVAL

(●) **Preliminary Specification**
( ) **Final Specification**

Title	23” Full HD TFT LCD

BUYER	
B/A MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LM230WF3
SUFFIX	SJE1

*When you obtain standard approval,
please use the above model name without suffix

SIGNATURE	DATE
/	
/	
/	

Please return 1 copy for your confirmation
With your signature and comments.

APPROVED BY	DATE
REVIEWED BY	
PREPARED BY	

Product Engineering Dept.
LG Display Co., Ltd

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RECORD OF REVISIONS

Revision No	Revision Date	Page	Description
0.0	Jul., 23, 2012	-	First Draft, **Preliminary Specifications**

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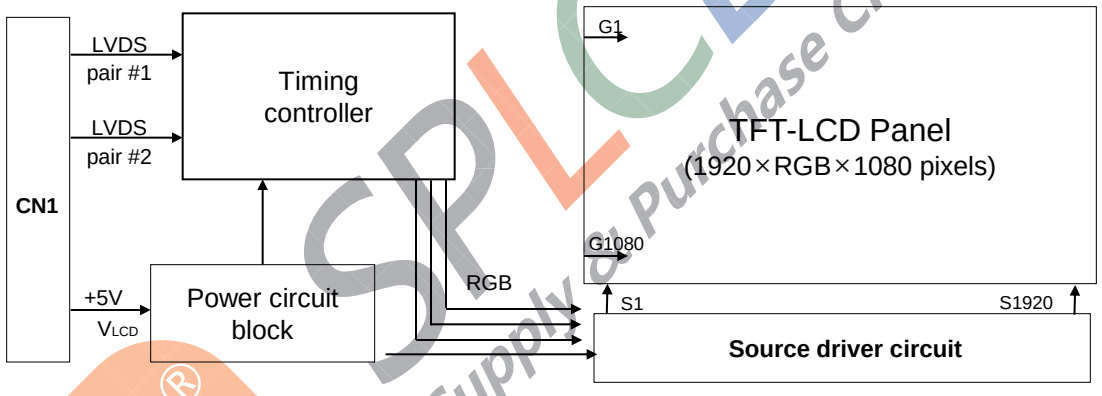
1. General description

LM230WF3-SJE1 is a Color Active Matrix Liquid Crystal Display. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 23.0 inch diagonally measured active display area with Full HD resolution (1080 vertical by 1920 horizontal pixel array) Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16.7M colors with Advanced-FRC(Frame Rate Control). It has been designed to apply the interface method that enables low power, high speed, low EMI. FPD Link or compatible must be used as a LVDS(Low Voltage Differential Signaling) chip. It is intended to support applications where thin thickness, wide viewing angle, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LM230WF3-SJE1 characteristics provide an excellent flat panel display for office automation products such as monitors.

FIG. 1 Block diagram



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General features

Active Screen Size	23 inches(58.42cm) diagonal (Aspect ratio 16:9)
Outline Dimension	526.184(H) x 303.416 X 2.4(D) mm(Typ.)
Pixel Pitch	0.2652(H)mm x 0.2652(V)mm
Pixel Format	1920 hor. By 1080 vert. Pixels RGB stripes arrangement
Interface	LVDS 2Port
Color Depth	16.7M colors (6bit + A-FRC)
Viewing Angle (CR>10)	R/L 178(Typ.), U/D 178(Typ.)
Power Consumption (P_{LCD_TYP})	4.8 Watt @ V_{LCD}
Weight	470 g (typ.)
Display Operating Mode	Transmissive mode, normally Black
Surface Treatment	Hard coating (3H), Glare treatment of the front polarizer

2. Absolute Maximum Ratings

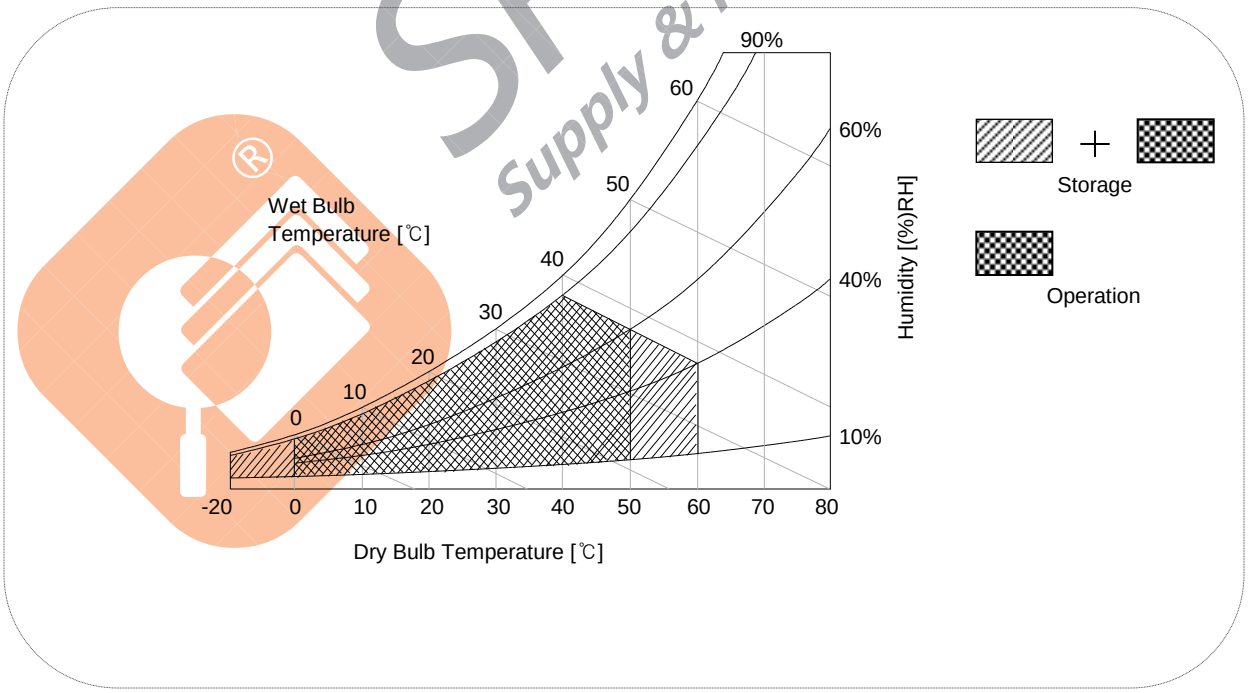
The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. Absolute maximum ratings

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Supply Input Voltage	V_{LCD}	-0.3	+6.0	Vdc	At 25℃
Operating Temperature	T_{OP}	0	50	℃	1
Storage Temperature	T_{ST}	-20	60	℃	
Operating Ambient Humidity	H_{OP}	10	90	%RH	
Storage Humidity	H_{ST}	10	90	%RH	

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C Max, and no condensation of water.
2. Storage condition is guaranteed under packing condition.

FIG. 2 Temperature and relative humidity



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3. Electrical Specifications

3-1. Electrical Characteristics

This model is required to power the LCD electronics and to drive the TFT array and liquid crystal.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol		Values			Unit	Notes
			Min	Typ	Max		
MODULE :							
Power Supply Input Voltage	V_{LCD}		4.5	5.0	5.5	Vdc	
Permissive Power Input Ripple	V_{LCD}		-	-	0.3	V	1
Power Supply Input Current	I_{LCD}	60Hz	-	960	1240	mA	2
		75Hz	-	-	1380	mA	
		60Hz	-	1150	1490	mA	3
		75Hz	-	-	1770	mA	
Power Consumption	P_{LCD_TYP} (@60Hz)		-	4.8	6.2	Watt	2
	P_{LCD_MAX} (@60Hz)		-	5.75	7.45	Watt	3
Inrush current	I_{RUSH}		-	-	3.5	A	4

Note :

1. Permissive power ripple should be measured under V_{LCD} =5.0V, 25°C, fV(frame frequency)=MAX condition and At that time, we recommend the bandwidth configuration of oscilloscope is to be under 20MHz. See the next page.

2. The specified current and power consumption are under the V_{LCD}=5.0V, 25± 2°Ccondition whereas Typical Power Pattern [Mosaic] shown in the [Figure 3] is displayed.

3. The current is specified at the maximum current pattern of [Figure 3].

4. Maximum Condition of Inrush current :
   The duration of rush current is about 5ms and rising time of power Input is 500us ± 20%.(min.).
   The reference of V_{LCD} Input voltage is LCD INPUT.

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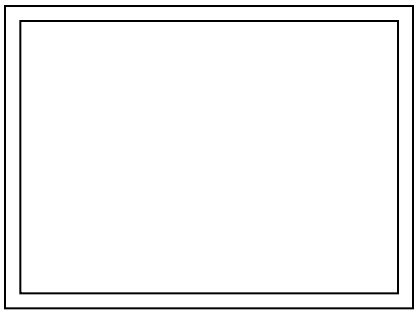
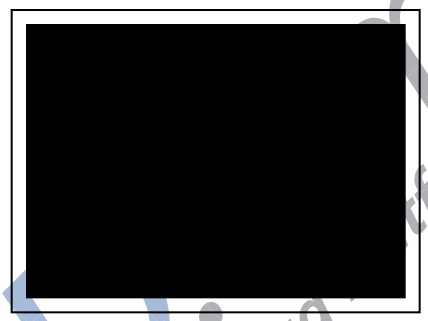
• **Permissive Power input ripple (**V_{LCD} =5.0V, 25°C, fV (frame frequency)=MAX condition**)**

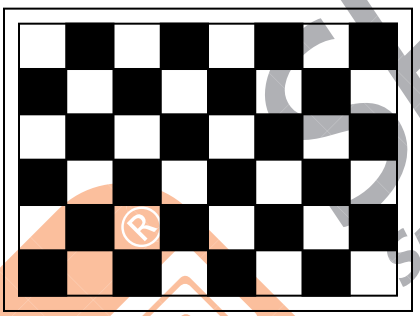


White pattern

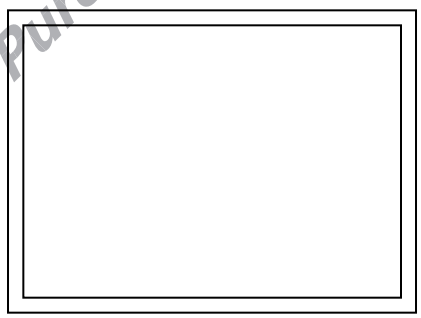


Black pattern

• **Power consumption (**V_{LCD} =5V, 25°C, fV (frame frequency=60Hz condition**)**



Typical power Pattern



Maximum power Pattern

FIG.3 Mosaic pattern & White Pattern for power consumption measurement

3-2. Interface Connections

3-2-1. LCD Module

- LCD Connector(CN1) : IS100-L30O-C23(UJU) , GT103-30S-HF15(LSM), FI-XPB30SL-HF10(JAE)
- Mating Connector : FI-X30H and FI-X30HL (JAE) or Equivalent

Table 3. MODULE CONNECTOR(CN1) PIN CONFIGURATION

Pin No	Symbol	Description
1	RXO0-	Minus signal of 1st channel 0 (LVDS)
2	RXO0+	Plus signal of 1st channel 0 (LVDS)
3	RXO1-	Minus signal of 1st channel 1 (LVDS)
4	RXO1+	Plus signal of 1st channel 1 (LVDS)
5	RXO2-	Minus signal of 1st channel 2 (LVDS)
6	RXO2+	Plus signal of 1st channel 2 (LVDS)
7	GND	Ground
8	RXOC-	Minus signal of 1st clock channel (LVDS)
9	RXOC+	Plus signal of 1st clock channel (LVDS)
10	RXO3-	Minus signal of 1st channel 3 (LVDS)
11	RXO3+	Plus signal of 1st channel 3 (LVDS)
12	RXE0-	Minus signal of 2nd channel 0 (LVDS)
13	RXE0+	Plus signal of 2nd channel 0 (LVDS)
14	GND	Ground
15	RXE1-	Minus signal of 2nd channel 1 (LVDS)
16	RXE1+	Plus signal of 2nd channel 1 (LVDS)
17	GND	Ground
18	RXE2-	Minus signal of 2nd channel 2 (LVDS)
19	RXE2+	Plus signal of 2nd channel 2 (LVDS)
20	RXEC-	Minus signal of 2nd clock channel (LVDS)
21	RXEC+	Plus signal of 2nd clock channel (LVDS)
22	RXE3-	Minus signal of 2nd channel 3 (LVDS)
23	RXE3+	Plus signal of 2nd channel 3 (LVDS)
24	GND	Ground
25	SCL	I2C Serial interface for P_VCOM
26	SDA	I2C Serial interface for P_VCOM
27	PWM_OUT	Reference signal for LED dimming control
28	VLCD	Power Supply (5.0V)
29	VLCD	Power Supply (5.0V)
30	VLCD	Power Supply (5.0V)

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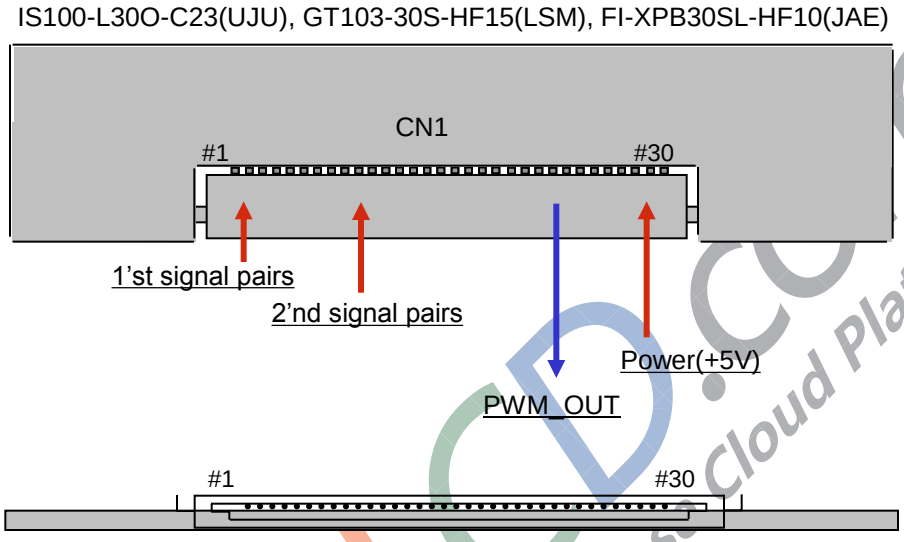
FIG. 4 Connector diagram



Rear view of LCM

Note:

1. NC: No Connection.
2. All GND(ground) pins should be connected together and to Vss which should also be connected to the LCD's metal frame.
3. All V_{LCD} (power input) pins should be connected together.
4. Input Level of LVDS signal is based on the IEA 664 Standard.
5. PWM_OUT is a reference signal for LED PWM control.
   This PWM signal is synchronized with vertical frequency.
   Its frequency is 3 times of vertical frequency, and its duty ratio is 50%.
   If the system don't use this pin, do not connect.

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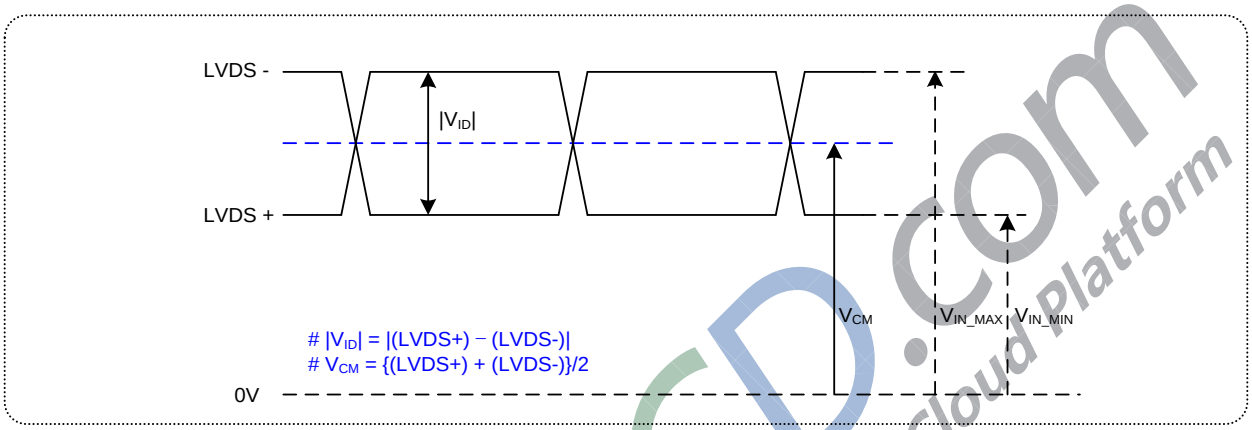
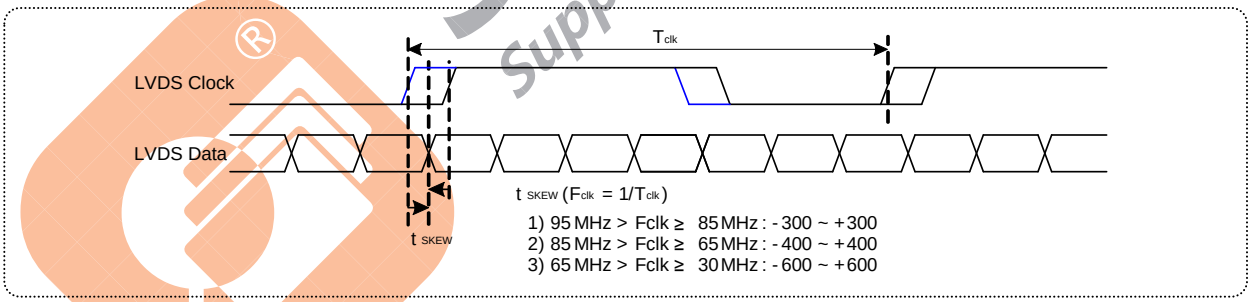
3-3. LVDS characteristics

1. DC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	200	600	mV	-
LVDS Common mode Voltage	V_{CM}	1.0	1.5	V	-
LVDS Input Voltage Range	V_{IN}	0.7	1.8	V	-
Change in common mode Voltage	ΔV_{CM}	-	250	mV	-

2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 300	+ 300	ps	95MHz > Fclk ≥ 85MHz
	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 30MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-

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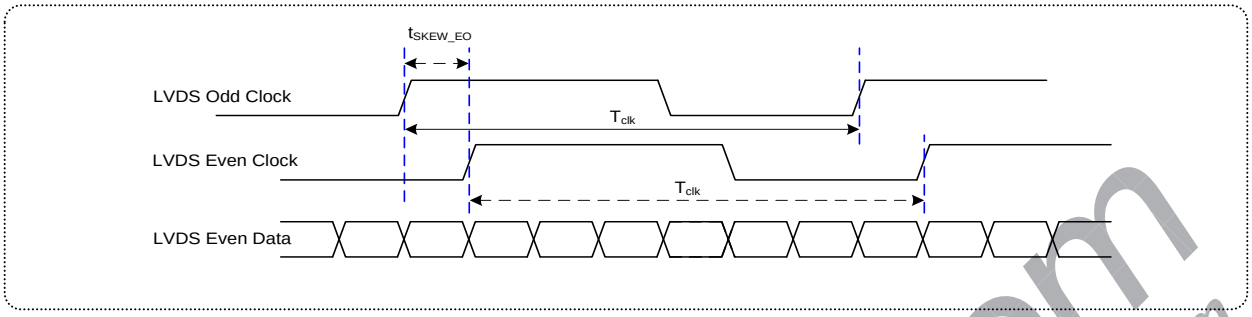
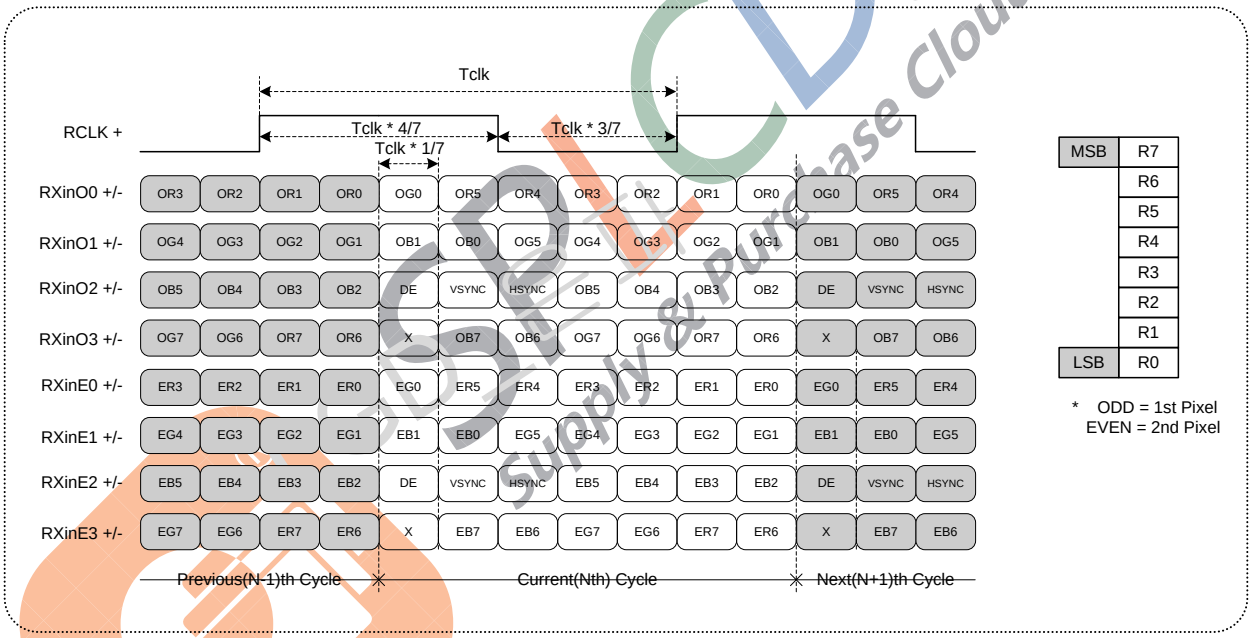


< Clock skew margin between channel >

3. Data Format

1) LVDS 2 Port



< LVDS Data Format >

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Table 4. REQUIRED SIGNAL ASSIGNMENT FOR Flat Link (TI:SN75LVDS83) Transmitter

Pin #	Pin Name	Require Signal	Pin #	Pin Name	Require Signal
1	VCC	Power Supply for TTL Input	29	GND	Ground pin for TTL
2	D5	TTL Input (R7)	30	D26	TTL Input (DE)
3	D6	TTL Input (R5)	31	T_X CLKIN	TTL Level clock Input
4	D7	TTL Input (G0)	32	PWR DWN	Power Down Input
5	GND	Ground pin for TTL	33	PLL GND	Ground pin for PLL
6	D8	TTL Input (G1)	34	PLL VCC	Power Supply for PLL
7	D9	TTL Input (G2)	35	PLL GND	Ground pin for PLL
8	D10	TTL Input (G6)	36	LVDS GND	Ground pin for LVDS
9	VCC	Power Supply for TTL Input	37	TxOUT3 +	Positive LVDS differential data output 3
10	D11	TTL Input (G7)	38	TxOUT3 −	Negative LVDS differential data output 3
11	D12	TTL Input (G3)	39	T_X CLKOUT +	Positive LVDS differential clock output
12	D13	TTL Input (G4)	40	T_X CLKOUT −	Negative LVDS differential clock output
13	GND	Ground pin for TTL	41	T_X OUT2 +	Positive LVDS differential data output 2
14	D14	TTL Input (G5)	42	T_X OUT2 −	Negative LVDS differential data output 2
15	D15	TTL Input (B0)	43	LVDS GND	Ground pin for LVDS
16	D16	TTL Input (B6)	44	LVDS VCC	Power Supply for LVDS
17	VCC	Power Supply for TTL Input	45	T_X OUT1 +	Positive LVDS differential data output 1
18	D17	TTL Input (B7)	46	T_X OUT1 −	Negative LVDS differential data output 1
19	D18	TTL Input (B1)	47	T_X OUT0 +	Positive LVDS differential data output 0
20	D19	TTL Input (B2)	48	T_X OUT0 −	Negative LVDS differential data output 0
21	GND	Ground pin for TTL Input	49	LVDS GND	Ground pin for LVDS
22	D20	TTL Input (B3)	50	D27	TTL Input (R6)
23	D21	TTL Input (B4)	51	D0	TTL Input (R0)
24	D22	TTL Input (B5)	52	D1	TTL Input (R1)
25	D23	TTL Input (RSVD)	53	GND	Ground pin for TTL
26	VCC	Power Supply for TTL Input	54	D2	TTL Input (R2)
27	D24	TTL Input (HSYNC)	55	D3	TTL Input (R3)
28	D25	TTL Input (VSYNC)	56	D4	TTL Input (R4)

Notes : 1. Refer to LVDS Transmitter Data Sheet for detail descriptions.
2. 7 means MSB and 0 means LSB at R,G,B pixel data

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3-4. Signal timing specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

Table 5. Timing table

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
D_{CLK}	Period	t_{CLK}	10.6	13.89	17.4	ns	Pixel frequency : Typ.144MHz
	Frequency	f_{CLK}	59.4	72	90	MHz	
Horizontal	Horizontal Valid	t_{HV}	960	960	960	t_{CLK}	
	H Period Total	t_{HP}	1024	1088	1300		
	Hsync Frequency	f_H	54	66	85.5	kHz	
Vertical	Vertical Valid	t_{VV}	1080	1080	1080	t_{HP}	
	V Period Total	t_{VP}	1090	1100	1366		For D_{CLK}
	Vsync Frequency	f_V	48	60	76	Hz	
DE (Data Enable)	DE Setup Time	t_{SI}	4	-	-	ns	
	DE Hold Time	t_{HI}	4	-	-		
Data	Data Setup Time	t_{SD}	4	-	-	ns	For D_{CLK}
	Data Hold Time	t_{HD}	4	-	-		

Note:

1. DE Only mode operation. The input of Hsync & Vsync signal does not have an effect on LCD normal operation.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rates.
3. Horizontal period should be even.

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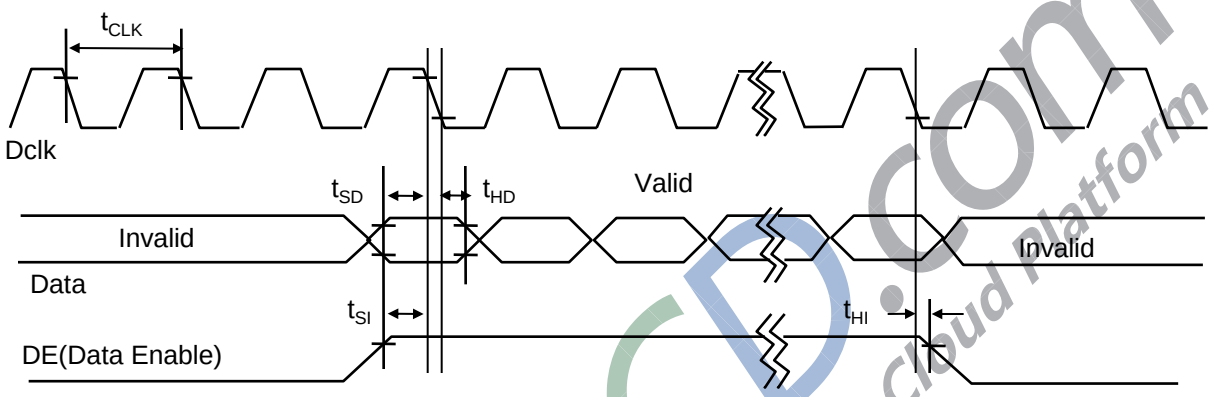
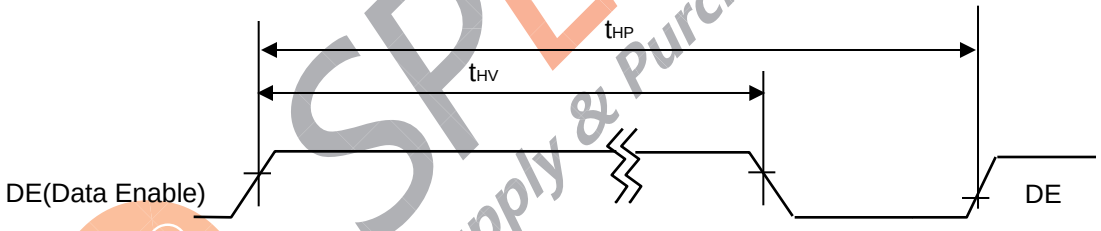
3-5. Signal Timing Waveforms

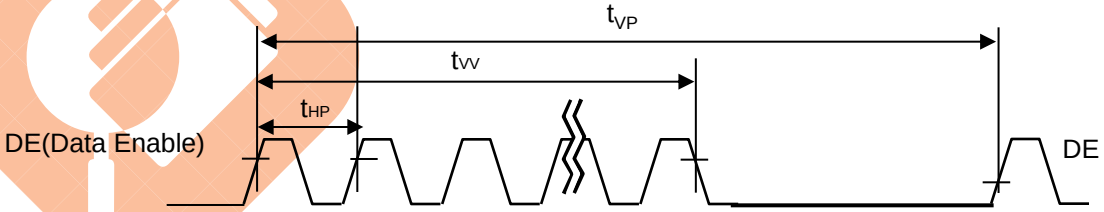
1. DCLK , DE, DATA waveforms



2. Horizontal waveform



3. Vertical waveform



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3-6. Color Input Data Reference

The Brightness of each primary color(red,green,blue) is based on the 8-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																							
		Red (MSB → LSB)								Green (MSB → LSB)								Blue (MSB → LSB)							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(002)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	- - - - - - - - -	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255) Bright	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(002)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	- - - - - - - - -	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue(000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(002)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255) Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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3-7. Power sequence

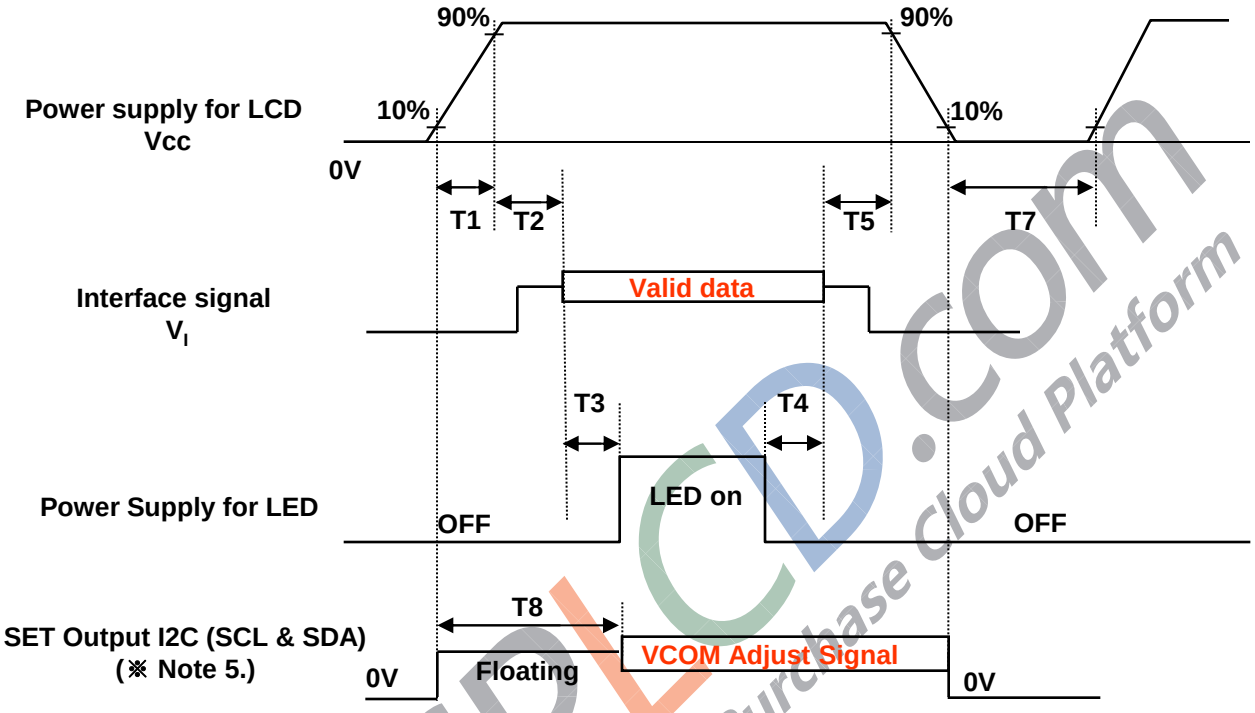

Table 7. POWER SEQUENCE

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0.01	-	50	ms
T3	500	-	-	ms
T4	200	-	-	ms
T5	0.01	-	50	ms
T7	1000		-	ms
T8	500	-	-	ms

Notes :

1. Please V_{LCD} power on only after connecting interface cable to LCD.
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD V_{LCD} to 0V.
4. LED power must be turn on after power supply for LCD an interface signal are valid.
5. When the Vcc is to 0V, The SET output signal (SCL,SDA) must be 0V and the SET output signal (SCL,SDA) must be non-existant the induced voltage during the floating period (500ms after power on) for well-communicating between TCON and EEPROM

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3-8. V_{LCD} Power Dip Condition

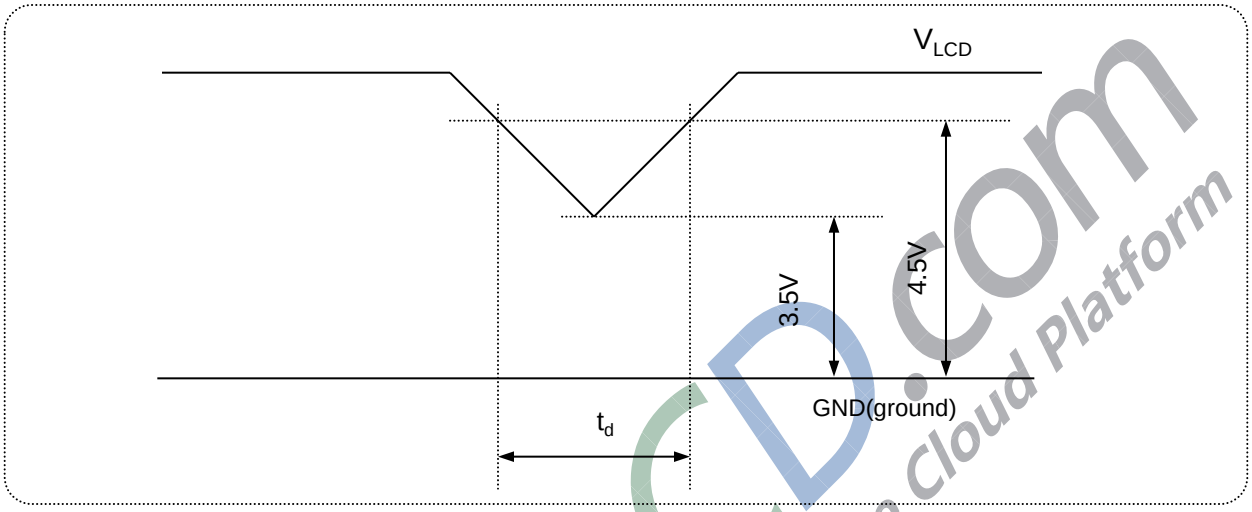

FIG.5 Power dip condition

1) Dip condition

$3.5V \leq V_{LCD} < 4.5V$, $t_d \leq 20ms$

2) $V_{LCD} < 3.5V$

V_{LCD}-dip conditions should also follow the Power On/Off conditions for supply voltage.

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3-9. Control of VCOM voltage

FIG. 6 The Control of VCOM voltage

Parameter	Unit	min.	Typ.	Max.	Notes
Inversion method	-	Horizontal 2 dot inversion (normal pattern) Horizontal 4 dot inversion (Smear pattern)			1
Control Pattern/Gray		FIG.7 @ 127 gray			1
The optimized point	-	Center			
Offset	-	無			
Slave Address	byte	MSB 0 1 0 1 0 0 0 R/W LSB			
Control range	Level (step)	0	64	127	1,2
	Voltage(V)	4.0	4.6	5.2	

1. Fig.7 is the pattern for control & inspection. This pattern made the optimized display about Flicker by FRC ,etc..
2. Signal sequence : This sequence must applied the below spec for IC Damage.
   -. VCC → VDD → Control signa (SCL /SDA)

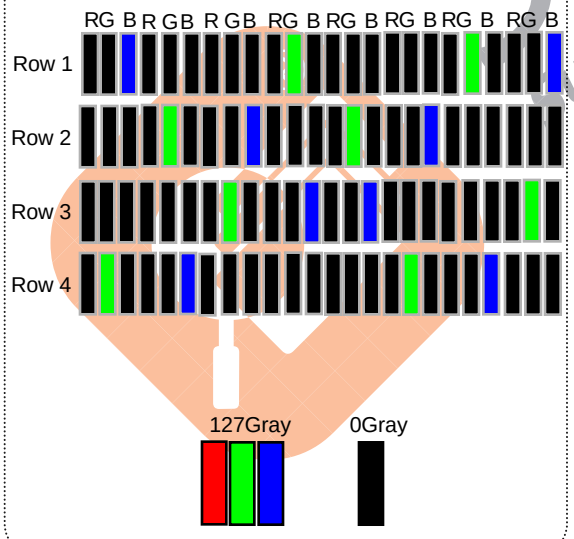
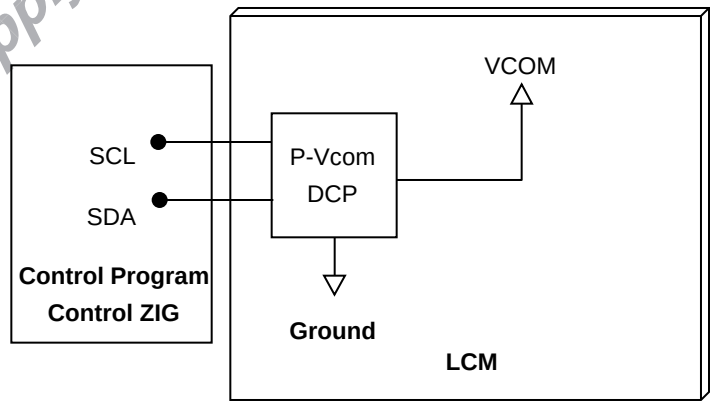


FIG. 7 The Pattern of VCOM control



* DCP : Digitally Controlled Potentiometer

FIG. 8 VCOM Block Diagram

4. Optical specification

Optical characteristics are determined after the unit has been 'ON' for 30 minutes in a dark environment at 25°C.

4-1. 2D Optical specifications

Table 8. Optical characteristics

Ta= 25°C, V_{LCD}=5.0V, fv=60Hz f_{CLK}=72MHz, Is=100mA

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	700	1000	-		1(PR880)
Surface Luminance	white	L_{WH}	200	250	-	cd/m^2	2(PR880)
Response Time (Gray to Gray)		GTG	-	14	28	ms	3(RD80S)
Color Coordinates [CIE1931] (By PR650)	RED	Rx	Typ -0.03	0.638	Typ +0.03		(PR650) Not fixed
		Ry		0.334			
	GREEN	Gx		0.309			
		Gy		0.627			
	BLUE	Bx		0.153			
		By		0.073			
	WHITE	Wx		0.313			
		Wy		0.329			
Viewing Angle (CR>10)							
x axis, right(ϕ=0°)		θr	85	89		Degree	4(PR880)
x axis, left (ϕ=180°)		θl	85	89			
y axis, up (ϕ=90°)		θu	85	89			
y axis, down (ϕ=270°)		θd	85	89			
Crosstalk					1.5	%	5

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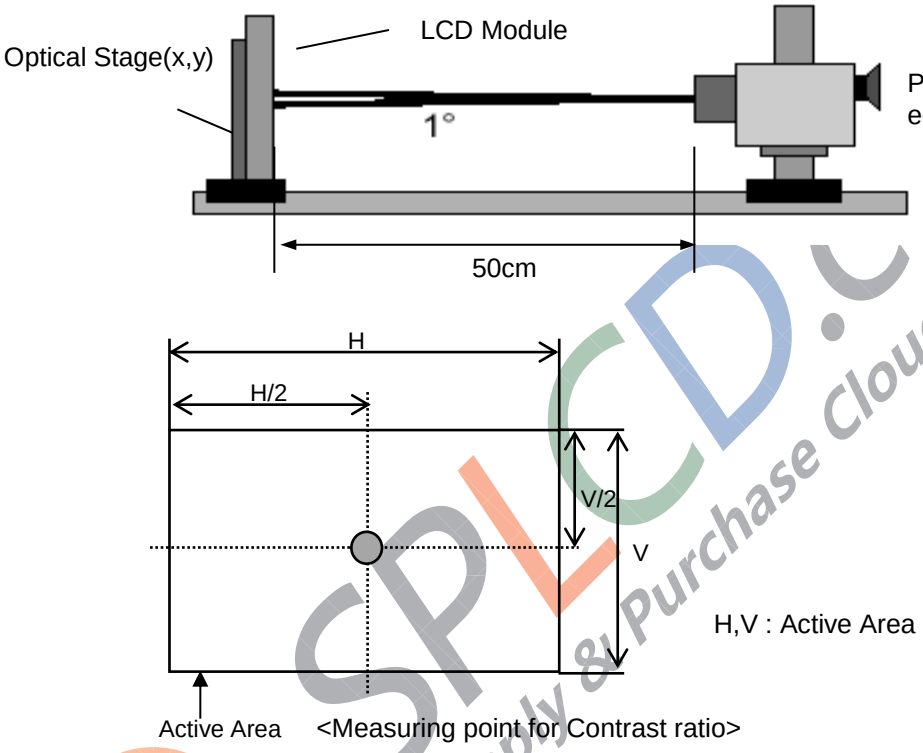
The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 9 presents additional information concerning the measurement equipment and method.

FIG. 9 Optical characteristic measurement equipment and method



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Notes :

1. Contrast ratio(CR) is defined mathematically as :It is measured at center point(1)

$$\text{Contrast ratio} = \frac{\text{Surface luminance with all white pixels}}{\text{Surface luminance with all black pixels}}$$

2. Surface luminance is the luminance value at center 1 point(1) across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 9.

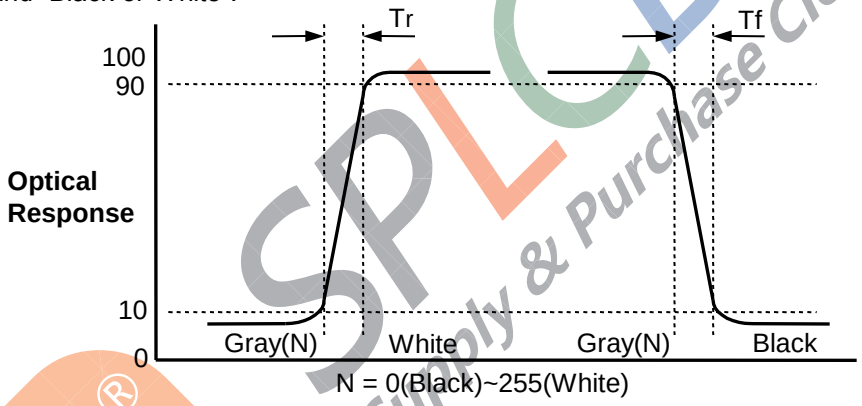
Notes :

3. Gray to gray response time is the time required for the display to transition from gray to gray. For additional information see Table 9. ***(By RD80S)***

Table 9. GTG Gray Table

Gray to Gray		Rising Time				
		G255	G191	G127	G63	G0
Falling Time	G255					
	G191					
	G127					
	G63					
	G0					

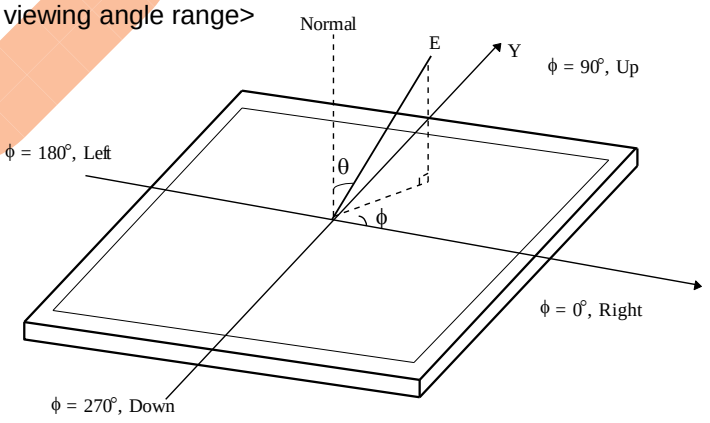
Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Black or White".



4. Viewing angle is the angle at which the contrast ratio is greater than 10 or 5. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG. 10 .

FIG. 10 Viewing angle

<Dimension of viewing angle range>



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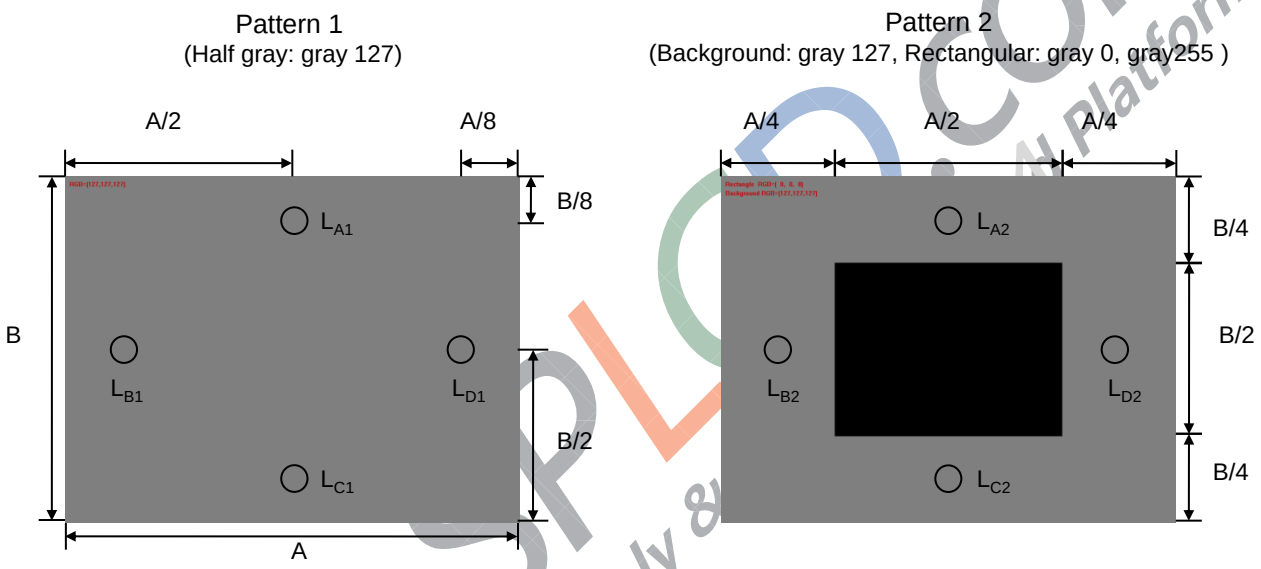
Notes :

5. The equation of crosstalk : ($|L_{A[or\ C]2}-L_{A[or\ C]1}|/L_{A[or\ C]1}$) ×100(%) [Vertical],
($|L_{B[or\ D]2}-L_{B[or\ D]1}|/L_{B[or\ D]1}$) ×100(%) [Horizontal]

FIG. 11 Crosstalk



6. Gray scale specification

Table 10. Gray scale

Gray level	Luminance [%] (Typ)
L0	0.1
L31	1.08
L63	4.72
L95	11.49
L127	21.66
L159	35.45
L191	53.00
L223	74.48
L255	100

5. Mechanical Characteristics

The contents provide general mechanical characteristics. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	526.184mm
	Vertical	303.416mm
	Depth	2.4mm
Active Display Area	Horizontal	509.184mm
	Vertical	286.416mm
Weight	Typ : 470g , Max : 500g	
Surface Treatment	Hard coating (3H), Glare treatment of the front polarizer	

Notes : Please refer to a mechanic drawing in terms of tolerance at the next page.

6. Reliability

Environment test condition

No	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0G RMS Duration : Z Direction, 10 min

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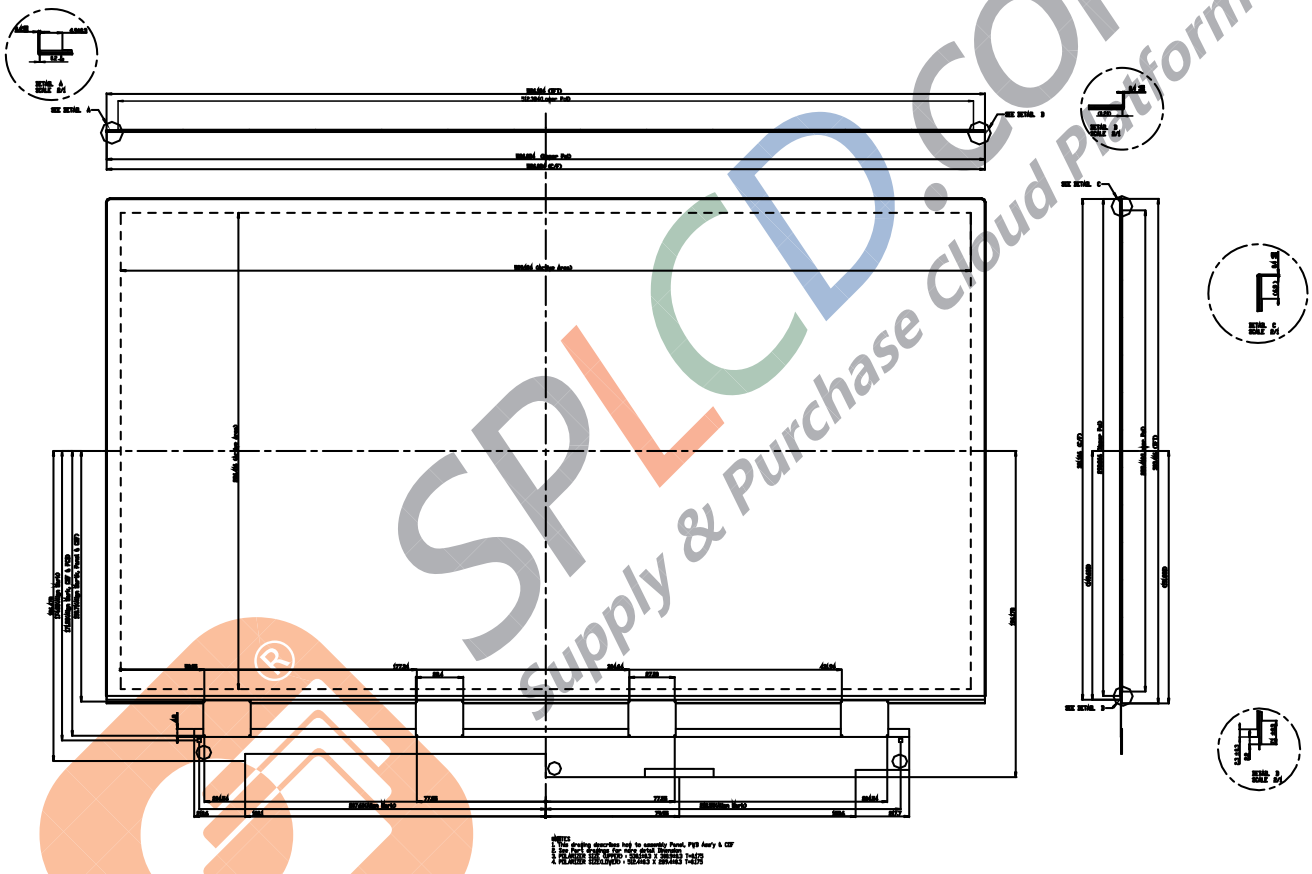
<FRONT VIEW>



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7. International Standards

7-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

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8. Packing

8-1. Packing Form

a) Package quantity in one Pallet : 560 pcs

b) Pallet Size :1,100 mm(L) X 1,330 mm(W) X 1,090 mm(H)

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9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. Assembly Precautions

(1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) You should adopt radiation structure to satisfy the temperature specification.
(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Mechanical structure for backlight system should be designed for sustaining drive ass'y safely.

9-2. Operating precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage : V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to board ass'y. Otherwise, it can not be operated its full characteristics perfectly.
(7) When Sealing assemblies are used for public display, defects such as Yogore, Image sticking can not be guarantee.
(8) Sealing assemblies can not support "Interlaced Scan Method".

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9-3. Electrostatic discharge control

Since a board ass'y is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for strong light exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the board ass'y to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9-6. Life time

The board Assembly life time is minimum 30,000hr,on the condition of continuous operating at 25 ± 2℃.

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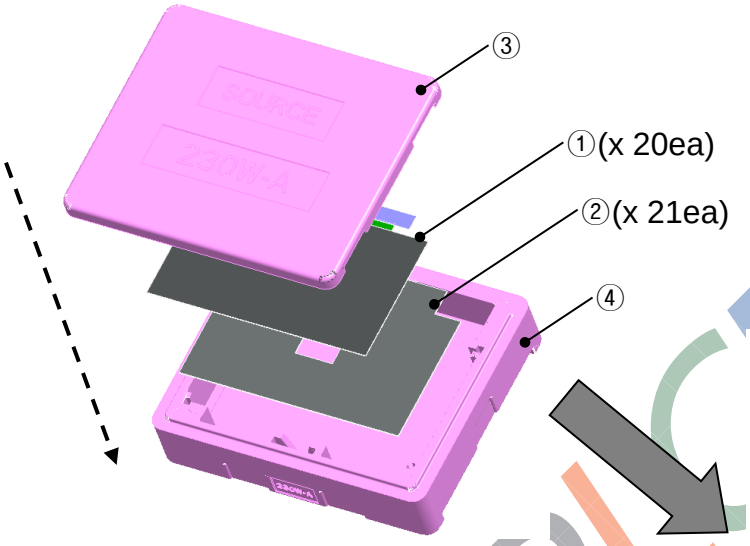
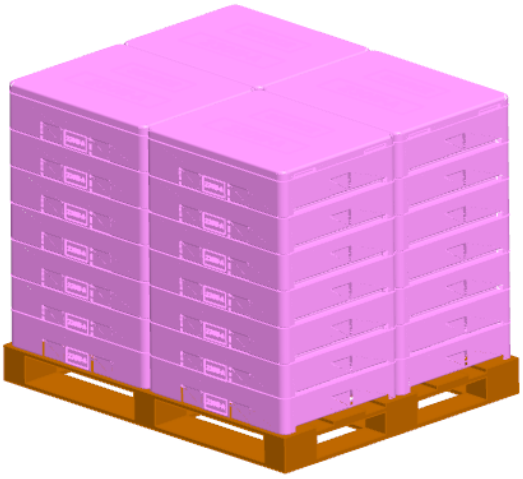
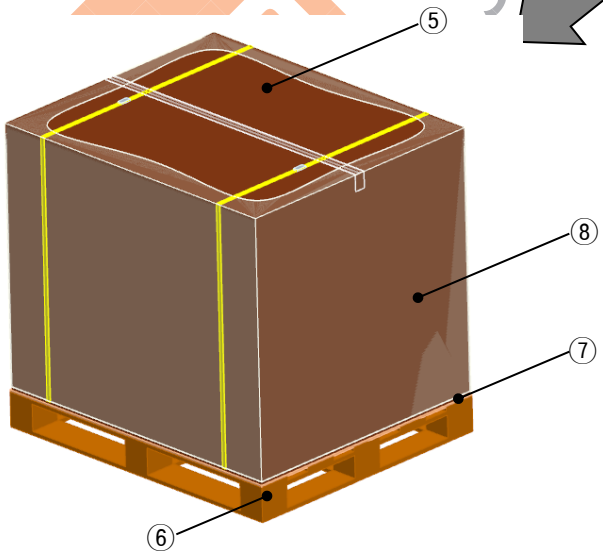
APPENDIX-I

■ LM230WF3-SJE1 – Pallet Ass'y





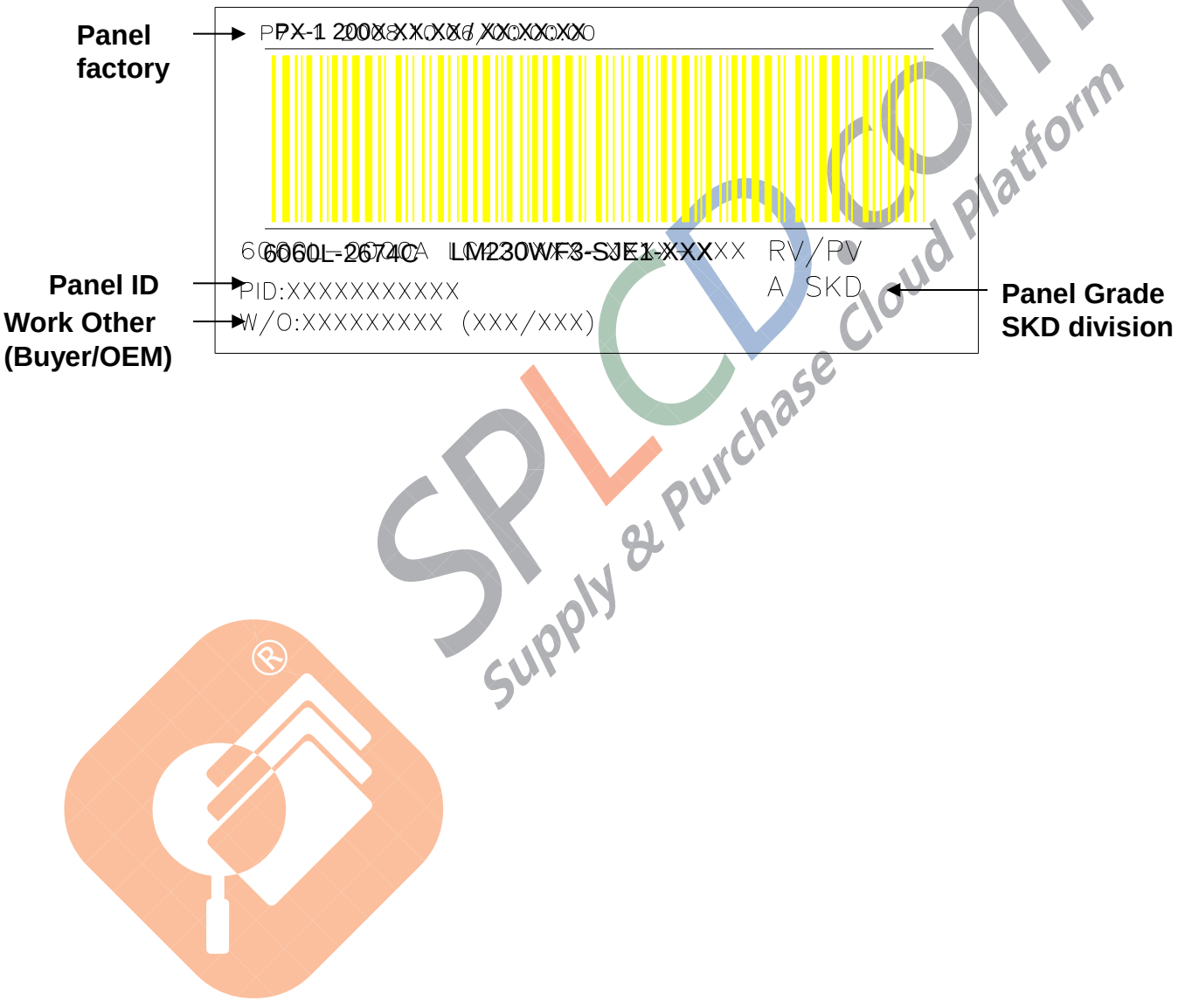
2 x 2 x 7 = 28-Box



No.	Description	Material
①	Board A'ssy	-
②	Sheet	PE
③	Top Packing	EPP
④	Bottom Packing	EPP
⑤	Angle Packing	SW_"A" Flute
⑥	Pallet	Plywood
⑦	Pallet Sheet	DW_"A" Flute
⑧	Wrap	L-LDPE

 # APPENDIX- II-1

■ LM230WF3-SJE1-Board Ass'y ID Label



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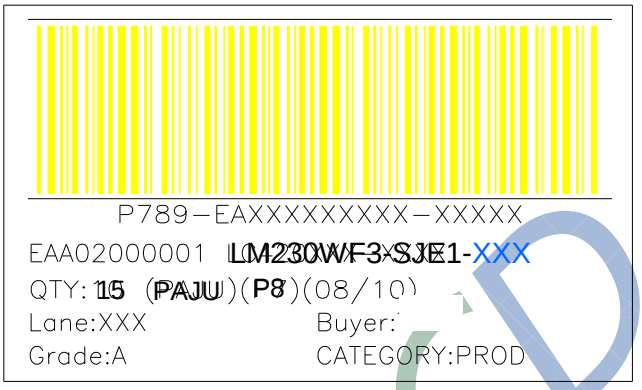
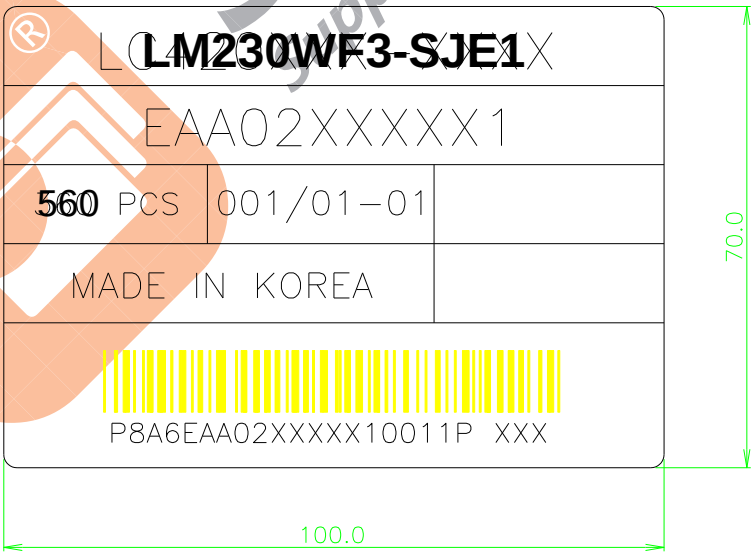
APPENDIX- II-2

■ LM230WF3-SJE1-BOX Label



■ LM230WF3-SJE1-Pallet Label



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