



LM240120FFW

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary release	2014-4-8

1. Basic Specifications

1.1 Display Specifications

- 1) LCD Display Mode : STN, Negative, Transmissive
- 2) Display Color : Display Data = "1" : Light Gray (*1)
: Display Data = "0" : Light Blue (*2)
- 3) Viewing Angle : 12H
- 4) Driving Method : 1/128 duty, 1/12 bias
- 5) Back Light : White LED backlight

Note:

*1. Color tone may slightly change by Temperature and Driving Condition.

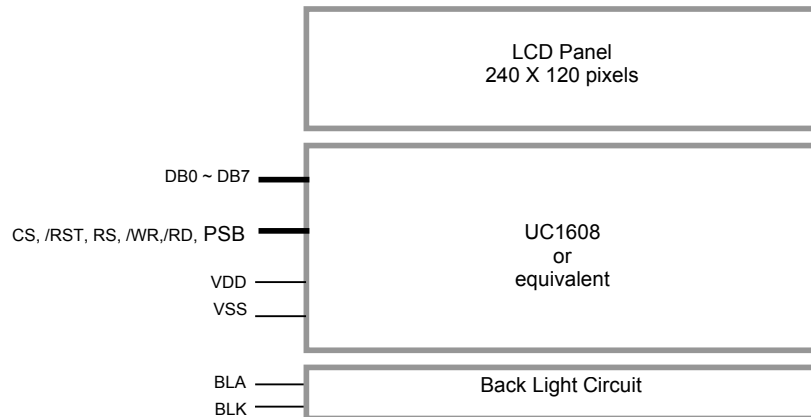
*2. The Color is defined as the inactive / background color

*3. Fine Contrast adjustment function is necessary in the application design for optimal display result

1.2 Mechanical Specifications

- 1) Outline Dimension : 93.0 x 70.0 x 10.1(Max)
(See attached Outline Drawing for details)

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions			
			8080 mode(Default)	6800 mode	4Line SPI mode	
1	VSS	Power	Negative power supply,0V			
2	VDD	Power	Positive power supply			
3	NC	-	No connect			
4	RS	Input	Register Select RS =HIGH: data is display data RS =LOW: data is control data			
5	/WR(R/W)	Input	/WR=L→H Data or Instruction latch into the LCD module	R/W=H,E=H; Data or Status read from the LCD module R/W=L,E=H→L;	Connect to VSS	
6	/RD(E)	Input	/WR=H, /RD=L; Data or Status read from the LCD module	Data or Status latch into the LCD module	Connect to VSS	
7	DB0(SCK)	I/O	8-bit Data bus; Three state I terminal for display data or instruction data when /CS =L, DB0~DB7=Hi-Z			
:	:					
10	DB3(SDA)					Serial clock input
:	:					Connect to VSS
14	DB7		Serial data input	Connect to VSS		
15	PSB	-	Serial and parallel Select (*2)			
16	CS	Input	Chip Select CS=High : Data IO is enabled			
17	/RST	Input	Reset: /RST=LOW: Initialization is executed /RST=HIGH: Normal			
18	NC	-	No connect			
19	BLA	Power	Backlight Positive Power Supply			
20	BLK	Power	Backlight Negative Power Supply			

Note:

1. About Interface setting, please refer to UC1608 datasheet for more detail.
2. It is used when JP1,JP2 are opened and JP5 is closed.

Interface setting:

Setting	8080 mode(Default)	6800 mode	4Line SPI mode
JP1	CLOSE	CLOSE	OPEN
JP2	OPEN	OPEN	CLOSE
JP3	OPEN	CLOSE	OPEN
JP4	CLOSE	OPEN	CLOSE
JP8	OPEN	OPEN	CLOSE

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	$V_{SS} = 0V$
Input Voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V	$V_{SS} = 0V$
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

$V_{SS}=0V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	V_{DD}	2.7	3.0	3.3	V	VDD
Input High Voltage	V_{IH}	$0.8xV_{DD}$	-	V_{DD}	V	/RST, CS, RS, /WR, /RD, PSB, DB0~DB7
Input Low Voltage	V_{IL}	0	-	$0.2xV_{DD}$	V	
Operating Current	I_{DD}	-	0.8		mA	VDD

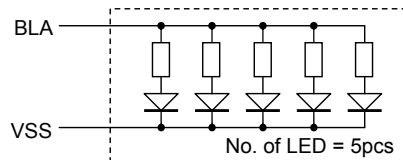
3.2 LED Backlight Circuit Characteristics

$V_{SS}=0V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	$V_{f_{BLA}}$	-	3.3	-	V	BLA
Forward Current	$I_{f_{BLA}}$	-	74	100	mA	BLA

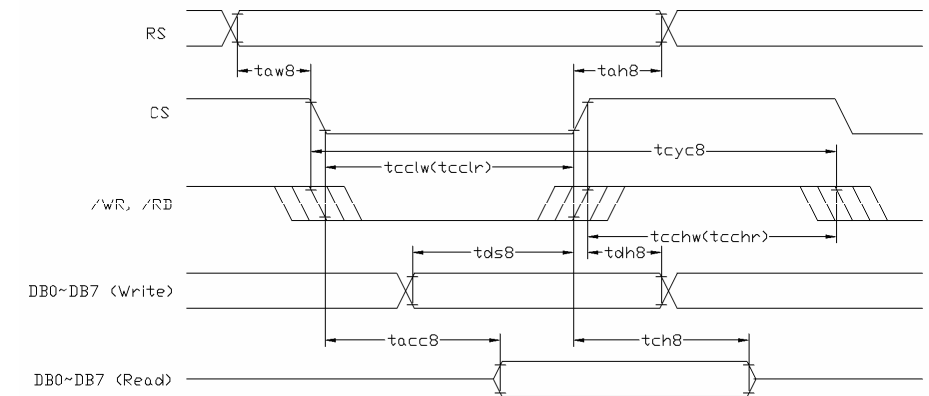
Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



3.3 AC Characteristics

3.3.1 8080 Mode System Bus Timing



Parallel Bus Timing Characteristics(for 8080MCU)

$V_{SS}=0V, 2.7V \leq V_{DD} \leq 3.3V, T_{OP}=25^{\circ}C$

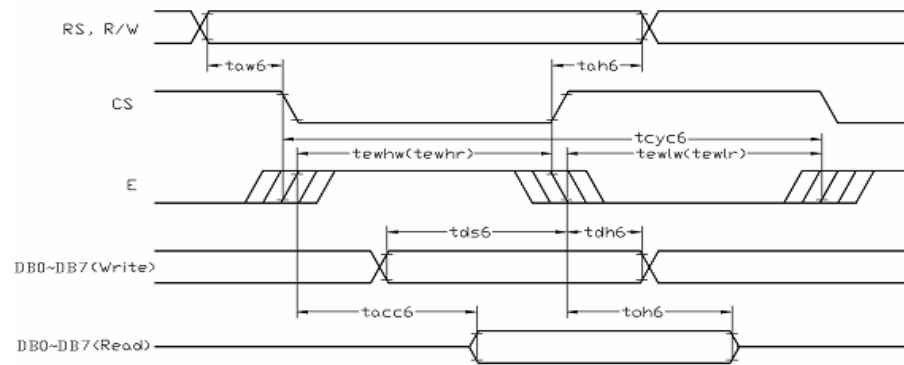
Item	Symbol	MIN.	TYP.	MAX.	Unit
System cycle time	tcyc8	160	-	-	ns
Address setup time (RS)	taw8	20	-	-	ns
Address hold time (RS)	tah8	50	-	-	ns
Control LOW pulse width (/WR)	tcclw	55	-	-	ns
Control LOW pulse width (/RD)	tcclr	85	-	-	ns
Control HIGH pulse width (/WR)	tcchw	55	-	-	ns
Control HIGH pulse width (/RD)	tcchr	85	-	-	ns
Data setup time	tds8	50	-	-	ns
Data hold time	tdh8	40	-	-	ns
/RD access time (*2)	tacc8	-	-	80	ns
Output disable time (*2)	tch8	12	-	20	ns

Note:

*1. Input signal rise/fall time should be less than 12ns

*2. CL=100pF

3.3.2 6800 Mode System Bus Timing



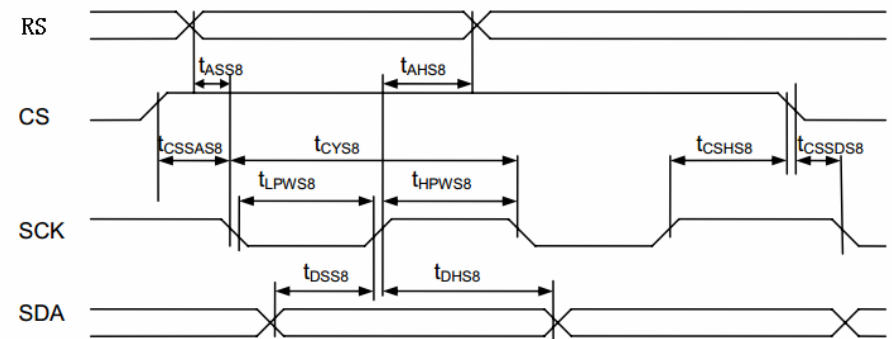
Parallel Bus Timing Characteristics(for 6800MCU)

$V_{SS}=0V, 2.7V \leq V_{DD} \leq 3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
System cycle time	tcyc6	160	-	-	ns
Address setup time (RS)	taw6	20	-	-	ns
Address hold time (RS)	tah6	40	-	-	ns
Control LOW pulse width (E)	tewlr(tewlw)	80	-	-	ns
Control HIGH pulse width (E)	tewhr(tewhw)	80	-	-	ns
Data setup time	tds6	50	-	-	ns
Data hold time	tdh6	40	-	-	ns
/RD access time (*2)	tacc6	-	-	60	ns
Output disable time (*2)	toh6	-	-	20	ns

Note:
*1. Input signal rise/fall time should be less than 12ns
*2. CL=100pF

3.3.3 SPI Mode System Bus Timing

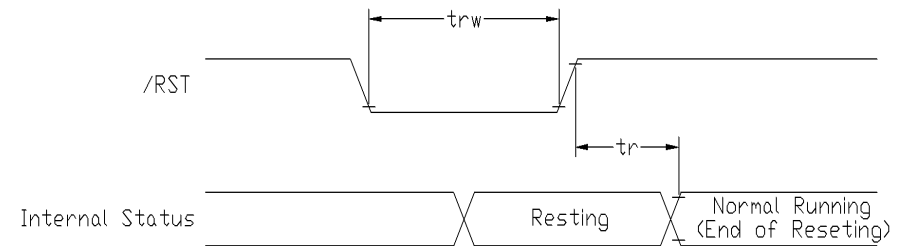


SPI Bus Timing Characteristics

$V_{SS}=0V, 2.7V \leq V_{DD} \leq 3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Serial Clock Period	tCYS8	160	-	-	ns
SCL "H" pulse width(SCL)	tHPWS8	75	-	-	ns
SCL "L" pulse width(SCL)	tLPWS8	75	-	-	ns
Address setup time(RS)	tASS8	20	-	-	ns
Address hold time(RS)	tAHS8	40	-	-	ns
Data setup time(SDA)	tDSS8	50	-	-	ns
Data hold time(SDA)	tDHS8	40	-	-	ns
/CS-SCL time	tCSSAS8	20	-	-	ns
/CS-SCL time	tCSS8	50	-	-	ns

3.3.4 Reset Timing



$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset time	tr	-	-	15	ms
Reset LOW pulse width	trw	2	-	-	μs

Note:
*1. Input signal rise/fall time should be less than 12ns

4. Function Specifications

4.1 Adjusting the Display Contrast

This LCD module equipped with latest digital contrast adjustment function. Its display contrast could be adjusted by MCU command.

(Please see the command tables for details)

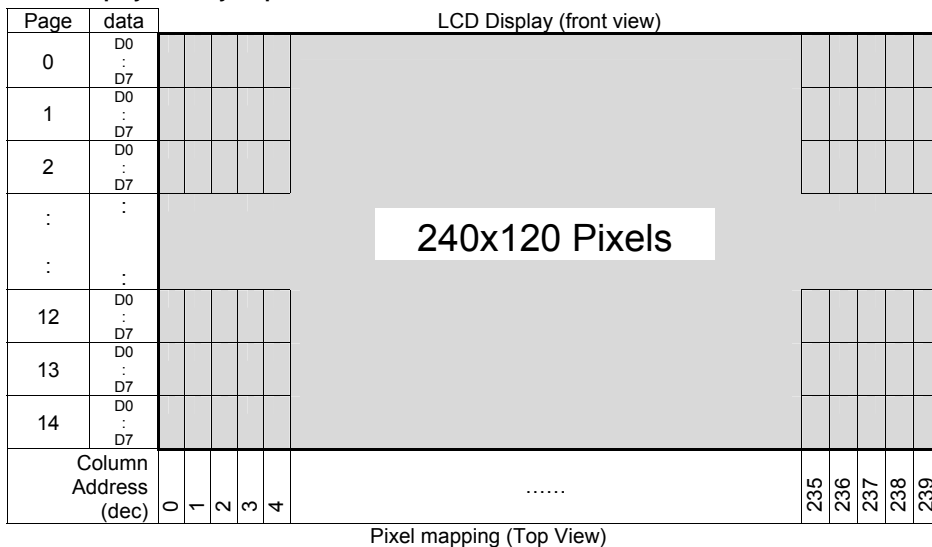
It is recommended to provide a contrast adjustment interface for end-user, where the best display result could meet the individual preference in mass production.

4.2 Resetting the LCD module

The LCD module should be initialized by using /RST terminal.

While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level. After the power supply stabilized, release the reset terminal (/RST=HIGH)

4.3 Display Memory Map



Note:

*1. Based on the top view of the LCD module,

4.4 Commands

4.4.1 Register Table

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127- 2xFL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CR	8	00H	Return Column Address. Useful for cursor implementation.
CA	8	00H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	4	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS} . 00b= 10.7 01b= 11.3 10b= 12.0 11b= 12.7
TC	2	0H	Temperature Compensation (per °C). 00b: 0.0% 01b: -0.05% 10b: -0.1% 11b: -0.2%
GN	2	3H	Gain, coarse setting of V_{BIAS} and V_{LCD}
PM	6	00H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
MR	1	1H	Multiplexing Rate: Number of pixel rows: 0b: 96 1b: 128
OM	2	-	Operating Modes (Read Only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
BZ	1	-	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1	-	Reset in progress, Host Interface not ready
PC	3	5H	Power Control. PC[1:0]: Panel Loading 00b: LCD < 26nF 01b: 26nF < LCD < 43nF 10b: 43nF < LCD < 60nF 11b: 60nF < LCD < 90nF For COG module, the ITO substrate for SEG plate and COM routing: 15 , /Sq - 15nF < LCD < 35nF. 10 , /Sq - 35nF < LCD < 50nF 7 , /Sq - 50nF < LCD < 75nF PC[2]: Pump Control 0b: External V_{LCD} 1b: Internal V_{LCD}

4.4.2 Register Table (continue)

Name	Bits	Default	Description
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (Default 0 : OFF) DC[1]: APO: All Pixels ON (Default 0 : OFF) DC[2]: Display ON/OFF (Default 0 : OFF).
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default 1 : ON) AC[1]: Reserved (always set to 0) AC[2]: PID: PA (page address) auto increment direction (0 : +1 , 1 : -1) AC[3]: CUM: Cursor update mode, (Default 0 : OFF) when CUM=1, CA increment on write only, wrap around suspended
LC	4	0H	LCD Mapping Control: LC[0]: MSF: MSB First mapping Option (Default 0 : OFF) LC[1]: Reserved (always set to 0) LC[2]: MX, Mirror X (Column sequence inversion) (Default 0 : OFF) LC[3]: MY, Mirror Y (Row sequence inversion) (Default 0 : OFF)
APC0	8	2AH	Advanced Product Configuration. For UltraChip only. Please do not use.
APC1	4	EH	Advanced Product Configuration. For UltraChip only. Please do not use.

4.5 Command Table

The following setting should be issue to LCD module after hardware reset.

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Mux Rate and temperature compensation.	0	0	0	0	1	0	0	#	#	#	Set {MR, TC[1:0]}	MR: 1b TC: 00b
6	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	101b
7	Set Adv. Program Control. (double byte command)	0	0	0	0	1	1	0	0	0	R	For UltraChip only. Do not use.	N/A
	Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9	Set Gain and Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set {GN[1:0], PM[5:0]}	GN=3 PM=0
	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
11	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0=disable
12	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0=disable
13	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0=disable
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
16	Set LCD Mapping Control	0	0	1	1	0	0	#	#	#	#	Set LC[3:0]	0
17	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
18	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
19	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b=12
20	Reset Cursor Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
21	Set Cursor Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
22	Set Test Control	0	0	1	1	1	0	0	1	TT		For UltraChip only.	N/A
	(double byte command)	0	0	#	#	#	#	#	#	#	#	Do not use.	

Note:

Please refer to UC1608 data sheet for details

W/R=0 means it is a write function, W/R=1 means it is a read function

D/C=0 means it is a control data, D/C=1 means it is a display data

Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping from high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free from twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module