



深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

# LM240128FCW-C

## LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary release	2016-06-07

## Table of Content

<b>1. Basic Specifications</b> .....	<b>3</b>
1.1 Display Specifications .....	3
1.2 Mechanical Specifications .....	3
1.3 Block Diagram .....	3
1.4 Terminal Functions .....	4
<b>2. Absolute Maximum Ratings</b> .....	<b>5</b>
<b>3. Electrical Characteristics</b> .....	<b>5</b>
3.1 DC Characteristics .....	5
3.2 LED Backlight Circuit Characteristics .....	5
3.3 AC Characteristics .....	6
<b>4. Function specifications</b> .....	<b>8</b>
4.1 Adjusting the Display Contrast.....	8
4.2 Resetting the LCD module .....	8
4.3 Display Commands.....	9
4.4 Touch screen operating command .....	13
<b>5. Design and Handling Precaution</b> .....	<b>14</b>

## 1. Basic Specifications

### 1.1 Display Specifications

- 1) LCD Display Mode : FSTN, Positive, Transflective
- 2) Display Color : Display Data = "1" : Light Gray(\*1)  
: Display Data = "0" : Dark Blue (\*2)
- 3) Viewing Angle : 6H
- 4) Driving Method : 1/128 duty, 1/12 bias
- 5) Backlight : White LED backlight

Note:

\*1. Color tone may slightly change by Temperature and Driving Condition.

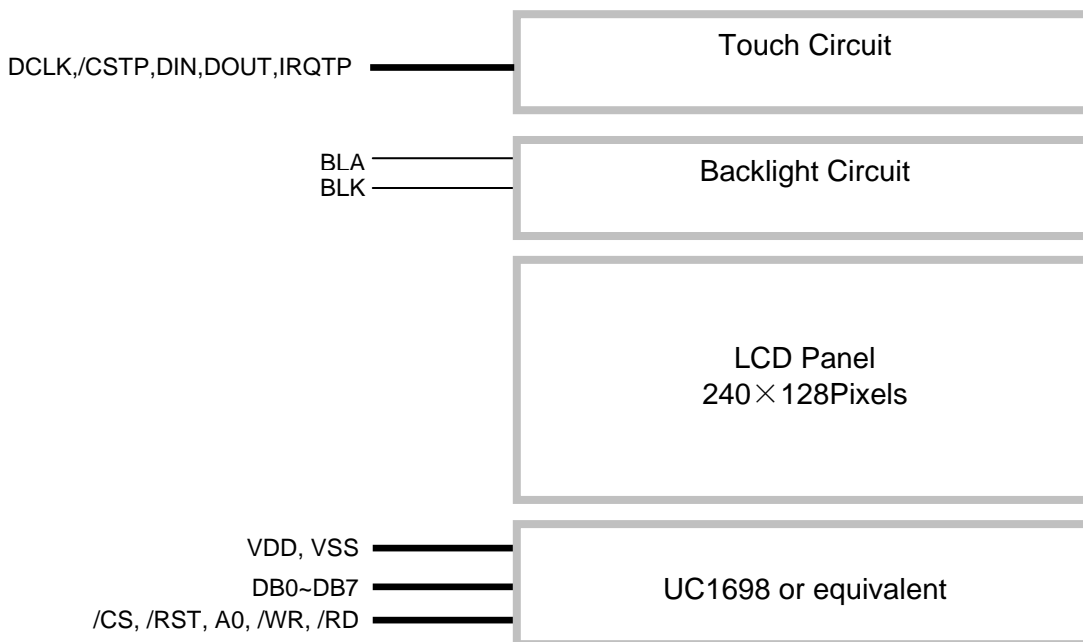
\*2. The Color is defined as the inactive / background color

\*3. Fine Contrast adjustment function is necessary in the application design for optimal display result

### 1.2 Mechanical Specifications

- 1) Outline Dimension : 144.0 x 104.0 x 12.3mm  
(See attached Outline Drawing for details)

### 1.3 Block Diagram



## 1.4 Terminal Functions

K1 Pin No.	PIN Name	I/O	Descriptions	
1	VSS	Power	Negative power supply,0V	
2	VDD	Power	Positive power supply	
3	NC	-	No connection, leave open	
4	A0	Input	Register Select A0 = H, Transferring the Display Data A0 = L, Transferring the Control Data	
5	/WR	Input	/WR=L→H, /RD=H; Data or Instruction latch into the LCD module	
6	/RD	Input	/WR=H, /RD=L; Data or Status read form the LCD module	
7	DB0	I/O	8-bit Data bus; Three state I/O terminal for display data or instruction data when /CS=H, DB0~DB7=High Impedance	
:	:			
14	DB7			
15	/CS	Input	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module	
16	/RST	Input	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.	
17	NC	-	No connection, leave open	
18	NC	-	No connection, leave open	
19	DCLK	Input	Control the touch interface	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
20	/CSTP	Input		Chip Select Input. Controls conversion timing and enables the serial input/output register.
21	DIN	Input		Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK.
22	DOUT	Output		Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH.
23	IRQTP	Output		Pen Interrupt. Open anode output (requires 10k Ω to 100k Ω pull-up resistor externally).
24	NC	-	No connection, leave open	
25	BLA	Power	Positive power for LED backlight	
26	BLK	Power	Negative power for LED backlight	

## 2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	$V_{DD}$	-0.3	+3.6	V	$V_{SS} = 0V$
Input Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	V	$V_{SS} = 0V$
Operating Temperature	$T_{OP}$	-20	+70	°C	No Condensation
Storage Temperature	$T_{ST}$	-30	+80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## 3. Electrical Characteristics

### 3.1 DC Characteristics

$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	$V_{DD}$	2.7	3.3	3.3	V	VDD
Input High Voltage	$V_{IH}$	$0.8 \times V_{DD}$	-	$V_{DD}$	V	/RST, /CS, A0, DCLK,
Input Low Voltage	$V_{IL}$	$V_{SS}$	-	$0.2 \times V_{DD}$	V	/CSTP, DIN, DOUT, IRQTP, DB0~DB7, /RD, /WR
Operating Current	$I_{DD}$	-	TBD	TBD	mA	VDD

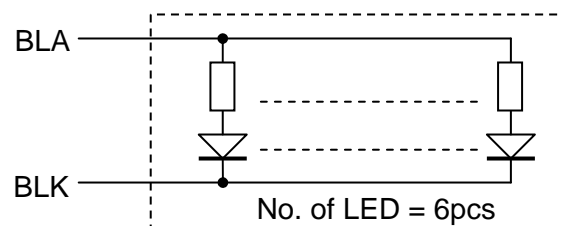
### 3.2 LED Backlight Circuit Characteristics

$V_{SS}=0V, I_{f_{BLA}}=120mA, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	$V_{f_{BLA}}$	-	3.3V	-	V	BLA
Forward Current	$I_{f_{BLA}}$	-	102	120	mA	BLA

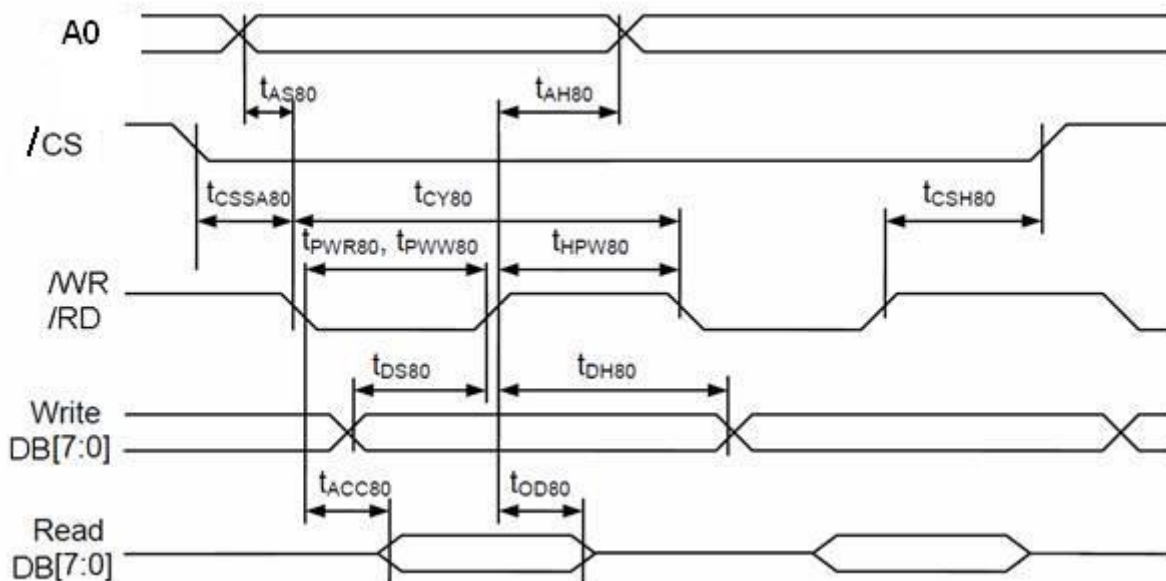
Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



3.3 AC Characteristics

3.3.1 8080 Mode System Bus Timing



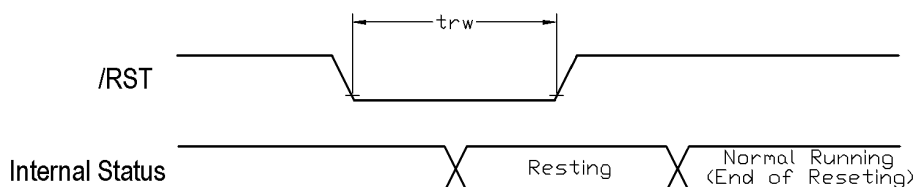
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (CD)	tas80	5	-	-	ns
Address hold time (CD)	tah80	5	-	-	ns
System cycle time (8bit)	tcy80	145	-	-	ns
Read pulse width	tpwr80	107	-	-	ns
Write pulse width	tpww80	65	-	-	ns
High pulse width (read)	thpw80	65	-	-	ns
High pulse width (write)	thpw80	59	-	-	ns
Data setup time	tds80	39	-	-	ns
Data hold time	tdh80	5	-	-	ns
Data access time	tacc80	-	-	78	ns
Data output disable time	tod80	10	-	21	ns
Chip select setup time	tcssa80	7	-	-	ns
Chip select hold time	tcsh80	7	-	-	ns

Note:

- \*1. Input signal rise/fall time should be less than 15ns .
- \*2. CL=100pF
- \*3.All timing is using 20% and 80% of VDD as the reference.

3.3.2 Reset Timing



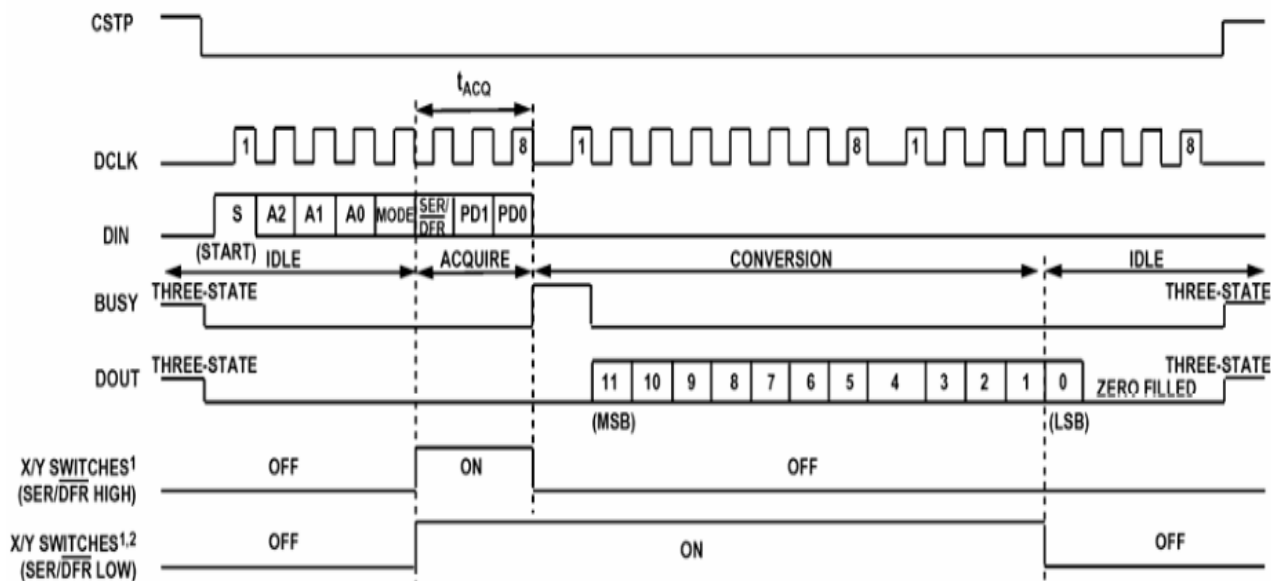
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	trw	4	-	-	ms
Internal Resetting time	trd	13			

Note:

- \*1.All timing is using 20% and 80% of VDD as the reference.

3.3.3 ADS7843 control Timing



Timing diagram

$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Acquisition time(*1)	$t_{ACQ}$	2	-	-	us
CSTP Falling to First DCLK Rising	$t_1$	130	-	-	ns
CSTP Falling to BUSY Enabled(*2)	$t_2$	-	-	140	ns
CSTP Falling to DOUT Enabled	$t_3$	-	-	140	ns
DCLK high pulse width	$t_4$	260	-	-	ns
DCLK low pulse width	$t_5$	260	-	-	ns
DCLK Falling to BUSY Rising(*2)	$t_6$	-	-	140	ns
Data setup prior to DCLK Rising	$t_7$	130	-	-	ns
Data Hold to DCLK hold time	$t_8$	13	-	-	ns
Data access time after DCLK falling	$t_9$	-	-	140	ns
CSTP Rising to DOUT Disabled	$t_{10}$	0	-	-	ns
CSTP Rising to BUSY high impedance(*2)	$t_{11}$	-	-	140	ns
CSTP Rising to DOUT high impedance	$t_{12}$	-	-	140	ns

NOTE:

\*1 See Serial Data Sequence Diagram.

\*2 The BUSY signal is not connected to Terminal, after one control byte send via DIN, some delay is needed to read the conversation result through DOUT.

\*3 Please see the AD7843 datasheet for details.

## 4. Function specifications

### 4.1 Adjusting the Display Contrast

This LCD module equipped with latest digital contrast adjustment function.

Its display contrast could be adjusted by MCU command.

(please see the command tables for details)

It is recommended to provide a contrast adjustment interface for end-user, where the best display result could meet the individual preference in mass production.

### 4.2 Resetting the LCD module

The LCD module should be initialized by using /RST terminal.

While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level. After the power supply stabilized, release the reset terminal (/RST=HIGH)

#### 4.2.1 Display Memory Map

ROW no.	LCD Display (front view)																						
1 <sup>st</sup>																							
2 <sup>nd</sup>																							
3 <sup>rd</sup>																							
:																							
126 <sup>th</sup>																							
127 <sup>th</sup>																							
128 <sup>th</sup>																							
<b>Column no.</b>												1 <sup>st</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	4 <sup>th</sup>	5 <sup>th</sup>	6 <sup>th</sup>	→	238 <sup>th</sup>	239 <sup>th</sup>	240 <sup>th</sup>	241 <sup>th</sup>	242 <sup>th</sup>
<b>Column Address</b>												00h		01h		→		4fh		50h			

Note:

\*1. This mono LCM is driven by a color LCD driver.

Every three dots are being driven by R G B segment driver.

\*2. The above is based on:

- 4R4G4B setting, each dot will be driven by 4bit; LC[7:6]=0:1, DC[4]=1
- Mirror Y direction; LC[2]=1
- Normal X direction; LC[1]=0
- Color Mapping as RGB; LC[5]=1

\*3. For details please refer to UC1698 datasheet



### 4.3 Display Commands

The LCD module contains register, which control the operation. These register can be modified by commands. The following table is a summary of the control registers, their meaning and their default value.

#### 4.3.1 Register Table

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (159 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL).  When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions.  When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between $V_{LCD}$ and $V_{BIAS}$ . 00b: 5                      01b: 10 10b: 11                    11b: 12
TC	2	0H	Temperature Compensation (per °C) 00b: -0.00%              01b: -0.05% 10b: -0.15%              11b: -0.25%
PM	8	40H	Electronic Potentiometer to fine tune $V_{BIAS}$ and $V_{LCD}$
PMO	7	00H	PM offset. PMO[6]=1b: The effective PM value, $PMV = PM - PMO[5:0]$ PMO[6]=0b: The effective PM value, $PMV = PM + PMO[5:0]$
PC	2	2H	Power Control. PC[0]: 0b: $LCD \leq 13nF$ 1b: $13nF < LCD \leq 22nF$ PC[1]: 0b: External $V_{LCD}$ 1b: Internal $V_{LCD}$ (10x charge pump)
AC	4	1H	Address Control. AC[0]: WA: Automatic column/row Wraparound (Default 1 : ON) AC[1]: Auto-Increment order 0b : Column (CA) first 1b : Row (RA) first AC[2]: RID: RA (row address) Auto Increment Direction (L : +1 H : -1) AC[3] : Window Program Mode 0b : Inside Mode: Write to SRAM within the window defined by (WPC0,WPP0) and (WPC1,WPP1) 1b : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0) and (WPC1,WPP1)

## Register Table (continue)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default <b>0: OFF</b> ) DC[1]: APO: All Pixels ON (Default <b>0: OFF</b> ) DC[2]: Display ON/OFF (Default <b>0: OFF</b> ) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode <b>1 : 32-shade Mode</b> DC[4]: Green Enhance Mode. <i>Only valid in 4K-color mode.</i> 0 : Enable. Allows an extra display bit for green color. <b>1 : Disable</b>
LC	9	090H	LCD Control: LC[0]: Enable the top FLT <sub>x2</sub> and bottom FLB <sub>x2</sub> lines in partial display mode (Default <b>0: OFF</b> ). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: <b>0: OFF</b> ) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: <b>0: OFF</b> ) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 25.2. Klps                      01b: 30.5 Klps <b>10b: 37.0 Klps</b> 11b: 44.8 Klps Line Rate (for On/Off mode) 00b: 8.5 Klps                      01b: 10.4 Klps <b>10b: 12.6 Klps</b> 11b: 15.2 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) <b>0 : BGR-BGR</b> 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode.              4R-4G-4B (12-bit/RGB) <b>10b : 64K color mode.</b> 5R-6G-5B (16-bit/RGB) when DC[4]=0: 01b : 4K color mode.              4R-5G-3B (12-bit/RGB) 10b : 64K color mode.              5R-6G-5B (16-bit/RGB) LC[8] : Partial Display Control <b>0b: Disable</b> Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled    Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	5	1DH	N-Line Inversion: NIV[2:0]:    000b: 11 lines              001b: 19 lines 010b: 21 lines              011b: 25 lines 100b: 29 lines <b>101b: 31 lines</b> 110b: 37 lines              111b: 43 lines NIV[3]:    0b: no-XOR <b>1b: XOR</b> NIV[4]:    0b: Disable NIV <b>1b: Enable NIV</b>
CSF	3	0H	COM Scan Function CSF[0]: Interlace Scan Function <b>0b: LRM sequence: AEBCD-AEBCD</b> 1b: LRM sequence: AEBCD-EBCDA CSF[1]: FRC function <b>0: Disable FRC</b> 1: Enable FRC CSF[2]: Shade-1 / Shade-30 option <b>0: Dither directly on input data (SRAM Change)</b> 1: PWM (Pulse-width modulation) on SEG output stage

## Register Table (continue)

Name	Bits	Default	Description
CEN	8	9FH	COM scanning end (last COM with full line cycle, 0 based index)
DST	8	00H	Display start (first COM with active scan pulse, 0 based index)
DEN	8	9FH	Display end (last COM with active scan pulse, 0 based index)
			Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ≥ DEN ≥ DST + 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	8	00H	Window program starting row address. Value range: 0~159.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	8	9FH	Window program ending row address. Value range: 0~159
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command <b>000</b> : <b>Idle</b> 001 : Read 010 : Erase                      011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore <b>1: Use</b>
MTP	7	--	Multiple-Time Programming. For V <sub>LCD</sub> fine tune.
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
<b>Status Registers</b>			
OM	2	-	Operating Modes (Read only) 00b: Reset                      01b: (Not used) 10b: Sleep                      11b: Normal
MD	1	-	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	-	MTP programming in-progress
WS	1	-	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

Note: Please refer to UC1698 data sheet for details

4.3.2 Command Table

The following is the list of host command supported.

	Command	DC	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A	
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A	
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A	
				Ver PMO[6:0]										
				Product Code (8h)				PID[1:0]		MID[1:0]				
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0	
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0	
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0	
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b	
7	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A	
		0	0	#	#	#	#	#	#	#	#			
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0	
		0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0	
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0	
		0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0	
10	Set V <sub>BIAS</sub> Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H	
		0	0	#	#	#	#	#	#	#	#			
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0	
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b	
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0	
		0	0	#	#	#	#	#	#	#	#			
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b	
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0	
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0	
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b	
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0	
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH	
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)	
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b	
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b	
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A	
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A	
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A	
		0	0	#	#	#	#	#	#	#	#			
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12	
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0	
		0	0	-	#	#	#	#	#	#	#			
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		Set WPP0	0
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Shared with MTP commands	Set WPC1	127
		0	0	#	#	#	#	#	#	#	#		Set WPP1	159
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Shared with MTP commands	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		Set WPP1	159
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Shared with MTP commands	Set WPP1	159
		0	0	#	#	#	#	#	#	#	#			
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside	
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H	
		0	0	-	-	-	#	#	#	#	#			
36	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[6:0] MTPM1[1:0]	0	
		0	0	-	#	#	#	#	#	#	#			
37	Set V <sub>MTP1</sub> Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program commands	Set MTP1	N/A
		0	0	#	#	#	#	#	#	#	#			
38	Set V <sub>MTP2</sub> Potentiometer	0	0	1	1	1	1	0	1	0	1	Shared with Window Program commands	Set MTP2	N/A
		0	0	#	#	#	#	#	#	#	#			
39	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0	Shared with Window Program commands	Set MTP3	N/A
		0	0	#	#	#	#	#	#	#	#			
40	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1	Shared with Window Program commands	Set MTP4	N/A
		0	0	#	#	#	#	#	#	#	#			

Note:

Please refer to UC1698 data sheet for details

#### 4.4 Touch screen operating command

Command	/PENIRQ	/CS	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Descriptions
CONTROL REGISTER (*1)	0	0	S	A2	A1	A0	MODE	SER/DER	PD1	PD0	**	S: Start bit ,must be 1 A2-A0: Channel select bit Mode:12 bit/8bit Conversation Selection Bit SER/DFR: Signal –Enable/Differential Reference selection bit PD1-PD0:Power Management Bits

Note:

\*1. Control register set to 90H when panel touched, set to 93H or D3H to read the conversation data.

\*2. For more details, please refer to the datasheet of ADS7843E.

## 5. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping from high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free from twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module