



深圳市拓普微科技开发有限公司

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LM240160BCW-1

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary release	2016-11-01

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1. Basic Specifications

1.1 Display Specifications

- 1) LCD Display Mode : FSTN, Positive, Transflective
- 2) Display Color : Display Data = "1" : Dark Gray (*1)
: Display Data = "0" : Light Gray (*2)
- 3) Viewing Angle : 6H
- 4) Driving Method : 1/160 duty, 1/12 bias
- 5) Back Light : White LED backlight

Note:

*1. Color tone may slightly change by Temperature and Driving Condition.

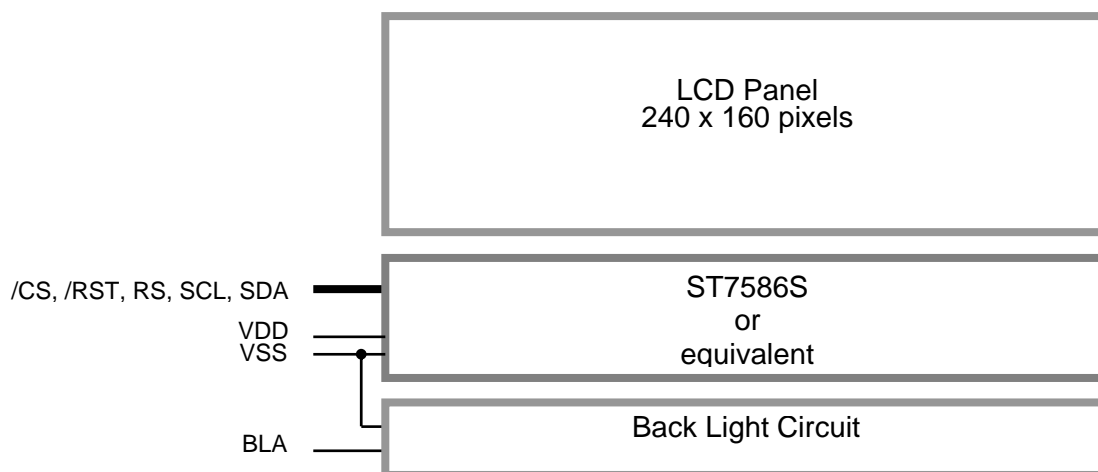
*2. The Color is defined as the inactive / background color

*3. Fine Contrast adjustment function is necessary in the application design for optimal display result

1.2 Mechanical Specifications

- 1) Outline Dimension : 84.5x 71.0x 9.7 MAX. (Except FFC)
(See attached Outline Drawing for details)

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions		
			(4-Line)SPI mode (Default)	8080 mode	6800 mode
1	VDD	Power	Positive Power Supply		
2	VSS	Power	0V Supply, Ground (0V)		
3	/CS	Input	Chip Select /CS=LOW : Data bus is enabled		
4	SCL (RS)	Input	Serial clock input	Register Select RS=HIGH: data on DB0 to DB7 is display data RS=LOW: data on DB0 to DB7 is control data	
5	NC(/WR)	Input	Not used, connect to VDD	/WR=L→H, /RD=H; Data or Instruction latch into the LCD module	R/W=H,E=H; Data or Status read from the LCD module
6	NC(/RD)	Input		/WR=H, /RD=L; Data or Status read form the LCD module	R/W=L,E=H→L; Data or Status latch into the LCD module
7	SDA(DB0)	I/O	Serial data input	8-bit Data bus; Three state I/O terminal for display data or instruction data when /CS=H, DB0~DB7=High Impedance	
8	RS (DB1)		Register Select RS=HIGH: Transferring the Display Data RS=LOW: Transferring the Control Data		
:	:		Not used, connect to VDD		
14	NC(DB7)				
15	/RST	Input	Reset: /RST=LOW: Initialization is executed /RST=HIGH: Normal		
16	BLA	Power	Backlight Positive Power Supply		

1.5 Interface setting:

Setting	4-SPI mode(Default)	8080 mode	6800 mode
JP1	CLOSE	OPEN	OPEN
JP2	OPEN	CLOSE	CLOSE
JP3	CLOSE	CLOSE	OPEN
JP4	OPEN	OPEN	CLOSE
JP5	OPEN	CLOSE	CLOSE
JP6	CLOSE	OPEN	OPEN
JP7~JP14	CLOSE	OPEN	OPEN

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	$V_{SS} = 0V$
Input Voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V	$V_{SS} = 0V$
Operating Temperature	T_{OP}	-30	+85	°C	No Condensation
Storage Temperature	T_{ST}	-40	+90	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	V_{DD}	3.0	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	$0.8 \times V_{DD}$	-	V_{DD}	V	/RST, /CS, RS, SCL, SDA
Input Low Voltage	V_{IL}	0	-	$0.2 \times V_{DD}$	V	
Operating Current	I_{DD}	-	1.3	3.3	mA	VDD

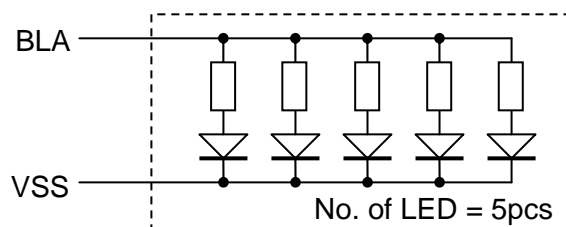
3.2 LED Backlight Circuit Characteristics

$V_{SS}=0V, BLA=3.3V, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	BLA	-	3.3	-	V	BLA
Forward Current	I_{BLA}	-	70	100	mA	BLA

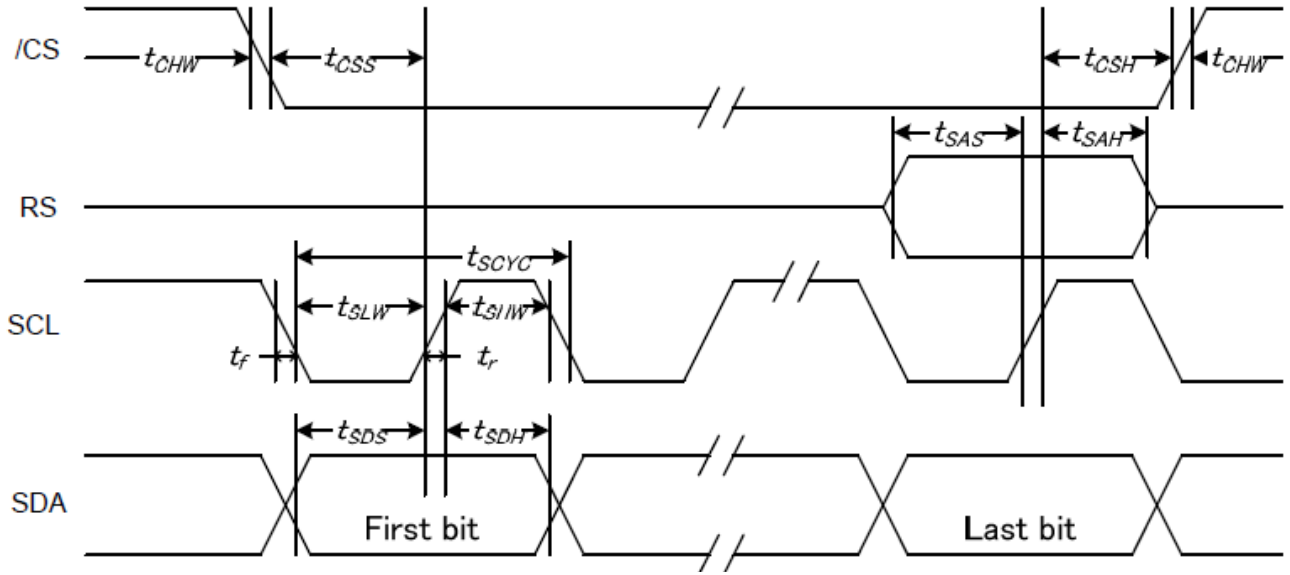
Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



3.3 AC Characteristics

3.3.1 4-Line SPI Mode System Bus Timing(Default)



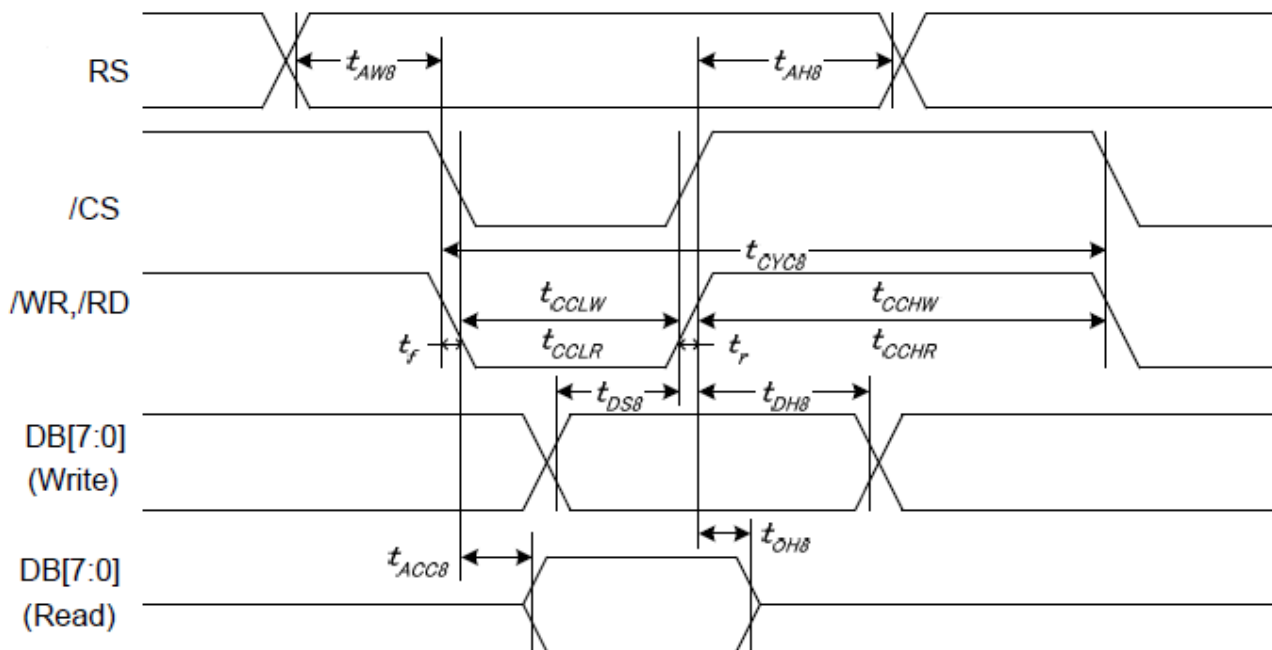
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		143	—	ns
SCL "H" pulse width		tSHW		62	—	
SCL "L" pulse width		tSLW		62	—	
Address setup time	RS	tSAS		28	—	
Address hold time		tSAH		28	—	
Data setup time	SDA	tSDS		28	—	
Data hold time		tSDH		28	—	
/CS-SCL time	/CS	tCSS		28	—	
/CS-SCL time		tCSH		28	—	
/CS "H" pulse width		tCHW		10	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 10 ns or less.
2. Please refer to ST7586S data sheet for details.

3.3.2 8080 Mode System Bus Timing



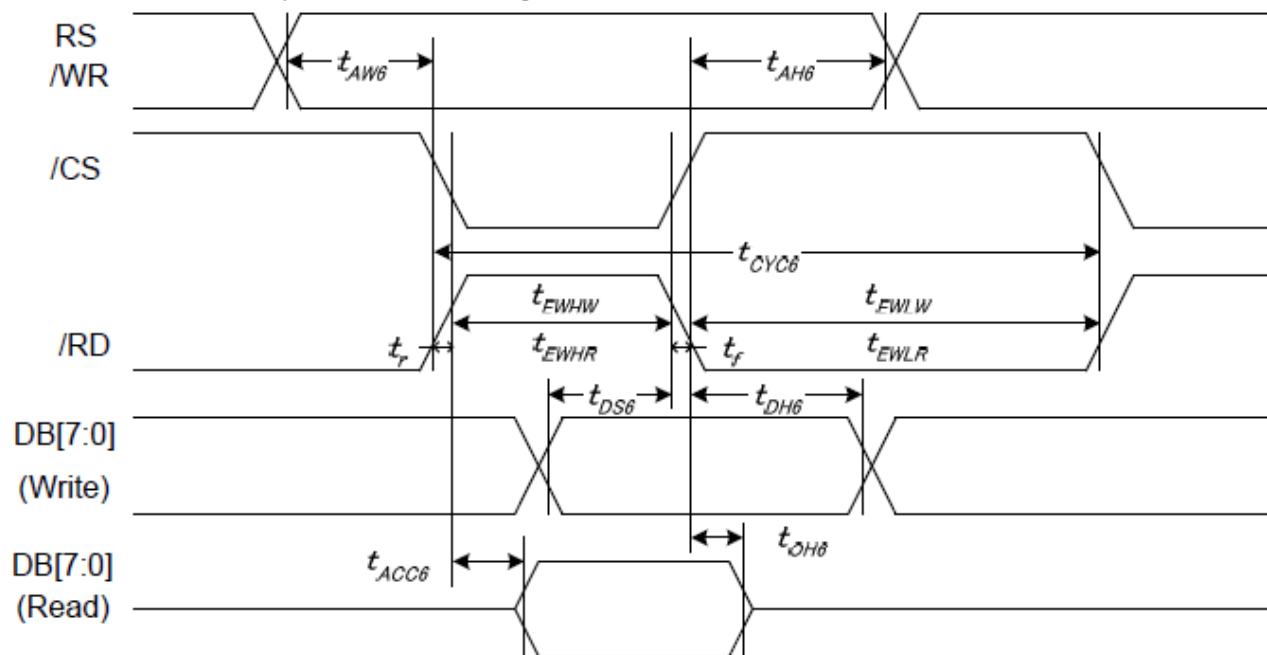
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time tAW8	RS	tAW8		10	—	ns
Address hold time		tAH8		10	—	
System cycle time (WRITE)	/WR	tCYC8		343	—	
/WR L pulse width (WRITE)		tCCLW		143	—	
/WR H pulse width (WRITE)		tCCHW		143	—	
System cycle time (READ)	/RD	tCYC8		714	—	
/RD L pulse width (READ)		tCCLR		314		
/RD H pulse width (READ)		tCCHR		314		
WRITE Data setup time	DB[7:0]	tDS8		28	—	
WRITE Data hold time		tDH8		28	—	
READ access time		tACC8	CL = 30 pF	—	143	
READ Output disable time		tOH8	CL = 30 pF	7	157	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
2. Please refer to ST7586S data sheet for details.

3.3.3 6800 Mode System Bus Timing



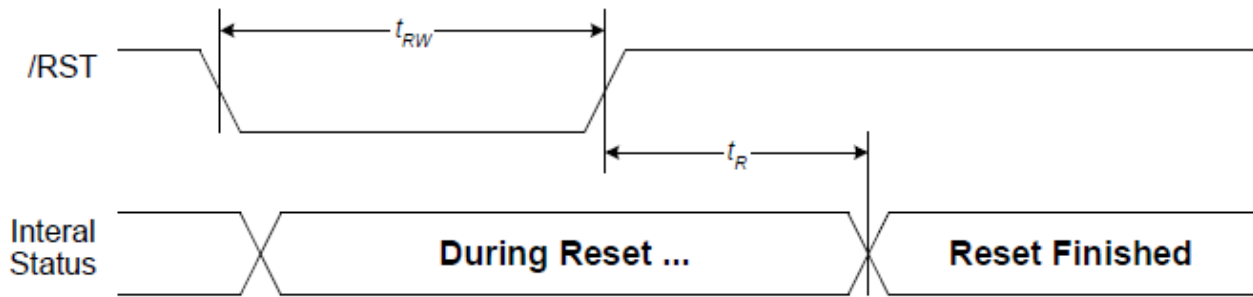
$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Signal	Symbol	Condition	Min.	Max.	Unit	
Address setup time	RS	t_{AW6}		10	—	ns	
Address hold time		t_{AH6}		10	—		
System cycle time (WRITE)	/RD	t_{CYC6}		343	—		
Enable L pulse width (WRITE)		t_{EHLW}		143	—		
Enable H pulse width (WRITE)		t_{EHLW}		143	—		
System cycle time (READ)		t_{CYC6}		714	—		
Enable L pulse width (READ)		t_{EHLR}		314	—		
Enable H pulse width (READ)		t_{EHLR}		314	—		
Write data setup time		DB[7:0]	t_{DS6}		28		—
Write data hold time			t_{DH6}		28		—
Read data access time	t_{ACC6}		CL = 16 pF	—	143		
Read data output disable time	t_{OH6}		CL = 16 pF	7	157		

Note:

1. The input signal rise time and fall time (t_r, t_f) is specified at 10 ns or less.
2. Please refer to ST7586S data sheet for details.

3.4 Reset Timing



VSS=0V, VDD=3.3V, T_{OP}=25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	t _R		171	—	ms
Reset "L" pulse width	t _{RW}		14	—	us

4. Function Specifications

4.1 Adjusting the Display Contrast

This LCD module equipped with latest digital contrast adjustment function.

Its display contrast could be adjusted by MCU command.

(Please see the command tables for details)

It is recommended to provide a contrast adjustment interface for end-user, where the best display result could meet the individual preference in mass production.

4.2 Resetting the LCD module

The LCD module should be initialized by using /RST terminal.

While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level.

After the power supply stabilized, release the reset terminal (/RST=HIGH)

4.3 Display Memory Map

LINE	Column Add (dec)												
	0			1			...	78			79		
	D7, D6	D4, D3	D1, D0	D7, D6	D4, D3	D1, D0		D7, D6	D4, D3	D1, D0	D7, D6	D4, D3	D1, D0
0													
1													
2													
⋮	240x160dot												
157													
158													
159													

Pixel mapping (Top View)

Note:

*1. Based on the top view of the LCD module

*2. The above is memory map based on:

MX[1:0]=11 , MY=1

Inverse Display = Normal

All Pixel ON/OFF =OFF

Display ON/OFF = ON

Partial Mode = OFF

Start Line =0

Display Mode = Monochrome mode

Display Duty = 1/160

*3. 1Byte data in Column Add relate to 3 pixels

*4. please refer to ST7586s datasheet for details and gray scale operation

4.4 Command Table

The following setting should be issue to LCD module after hardware reset.

INSTRUCTION	RS	R/W	COMMAND BYTE								DESCRIPTION
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
NOP	0	0	0	0	0	0	0	0	0	0	No operation
RESET	0	0	0	0	0	0	0	0	0	1	Software reset
Power Save	0	0	0	0	0	1	0	0	0	SLP	Set power save mode SLP=0: Sleep in mode SLP=1: Sleep out mode
Partial Mode	0	0	0	0	0	1	0	0	1	PTL	Set partial mode PTL=0: Partial mode on PTL=1: Partial mode off
Inverse Display	0	0	0	0	1	0	0	0	0	INV	Set inverse display mode INV=0: Normal display INV=1: Inverse display
All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
Display ON/OFF	0	0	0	0	1	0	1	0	0	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
Set Column Address	0	0	0	0	1	0	1	0	1	0	Set column address Starting column address: $00h \leq XS \leq 7Fh$ Ending column address: $XS \leq XE \leq 7Fh$
	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
Set Row Address	0	0	0	0	1	0	1	0	1	1	Set row address Starting row address: $00h \leq YS \leq 9Fh$ Ending row address: $YS \leq YE \leq 9FH$
	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
Write Display Data	0	0	0	0	1	0	1	1	0	0	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Read Display Data	0	0	0	0	1	0	1	1	1	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Display Area	0	0	0	0	1	1	0	0	0	0	Set partial area Partial display address start: $00h \leq PTS \leq 9Fh$ Partial display address end: $00h \leq PTE \leq 9Fh$ Display Area: $64 \leq Duty \leq 160$
	1	0	PTS15	PTS14	PTS13	PTS12	PTS11	PTS10	PTS9	PTS8	
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE15	PTE14	PTE13	PTE12	PTE11	PTE10	PTE9	PTE8	
Scroll Area	0	0	0	0	1	1	0	0	1	1	Set scroll area Top Area: TA=00h~A0h Scrolling Area: SA=00h~A0h Bottom Area: BA=00h~A0h TA+SA+BA=160
	1	0	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	1	0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
Display Control	0	0	0	0	1	1	0	1	1	0	Set scan direction of COM and SEG MY=0: COM0→COM159 MY=1: COM159→COOM0 MX[1:0]=(0,0): SEG0→SEG383 MX[1:0]=(1,1): SEG383→SEG0
	1	0	MY	MX1	0	0	MX0	0	0	0	
Start Line	0	0	0	0	1	1	0	1	1	1	Set display start line S=00h~9Fh
	1	0	S7	S6	S5	S4	S3	S2	S1	S0	

Command Table (continue)

INSTRUCTION	RS	R/W	COMMAND BYTE								DESCRIPTION
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display Mode	0	0	0	0	1	1	1	0	0	M	Set display mode M=0: Gray mode M=1: Monochrome mode
Enable DDRAM Interface	0	0	0	0	1	1	1	0	1	0	Enable DDRAM interface
	1	0	0	0	0	0	0	0	1	0	
Display Duty	0	0	1	0	1	1	0	0	0	0	Set display duty DT=03h~9Fh
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
First Output COM	0	0	1	0	1	1	0	0	0	1	Set first output COM FC=00h~9Fh
	1	0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	
FOSC Divider	0	0	1	0	1	1	0	0	1	1	Set FOSC dividing ratio
	1	0	0	0	0	0	0	0	FOD1	FOD0	
Partial Display	0	0	1	0	1	1	0	1	0	0	Set partial display mode
	1	0	1	0	1	0	0	0	0	0	
N-Line Inversion	0	0	1	0	1	1	0	1	0	1	Set N-Line inversion
	1	0	M	0	0	NL4	NL3	NL2	NL1	NL0	
Read Modify Write	0	0	1	0	1	1	1	0	0	RMW	Read modify write control RMW=0: Enable read modify write RMW=1: Disable read modify write
Set Vop	0	0	1	1	0	0	0	0	0	0	Set Vop
	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	-	-	-	-	-	-	-	Vop8	
Vop Increase	0	0	1	1	0	0	0	0	0	1	Vop increase one step
Vop Decrease	0	0	1	1	0	0	0	0	1	0	Vop decrease one step
BIAS System	0	0	1	1	0	0	0	0	1	1	Set BIAS system
	1	0	-	-	-	-	-	BS2	BS1	BS0	
Booster Level	0	0	1	1	0	0	0	1	0	0	Set booster level
	1	0	-	-	-	-	-	BST2	BST1	BST0	
Vop Offset	0	0	1	1	0	0	0	1	1	1	Set Vop offset
	1	0	0	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
Analog Control	0	0	1	1	0	1	0	0	0	0	Enable analog circuit
	1	0	0	0	0	1	1	1	0	1	
Auto Read Control	0	0	1	1	0	1	0	1	1	1	Auto read control XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	

Note:

Please refer to ST7586S data sheet for details

5. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping from high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free from twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module