National Semiconductor

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LM2433
220V Monolithic Single Channel 16 MHz EDTV CRT Driver

General Description

The LM2433 is a single channel high voltage CRT driver circuit designed for use in Rear-Projection and Direct-View EDTV applications. The IC contains a high input impedance, wide band amplifier which can be DC coupled to a cathode of a CRT. The amplifier has its gain internally set to –53 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

The IC is packaged in a staggered 7-lead TO-220 molded plastic power package designed specifically to meet high voltage spacing requirements. See the section "Power Dissipation and Heatsink Calculation" for more information.

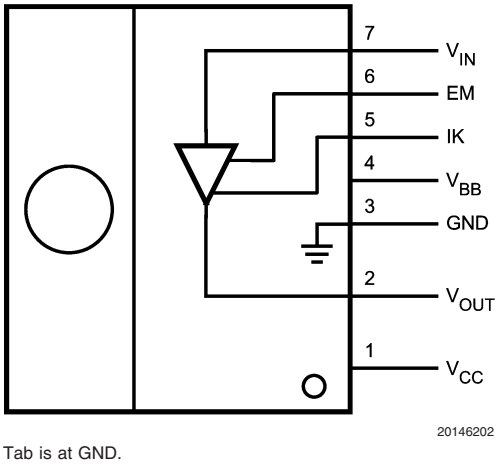
Features

- 16 MHz bandwith at $110V_{PP}$ output swing
- 0V to 4V input range
- Greater than $110V_{PP}$ output swing capability
- IK Current Output (pin 5) for IK feedback systems
- Emitter (pin 6) access to increase voltage gain

Applications

- For Rear-Projection and Direct-View DC coupled CRT applications using EDTV formats
- Compatible with RGB video processors with IK feedback for automatic cathode calibration

Pinout Diagram



Note: Tab is at GND.

Top View
Order Number LM2433TE

FIGURE 1. Simplified Connection and Pinout Diagram

Schematic Diagram

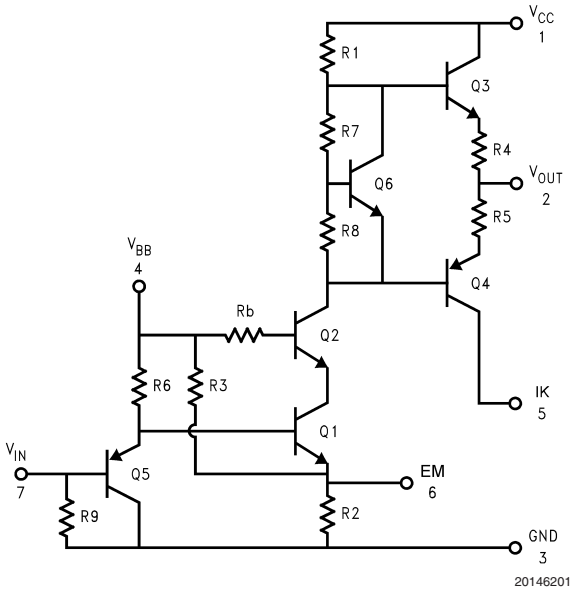


FIGURE 2. Simplified Schematic Diagram

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	+250V
Bias Voltage (V_{BB})	+16V
Input Voltage (V_{IN})	-0.5V to V_{BB}+0.5V
IK Voltage (V_{IK})	-0.5V to +16V
Storage Temperature Range (T_{STG})	-65˚C to +150˚C
Lead Temperature	
(Soldering, <10 sec.)	300˚C
ESD Tolerance,	
Human Body Model	2 kV
Machine Model	200V
Junction Temperature	150˚C
θ_{JC} (typ)	4.5˚C/W

Operating Ranges (Note 2)

V_{CC}	+130V to +230V
V_{BB}	+7V to +13V
V_{IN}	0V to +4.25V
V_{IK}	0V to V_{BB}+1V
V_{OUT}	+45V to V_{CC}–5V
Case Temperature	See *Figure 10*. Derate power for T_C above 110˚C.

Do not operate the part without a heat sink.

Electrical Characteristics (See *Figure 3* for Test Circuit)

Unless otherwise noted: V_{CC} = +220V, V_{BB} = +12V, C_L = 10 pF, T_C = 40˚C, pin 6 floating (R_{EM} = open).
DC Tests: $V_{IN} = 2.75V_{DC}$
AC Tests: Output = $110V_{PP}$ (80V - 190V) at 1 MHz

Symbol	Parameter	Conditions	LM2433			Units
			Min	Typical	Max	
I_{CC}	Supply Current	No AC Input Signal, No Output Load		12	17	mA
I_{BB}	Bias Current			8	11	mA
$V_{OUT, 1}$	DC Output Voltage	No AC Input Signal, $V_{IN} = 2.75V_{DC}$	121	125	131	V_{DC}
$V_{OUT, 2}$	DC Output Voltage	No AC Input Signal, $V_{IN} = 1.25V_{DC}$	199	204	209	V_{DC}
A_V	DC Voltage Gain	No AC Input Signal	–50	–53	–56	
LE	Linearity Error	(Note 4), No AC Input Signal		5		%
t_R	Rise Time	(Note 5), 10% to 90%		23		ns
+OS	Overshoot	(Note 5)		0		%
t_F	Fall Time	(Note 5), 90% to 10%		24		ns
–OS	Overshoot	(Note 5)		0		%
IK_{ERROR}	IK Current Output Error	(Notes 6, 7), V_{CC} = 210V, V_{OUT} = $150V_{DC}$		–5		µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

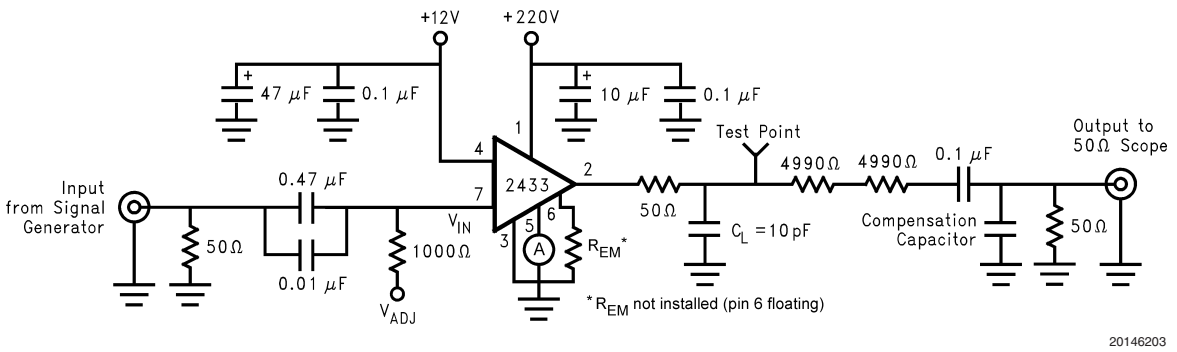
Note 4: Linearity Error is the variation in DC gain from V_{IN} = 1.15V to V_{IN} = 4.35V.

Note 5: Input from signal generator: t_r, t_f < 2 ns. Slower inputs to the LM2433 will change the transient response and reduce power dissipation.

Note 6: $IK_{ERROR} = I_K - I_{OUT}$, where I_K is the IK current output from pin 5 (IK) and I_{OUT} is the cathode current into pin 2 (V_{OUT}). I_K can be measured with a precision ammeter or calculated by measuring V_{IK} across a known resistor value between pin 5 and GND. Refer to the "Cathode Current Output for IK Feedback Systems" section for more information.

Note 7: Refer to the RGB Video Processor data sheet for IK leakage compensation, feedback operation, and adjustment range information.

AC Test Circuit



Note: 10pF load includes parasitic capacitance.

FIGURE 3. Test Circuit

Figure 3 shows a typical test circuit for evaluation of the LM2433. This circuit was designed to test the transient response of the LM2433 in a 50Ω environment without the use of an expensive FET probe. On the input side, a 50Ω pulse generator output can be AC coupled and biased with an external supply via the V_{ADJ} input. On the output side, the two 4990Ω resistors form a 400:1 divider with the 50Ω resistor and the oscilloscope. A test point can be included for easy use of an oscilloscope probe. A compensation capacitor can be used to compensate the network to achieve a flat frequency response.

Typical Performance Characteristics (V_{CC} = +220V, V_{BB} = +12V, C_L = 10 pF, V_{OUT} = 110V_{PP} (80V – 190V), pin 6 floating, Test Circuit - *Figure 3*, unless otherwise specified)

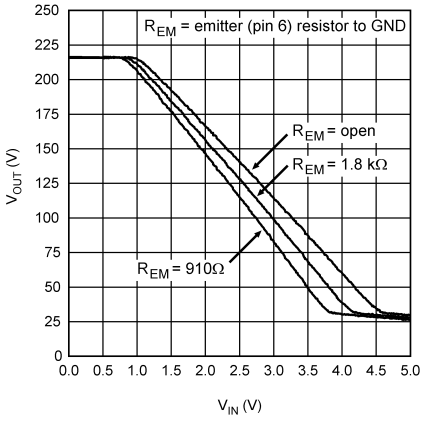


FIGURE 4. V_{OUT} vs V_{IN}

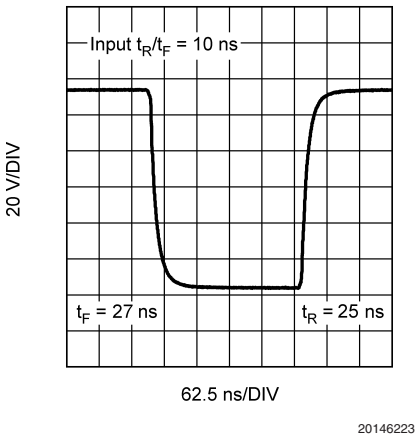


FIGURE 5. LM2433 Pulse Response

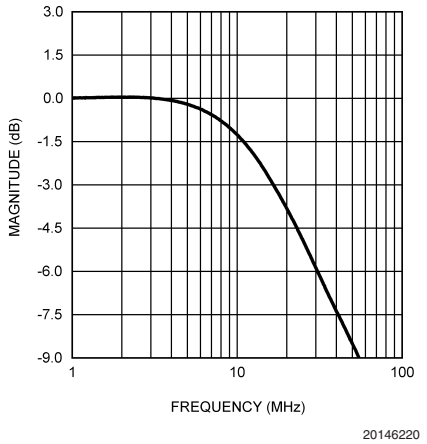


FIGURE 6. Bandwidth

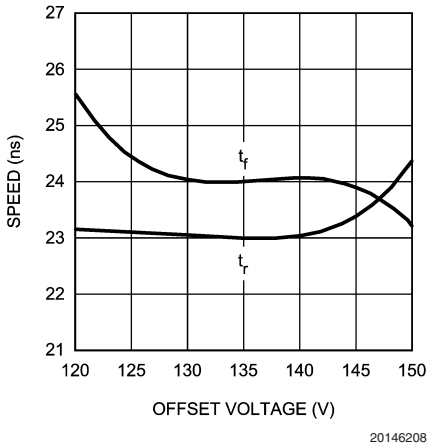


FIGURE 7. Speed vs Offset

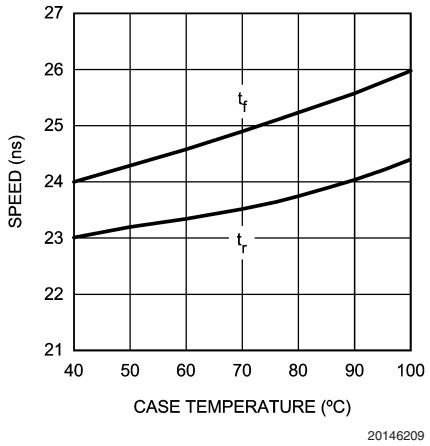


FIGURE 8. Speed vs Case Temperature

Typical Performance Characteristics (V_{CC} = +220V, V_{BB} = +12V, C_L = 10 pF, V_{OUT} = 110V_{PP} (80V – 190V), pin 6 floating, Test Circuit - *Figure 3*, unless otherwise specified) (Continued)

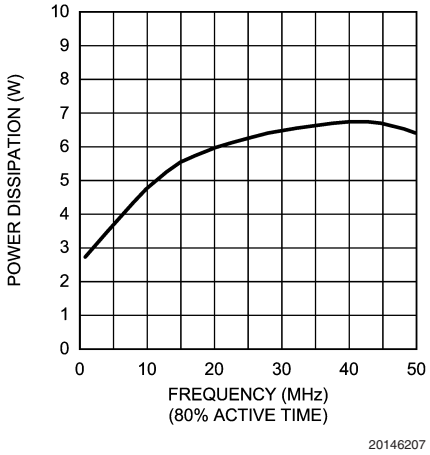


FIGURE 9. Power Dissipation vs Frequency

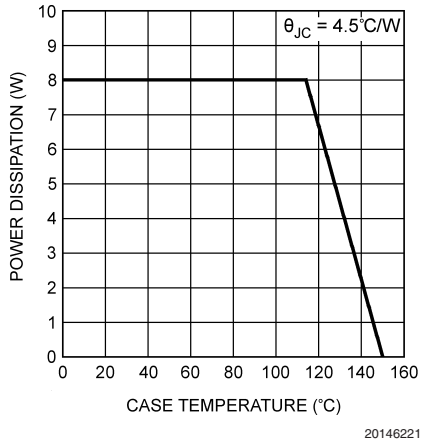


FIGURE 10. Power Derating Curve

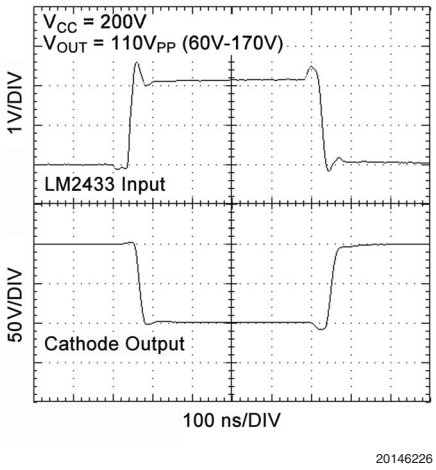


FIGURE 11. Cathode Pulse Response

Theory of Operation

The LM2433 is a high voltage monolithic single channel CRT driver suitable for EDTV applications. The LM2433 typically operates with +220V and +12V power supplies. The part is housed in a staggered 7-lead TO-220 molded plastic power package.

The circuit diagram of the LM2433 is shown in *Figure 2*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at −53. Emitter followers Q3 and Q4 isolate the high output impedance of the cascode stage from the capacitance of the CRT cathode which decreases the sensitivity of the device to load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels.

The emitter of Q1 is accessible via pin 6 and enables a higher voltage gain, if needed. The gain improvement can be helpful in applications where a channel's gain needs to be increased to compensate for a limited preamplifier drive register adjustment. An external resistor, R_{EM}, can be connected between pin 6 and GND, so it's in parallel with internal emitter resistor, R2. A properly chosen resistor will decrease the total emitter resistance to produce a higher voltage gain. *Figure 4* shows typical transfer curves for various values of R_{EM}. To determine the value of R_{EM} for the new voltage gain, A_V', use the following approximation: $R_{EM} = 10.6 / (|A_V'| - 53)$, where R_{EM} is in kΩ. If the application does not require higher gain, then pin 6 should be left floating.

The LM2433 has an IK current output (pin 5) that produces a replica of the actual cathode current into V_{OUT} (pin 2). The IK output pin is internally connected to the collector of Q4. The IK output can be connected through an interface circuit to a RGB video processor with IK feedback for automatic cathode calibration. **Note:** During the non-blanking period, video current levels can be as high as several mA, which is much higher than the reference currents (in µA range) produced during the IK measurement interval. These high currents have the potential to produce large voltages at the IK output pin. To avoid damage to Q4, the IK output pin should be protected with a clamp diode to V_{BB} so it's voltage, V_{IK}, does not exceed +16V ($V_{IK_{MAX}}$). Please see the section "Cathode Current Output for IK Feedback Systems" for more information on the usage and protection of the IK output. If the IK output is not used in the application, it should be connected to the same ground as pin 3 (GND).

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2433 performance is targeted for the EDTV market. The application circuits shown in this document to optimize performance and to protect against damage from CRT arcover are designed specifically for the LM2433. If another member of NSC's DTV CRT Driver family is used, please refer to its data sheet.

POWER SUPPLY BYPASS

Since the LM2433 is a wide bandwidth amplifier, proper power supply bypassing is critical for optimum performance and for robustness against arcover. Improper power supply bypassing can result in large overshoot, ringing or oscillation, and even arcover failure. 0.1 µF capacitors should be connected from the supply pins, V_{CC} and V_{BB}, to ground using very short traces. Additionally, a 10 µF or larger electrolytic capacitor should be connected from both supply pins to ground reasonably close to the LM2433.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. This fast, high voltage, high energy pulse can damage the LM2433 output stage since it is DC coupled to the cathode. In a DC coupled application, an external spark gap with an arcover voltage rating of 200 to 300V_{DC} on the cathode is NOT recommended. The internal CRT socket spark gap (1 to 2 kV_{DC} rating) can sufficiently reduce the initial arcover voltage seen at the cathode. The output circuit shown in *Figure 12* is designed to help clamp the voltage at the output of the LM2433 to a safe level during an arcover.

External arc protection clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. 1SS83 or equivalent diodes like BAV21 are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should have a very short connection to a separate V_{CC} bypass capacitor, C3. The ground connection of D2 and the C3 should have a short, direct path to ground. This will significantly reduce the high frequency voltage transients that the LM2433 would be subjected to during an arcover.

Resistor R2, which limits the arcover current that is seen by the diodes, should be a ½W solid carbon type resistor. R1 limits the current into the LM2433 as well as the voltage stress at the outputs of the device and can be a ¼W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2433 would be subjected to. The inductor will not only help protect the device but it will also help minimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 12*.

Application Hints (Continued)

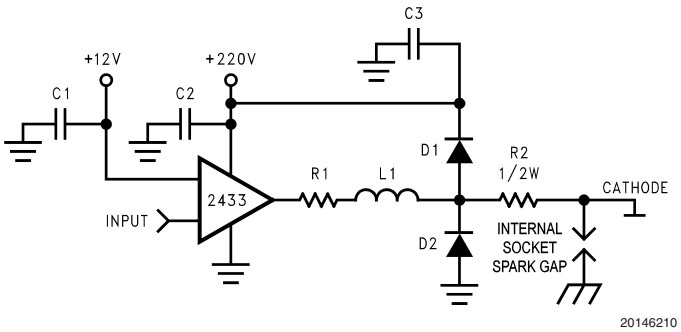


FIGURE 12. Recommended Application Circuit

EFFECT OF OFFSET

Figure 7 shows the variation in rise and fall times when the DC offset of the $110V_{PP}$ output swing is varied between 120V and $150V_{DC}$. The rise time and fall time show a maximum variation of about 6% relative to the center data point ($135V_{DC}$), which is a relatively small variation in speed over the 30V DC offset range.

THERMAL CONSIDERATIONS

Figure 8 shows the performance of the LM2433 as a function of case temperature. The figure shows that the rise and fall times of the LM2433 increase by approximately 4.5% and 6.5%, respectively, as the case temperature increases from 40˚C to 90˚C. This corresponds to a speed degradation of about 0.9% and 1.3% for every 10˚C rise in case temperature, which is very stable performance over the temperature range.

POWER DISSIPATION AND HEATSINK CALCULATION

Worst-Case Power Dissipation

Figure 9 shows the maximum power dissipation of the LM2433 vs. square wave frequency when the device uses V_{CC} of 220V and is driving a 10 pF load with $110V_{PP}$ swing alternating one pixel on, one pixel off signal. Note that the frequency range shown in the power dissipation figure is one-half the actual pixel frequency. The graph assumes 80% active time (device operating at the specified frequency), which is typical in an EDTV application. The other 20% of the time the device is assumed to be sitting at the black level (190V in this case). Under this worst-case condition, the maximum power dissipated by the LM2433 is about 6.8W at around 40 MHz. It is important to note that this power dissipation is a result of a high frequency square wave input, which is unrealistic in practical TV applications. The bandwidth of the input source used to drive the LM2433 was over 300 MHz. Using a RGB video processor or preamplifier with less bandwidth will cause the LM2433 to dissipate less power than shown in *Figure 9* at the same conditions.

A Practical Approach to Power Dissipation

The power curve (*Figure 9*) mentioned previously shows the LM2433 power dissipation for square wave frequencies ranging from 1 to 50 MHz at $110V_{PP}$ swing. In practice, it is uncommon for a TV to display average frequency content over the entire picture exceeding 20 MHz. Therefore, it is important to establish the worst-case picture condition under normal viewing to give a realistic maximum power dissipation for the LM2433. Here is one approach:

An EDTV signal generator pattern that yields a practical worst-case picture condition is a “multi-burst” pattern that consists of a 1-to-30 MHz sine wave sweep over each of the active lines. The power dissipated by the LM2433 as a result of this picture condition can be approximated by taking the average of the power between 1 to 30 MHz in *Figure 9*. This average is 5.1W. Because a square wave input was used to generate this power curve, a sine wave would cause the LM2433 to dissipate slightly less power, say 5.0W. This is one common way to determine a practical figure for maximum power dissipation. It is the system designer’s responsibility to establish the worst-case picture condition for his particular application and measure dissipation under that condition to choose a proper heatsink.

Heatsink Calculation Example

Once the maximum dissipation is known, *Figure 10* can be used to determine the heatsink requirement for the LM2433. If the 1-to-30 MHz multi-burst test described previously is assumed to be worst-case picture condition that yields maximum dissipation, then the LM2433 will dissipate about 5.0W. The power derating curve shows that the maximum allowed case temperature is 127.5˚C when 5.0W is dissipated. If the maximum expected ambient temperature is 65˚C, then the maximum thermal resistance from device case-to-air (θ_{CA}) can be calculated:

$$\theta_{CA} = (T_{C_{MAX}} - T_{A_{MAX}}) / P_{D_{MAX}} = \theta_{CS} + \theta_{SA}$$

$$\theta_{CA} = (127.5^{\circ}C - 65^{\circ}C) / 5.0W = 12.5^{\circ}C/W.$$

θ_{CS} is the thermal resistance of the thermal compound at the case-to-heatsink interface and θ_{SA} is the thermal resistance of the heatsink at the rated conditions.

This example assumes a capacitive load of 10 pF and no resistive load. The designer should note that if the V_{CC} supply voltage, output swing, input bandwidth, or load capacitance is increased, then the power dissipation will also increase.

Application Hints (Continued)

Tips for Reducing Power Dissipation

The following methods can be used to reduce the power dissipated by the LM2433 in order to optimize heatsink size and cost:

- Use a lower V_{CC} supply voltage while maintaining sufficient operating range for cutoff, brightness, and drive adjustments.
- Lower the maximum V_{PP} swing while maintaining acceptable picture contrast and brightness.
- Reduce the input bandwidth to the LM2433 while maintaining acceptable picture performance.
- Minimize capacitive load on the LM2433 output by using good PCB layout practices.

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 12*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR_ _k) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 15* can be used as a good starting point for the evaluation of the LM2433. Using a variable resistor for R1 will simplify finding the value needed for optimum performance in a given application. Once the optimum value is determined, the variable resistor can be replaced with a fixed value.

Figure 11 shows a typical cathode pulse response with an output swing of $110V_{PP}$ using a RGB video processor that provides input speeds with 12 ns rise and fall times. **Note:** The RGB processor's sharpness feature adds emphasis (pre-shoot and over-shoot) to the rising and falling edges of the input pulse, which consequently adds emphasis to the cathode pulse response.

CATHODE CURRENT OUTPUT FOR IK FEEDBACK SYSTEMS

IK Feedback Systems

IK feedback was developed to accurately bias the CRT and continuously calibrate it to the correct cut-off and/or drive levels over the useful life of the CRT. RGB video processors that use IK feedback to automatically adjust only cut-off, or black level, are realized by a 1-point calibration system. A few trade names for this system are Auto Kine Bias (AKB) and Black Current Stabilization (BCS). RGB processors that can automatically adjust both cut-off and drive, or white level, are realized by a 2-point calibration system. This is commonly known as Continuous Cathode Calibration (CCC). For convenience, some 2-point RGB processors may be programmed to 1-point operation if drive calibration is not required. The LM2433 is compatible with both 1- and 2-point systems.

To be compatible with various RGB processors, an interface circuit may be needed in the feedback path between the LM2433 IK output and the processor's IK input. This feedback circuit depends on the RGB processor and feedback topology (voltage or current) used. Because each processor has its own IK input signal and topology requirements, it is outside the scope of this data sheet to describe each feedback circuit in detail. For more information, please refer to the RGB processor data sheet or contact your local National Semiconductor Sales Office with your specific application requirements.

Feedback Topologies

RGB processors that use **voltage feedback** require the LM2433 IK current to be converted to voltage via a resistor (R_{IK}) to ground. This IK voltage, V_{IK}, will be fed back to the IK input of the RGB processor through an interface circuit, which will be AC or DC coupled depending on the processor's IK input requirement. For proper feedback operation, some processors may require an emitter follower to isolate the IK input from the high impedance of the resistor. During the closed-loop IK measurement interval, the IK input voltage will be sampled and compared with the processor's internal reference voltage to automatically calibrate the video levels for the next field. The value of R_{IK} is crucial, since it establishes the IK voltage and consequently, the operating point of the CRT. Once a stable operating point is established with a properly chosen resistor, this point can be fine-tuned using the adjustment range of the processor's RGB cut-off and/or gain controls via the I^2C-bus. After the IK measurement interval (usually at the end of blanking), normal video will resume and high currents will flow out of the IK output. These high video currents will produce large IK voltages across the resistor that can exceed the maximum voltage rating for V_{IK}. Therefore, it is recommended to use a high-speed diode (D_{PROT}) to clamp the LM2433 IK output to a safe level (preferably V_{BB} or a lower supply). If a zener diode is used instead, it may be necessary for the RGB processor to have IK leakage compensation for the leakage current attributed to the zener. Lastly, it is possible to use a single R_{IK} resistor to set the IK voltage for all three LM2433s. See a simplified voltage feedback interface circuit in *Figure 13*.

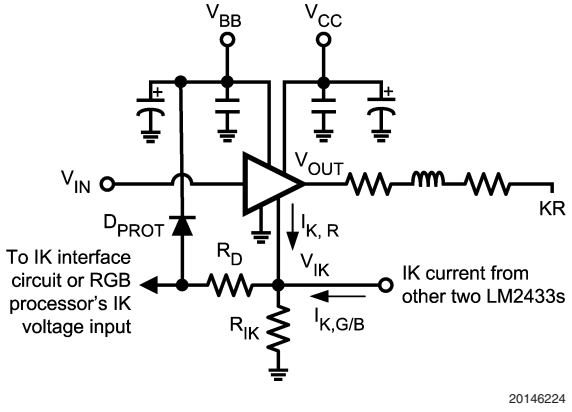


FIGURE 13. Simplified IK Interface for Voltage Feedback Systems

RGB processors that use **current feedback** do not require voltage conversion. The LM2433 IK current can be fed back directly to the IK input of the RGB processor, although some protection circuitry will be needed to protect the RGB processor and LM2433. During the closed-loop IK measurement interval, the voltage of the RGB processor's IK pin will be internally clamped, and the IK current will be sampled and compared with the processor's internal reference current to calibrate the video levels. The operating point of the CRT can be fine-tuned using the adjustment range of the processor's RGB cut-off and/or gain controls via the I^2C-bus. When

Application Hints (Continued)

normal video resumes, a protection element should shunt high video current away from the IK input of the RGB processor. Since the processor's IK pin is not clamped during normal video, V_{IK} of the LM2433 must not exceed +16V ($V_{IK_{MAX}}$). A properly chosen high speed, low-leakage zener diode (D_{PROT}) can be used to protect both the RGB processor input and LM2433 IK output in this case. Again, it may be necessary for the RGB processor to have IK leakage compensation for the leakage current attributed to the zener. See a simplified current feedback interface circuit in *Figure 14*.

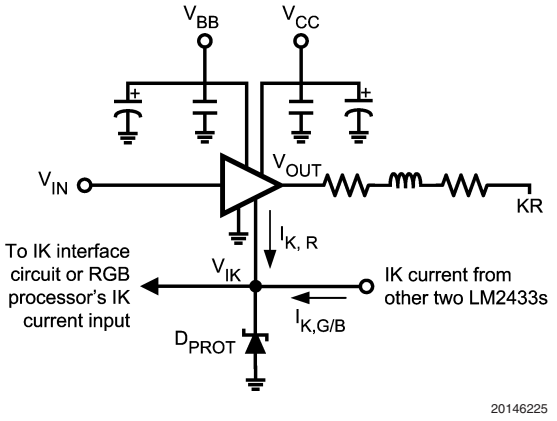


FIGURE 14. Simplified IK Interface for Current Feedback Systems

LM2433 IK Output and Protection Requirements

The LM2433 IK output sources a copy of the actual cathode current to the interface circuit during the closed-loop IK measurement interval and during normal video when the IK feedback loop is opened. Because the cathode current during normal video is much higher than the low current being measured during the measurement interval, V_{IK} may exceed it's maximum rating. To protect and prevent improper operation of the LM2433, V_{IK} must be maintained within the range specified in the *Section Operating Ranges* .

For voltage feedback topologies, it is recommended to use a high-speed diode to clamp the IK voltage to V_{BB} or a lower supply during normal video. A small series resistor (R_D in *Figure 13*) can be placed at the IK pin to limit the current through the diode when clamping. See the NSC Demonstration Board for an example. For current feedback topologies, it is recommended to use a high-speed, low-leakage zener diode to clamp V_{IK} to a properly chosen zener voltage and shunt the high video current away from the RGB processor's IK input. The zener voltage should be higher than the clamping voltage of the processor's IK pin and lower than the maximum voltage rating of either the processor's IK pin or LM2433 V_{IK}, whichever is the less.

In a Direct-View TV application with a single neck PCB, it is possible for the three LM2433 IK outputs to share the one feedback circuit and protection diode by connecting the IK pins together on the neck PCB. This will reduce component count. In a Rear-Projection TV application with three neck PCBs, the IK pins can be connected on the central neck PCB or the RGB processor mainboard through cabling. This way, they can share the interface circuit to feed back the IK voltage or current signal to the RGB processor. However, each LM2433 IK output should have its own protection diode on its PCB.

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2433 and from the LM2433 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a TV if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

TYPICAL APPLICATION

The high bandwidth, large swing capability, and simple application make the LM2433 ideal for Rear-Projection and Direct-View EDTV CRT applications. The IK output can be made compatible with any RGB video processor with IK feedback. If the IK output is not used in the application, it should be connected to the same ground as pin 3 (GND). See the section "Cathode Current Output for IK Feedback Systems" for more information.

NSC DEMONSTRATION BOARD

Figure 15 and *Figure 16* show the schematic and PCB layout for the NSC demonstration neck board for a typical Rear-Projection EDTV application with IK feedback. This single channel neck board could be used for all three channels, since each neck board receives video-related signals directly from the RGB mainboard. The power supplies are daisy-chained between each channel using inboard and outboard connectors J6 and J7. This board provides a good example of a layout that can be used as a guide for future layouts. Samples of the NSC demonstration neck board are available upon request to your local National Semiconductor Sales Office.

Input Video Interface

On the RGB mainboard, the video output of the RGB processor is buffered with a PNP transistor to drive the video through flat cabling to the NSC neck board. The cabling from the mainboard plugs into the neck board at connector J8 to supply it with video, IK, GND, and other signals. Between the video input (pin 3) of J8 and V_{IN} (pin 7) of the LM2433 is another buffer stage consisting of two NPN transistors. Both NPN transistors drop the video levels from the preceding PNP buffer by a total of two V_{BE}. This shifts the nominal input black level such that the LM2433 output (or cathode) black level voltage is near the nominal cut-off voltage of the CRT. The overall voltage shift from the processor output to the LM2433 input is one V_{BE} drop. **Note:** The same video level shifting could have been accomplished using one NPN buffer on the RGB mainboard to drive the processor's video output through cabling directly to the LM2433 input. However, it was decided to preserve the TV's original RGB mainboard circuitry (the PNP buffer) and use two NPN transistors on the neck board.

Application Hints (Continued)

The input stage from the RGB processor to the LM2433 will be determined by the system designer for his specific application. The input stage required depends mainly on the following system parameters:

- Nominal CRT cut-off voltage
- Nominal black level output voltage of the RGB processor
- V_{CC} & V_{BB} supply voltages of the LM2433

Once the nominal black level input to the LM2433 establishes a cathode black level near the CRT cut-off voltage, it can be fine-tuned using the processor's cut-off adjustment and calibrated automatically using the IK feedback system, if applicable. Lastly, some RGB processor video outputs cannot adequately drive the capacitive load introduced by the cabling between the RGB mainboard and neck boards. To prevent loading the processor's output, a NPN or PNP buffer stage can be applied close to the output on the mainboard to sufficiently drive the video signal through cabling to the neck board. It is important to bias the buffer stage(s) properly to obtain optimal video performance and maintain the full video adjustment range of the RGB processor.

Video Output and Arc Protection

The routing of the LM2433 output to the CRT is very critical to achieve optimal video performance and robustness against arcover. *Figure 16* shows the routing and component placement from V_{OUT} (pin 2) of the LM2433 to the cathode pin of the CRT socket. The components are placed so that there is a short, direct path from the LM2433 output to the cathode. This is done to reduce the PCB parasitic capacitance on the LM2433 output and minimize EMI. Note also that L3, D3, D4, and R6 are placed to minimize the size of the video nodes that they are attached to. This enhances the effectiveness of the arc protection diodes. The anode of protection diode D3 is connected directly to a section of the ground plane that has a short, direct path to the LM2433 ground plane. The cathode of D4 is connected to V_{CC} very close to decoupling capacitor C7, which is connected to the same section of the ground plane as D3. The diode placement and routing is very important to shunt arcover current away from the output and minimize the voltage stress on the LM2433. The internal CRT socket spark gap will serve to significantly reduce the initial arcover voltage seen at the cathode. The DAG connector should be connected to CRT ground for arc return current.

IK Feedback Circuit

The NSC demonstration neck board was made so that no modifications to the existing TV circuitry were necessary (except for replacing the original neck boards). Therefore, the video interface and IK feedback circuits are designed to be compatible with those original TV circuits. Referring to *Figure 15*, the LM2433 IK output (pin 5) is connected to protection circuitry before the IK current signal is routed to pin 4 of connector J8. Diode D1 protects the LM2433 IK pin from excessive voltage during normal video by clamping to the V_{BB} supply. Diode D2 isolates the IK output from the other channels during the active IK measurement interval. Resistors R17 and R12 limit the current through D1 and D2, and C12 is used for filtering. From connector J8, the IK current signal is passed through cabling and combined with the other two IK signals on the RGB mainboard.

Note: The following paragraph describes circuitry that is not part of the NSC demonstration neck board. The RGB processor, which operates with a voltage feedback IK topology, uses a single "IK resistor" on the RGB mainboard to convert all three IK currents into a voltage signal. The IK voltage signal is then buffered through a PNP transistor before it is filtered and AC coupled to the RGB processor's IK input. This is one implementation of the IK feedback circuit based on this TV's specific RGB processor. The system designer should refer to the RGB processor data sheet to determine the appropriate feedback circuit implementation for his application.

Supply Decoupling

Note the location of the following components:

- C5—V_{CC} bypass capacitor with short traces to the V_{CC} and GND pins of LM2433.
- C7—V_{CC} bypass capacitor with short traces to the V_{CC} arc protection diode and ground. This capacitor is very important for arc protection.
- C9—V_{BB} bypass capacitor with short traces to the V_{BB} and GND pins.
- C10 and C11—V_{CC} and V_{BB} electrolytic capacitors placed near supply pins of LM2433.

Other Items

Connector J1 and switches JP2 & JP4 can be used to bypass the TV's internal 200V and 12V supplies and evaluate the LM2433 with external V_{CC} and V_{BB} supplies. Also, this demonstration board uses medium-sized PCB holes to accommodate socket pins, which function to allow for multiple insertions of the LM2433 in a convenient manner. To benefit from the enhanced LM2433 package with thin leads, the device should be secured with solder in small PCB holes to optimize the metal-to-metal spacing between the leads.

Application Hints (Continued)

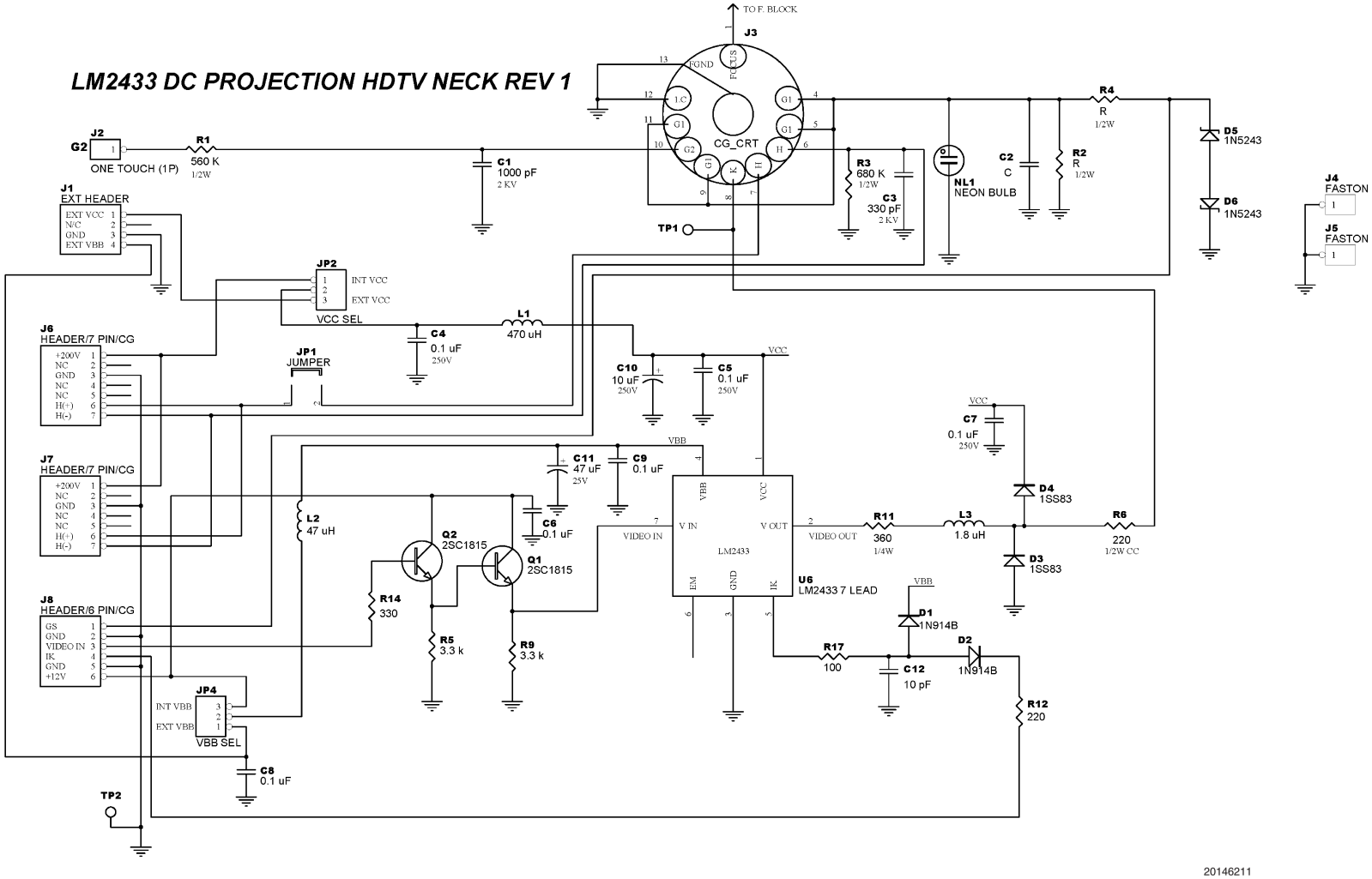


FIGURE 15. LM2433 Demonstration Board Schematic

Application Hints (Continued)

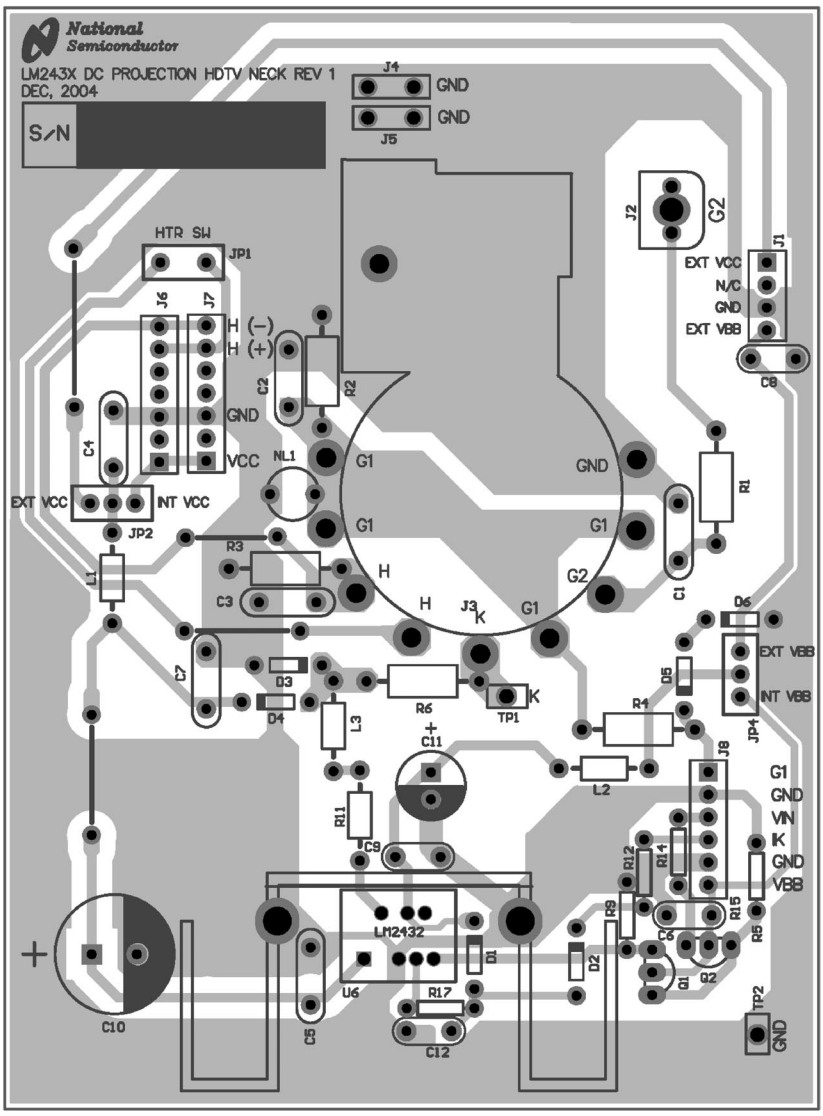


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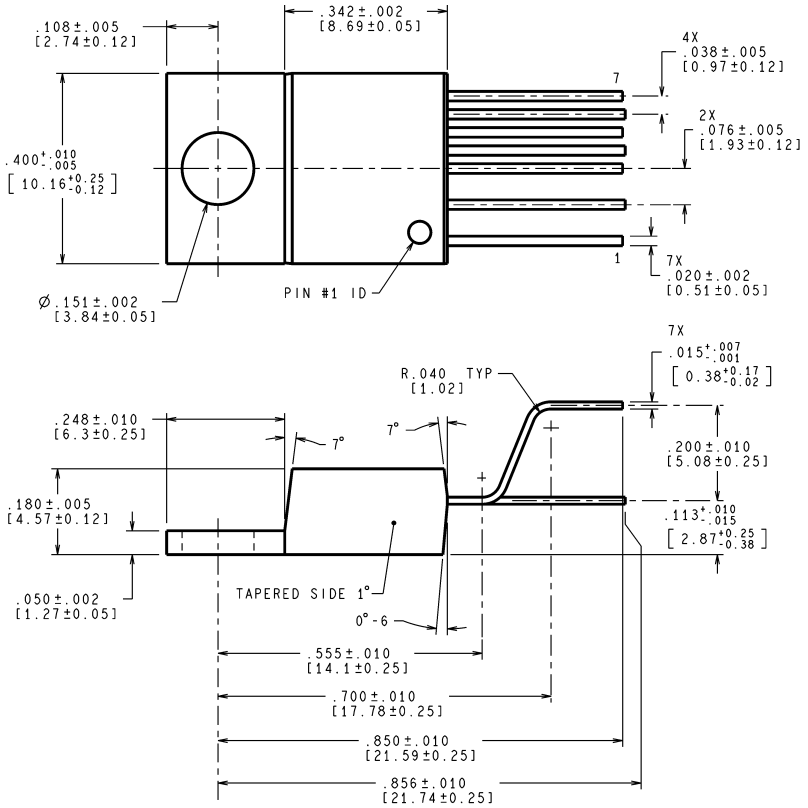
FIGURE 16. LM2433 Demonstration Board Layout
(slightly enlarged for more detail)

Physical Dimensions inches (millimeters) unless otherwise noted



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