National Semiconductor

April 2000

LM2453
Monolithic Triple 6 nS CRT Driver With Integrated Clamp and G1 Blanking

General Description

The AC2DC driver is an integrated high voltage triple CRT driver circuit designed for use in color monitor applications. The input signal interface to the IC is a multiplexed signal containing both clamp and video signal information, relative to a 1.7 V_{DC} reference.

The IC contains three high gain, high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to −52 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

Integrated with the driver is triple clamp circuit for DC recovery of each of the AC coupled outputs. The DC clamp circuit amplifies the clamp signal that is multiplexed on the video signal input. The DC clamp amplifiers are high gain, high input impedance amplifiers, setting a low impedance DC level at the clamp output which can be used to restore the DC level of the cathode drive. Each channel has a gain that is internally set to +73.

Also integrated within the package is a 40 V_{P-P} vertical blanking driver that is designed to provide vertical retrace blanking on G1 of the CRT. This is a current limited, low impedance output capable of driving normal G1 decoupling capacitances via an external resistor. The output of the G1 driver can also be used to drive a voltage boost capacitor (22 µF). When connected between the G1 drive output and the 120V supply input pin, a 120V boost supply is achieved which can be used to drive the internal DC clamp circuit, thereby eliminating the requirement for a 120V clamp supply.

The IC is packaged in an industry standard 15-lead TO-220 molded plastic power package.

Features

- Low power dissipation
- Well matched with LM1253A video pre-amp
- Three wideband video amplifiers
- Three integrated active clamp circuits
- Convenient TO-220 staggered lead package
- Built in horizontal blanking
- Integrated 120V supply and G1 vertical blank drive circuit

Applications

- 1280 x 1024 Resolution displays up to 85 Hz refresh
- Pixel clock frequencies up to 135 MHz
- Monitors requiring horizontal video blanking

Block Diagram

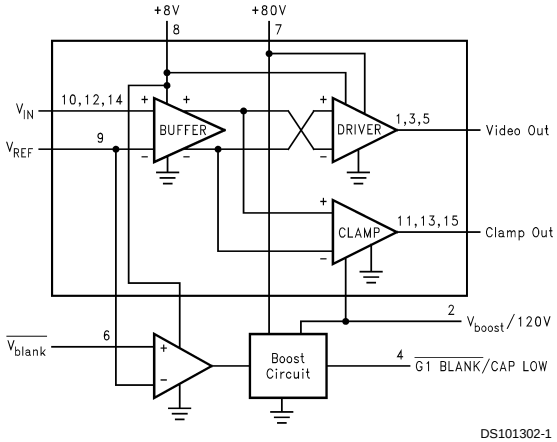

FIGURE 1. LM2453 Block Diagram

Package Pinout

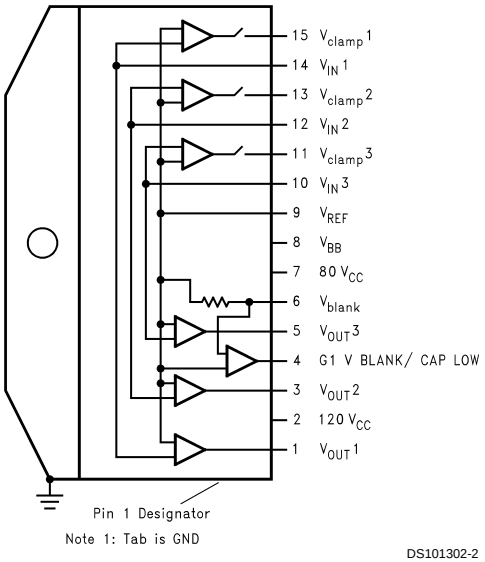

FIGURE 2. LM2453 Package Pinout
Order Number LM2453TA

Special Features

MULTIPLEXED VIDEO SIGNAL INPUT

The LM2453 accepts the multiplexed video signal from the LM1253 which contains the video signal and DC clamp level. This multiplexed signal is shown in *Figure 3*. It was designed to simplify the interface between the pre-amp and CRT Driver. Slightly over 1V of dynamic range is provided for the video and OSD portions of the waveform. The clamp signal control voltage range is approximately 0.9V. The typical numbers for the black and white levels shown correspond to a nominal swing of 40 V_{P-P} (from 25 to 65) at the video outputs of the LM2453. The clamp pulse lower level is used to set the voltage at the clamp outputs of the LM2453.

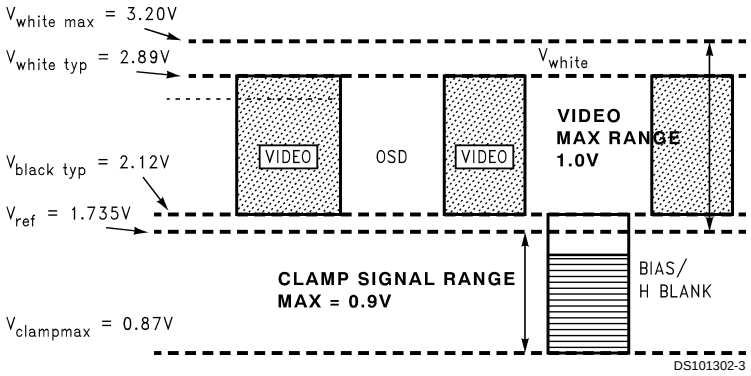

FIGURE 3. National LM1253 Multiplexed Video Signal

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

80V Voltage, V_{CC1}	+90V
120V Supply V_{CC2}	+130V
Bias Voltage, V_{BB}	+15V
Input Voltage, V_{IN}	0V to 4V
V_{BLANK} Input Voltage, V_{BLANK}	0V to V_{BB}V
Storage Temperature Range, T_{STG}	−65˚C to +150˚C
Lead Temperature (Soldering, <10 sec.)	300˚C
ESD Tolerance, Human Body Model	2 kV
ESD Tolerance, Machine Model	200V

Operating Ranges (Note 2)

V_{CC1}	+60V to +85V
V_{BOOST}	V_{CC1} to +125V
V_{BB}	7.0V to +9V
V_{IN}	0.8V to +3.5V
V_{REF}	+1.6V to +1.9V
V_{BLANK} Input Voltage, V_{BLANK}	0V to 5.5V
V_{OUT}	+15V to +78V
V_{CLAMP}	+55V to +118V
Case Temperature	−20˚C to 100˚C

AC Driver Electrical Characteristics

(See *Figure 4* for Test Circuit)
Unless otherwise noted: V_{CC} = +80V, V_{BB} = +8V, V_{IN} = 2.500 V_{DC}, C_L = 8 pF, Output = 40 V_{PP} at 1 MHz, T_C = 50˚C, V_{REF} = 1.735V, HEATSINK MUST BE GROUNDED.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	V_{CC} Supply Current	All 3 Channels, No Output Load		35	45	mA
I_{BB}	V_{BB} Supply Current	All 3 Channels, No Output Load		22	35	mA
I_{OUTTYP}	Typical DC Output Voltage	No AC Input Signal, V_{IN} = 2.100 V_{DC}	62	66	70	V_{DC}
A_{VTYP}	Typical DC Voltage Gain	No AC Input Signal		−52		V/V
I_{RTYP}	Typical Rise Time	10% to 90%, (Note 5)		6.0		ns
+OS	Overshoot on Rising Edge			5		%
t_{FTYP}	Typical Fall Time	90% to 10%, (Note 5)		6.0		ns
−OS	Overshoot on Falling Edge			6		%
LE	Linearity Error	V_{IN} 2.0 V_{DC} to 3.0 V_{DC}, (Note 4)		6		%

Note 1: Limits of "Absolute Maximum Ratings" indicate limits below which damage to the device will not occur.

Note 2: Limits of "Operating Ratings" indicate required boundaries of conditions for which the device is functional, but is not guaranteed to meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Linearity error is the variation in DC gain from V_{IN} = 2.0 to 3.0.

Note 5: Input from signal generator: t_r, t_f < 1 ns.

DRIVER Test Circuit

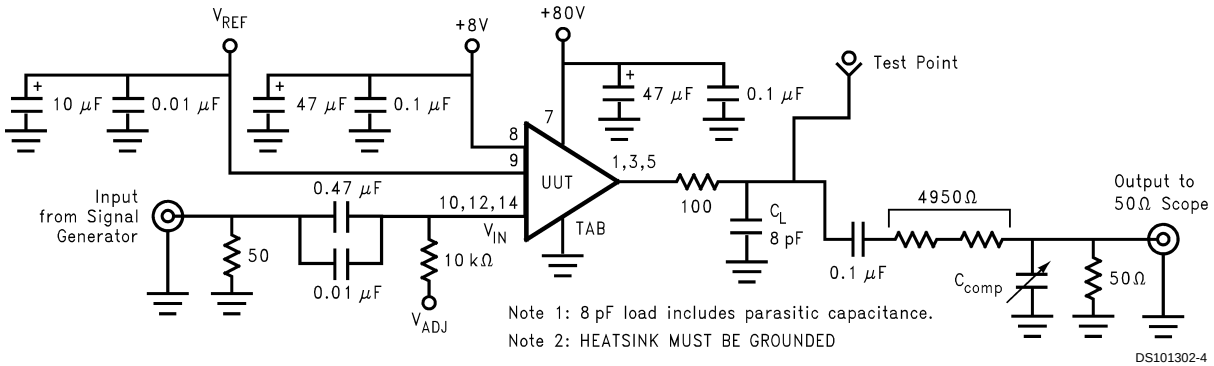

FIGURE 4. Test Circuit (One Channel)

Figure 4 shows the test circuit for the LM2453. This circuit allows testing of the LM2453 in a 50Ω environment as well as with a FET probe. The 4950Ω resistor at the output forms a 200:1 voltage divider when connected to a 50Ω load. C_{COMP} must be adjusted for equivalent performance to the FET probe. Performance will be affected slightly by the 5k load.

DRIVER Test Circuit (Continued)

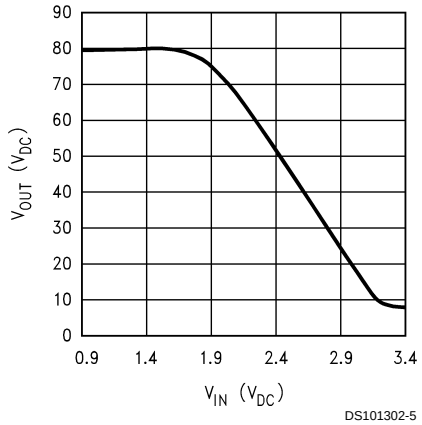

FIGURE 5. CRT Driver V_O vs V_{IN}

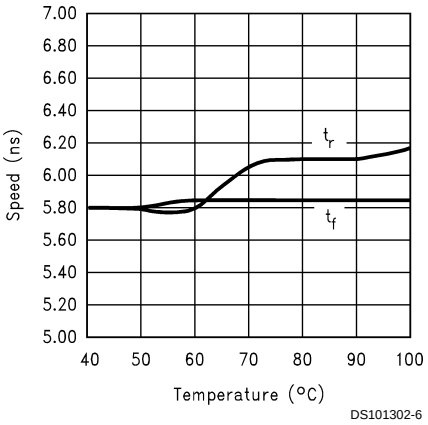

FIGURE 6. CRT Driver Speed vs. Temperature

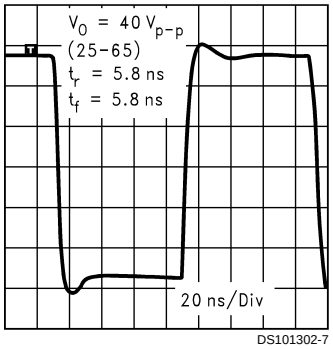

FIGURE 7. CRT Driver Transient Response

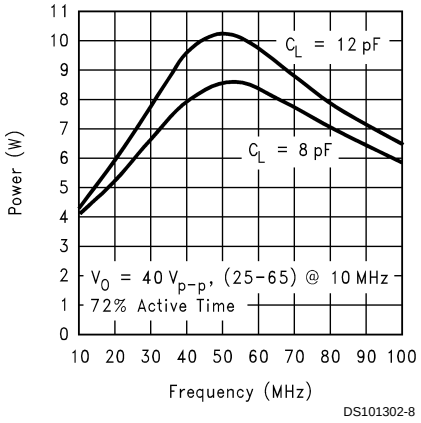

FIGURE 8. CRT Driver Power Dissipation vs. Frequency

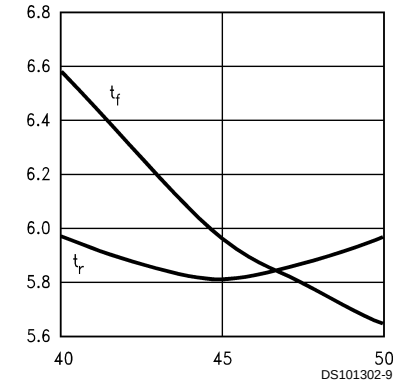

FIGURE 9. CRT Driver Speed vs. Offset

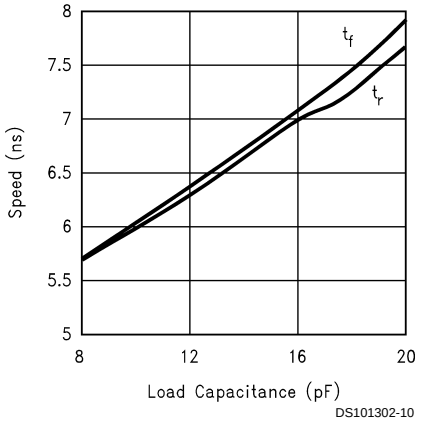

FIGURE 10. Speed vs. Load

DC CLAMP Electrical Characteristic Targets and Limits (See *Figure 11* for Test Circuit)

Unless otherwise noted: V_{CC1} = +80V, V_{CC2} = 120V, V_{BB} = +8V, T_C = 50˚C, V_{REF} = 1.735V, SW1 open.
HEATSINK MUST BE GROUNDED.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC2}	V_{CC2} Supply Current	All 3 Channels V_{IN} = 1.20 V_{DC}		4	7	mA
V_{OUT}	DC Output Voltage	No AC Input Signal, V_{IN} = 1.400V	87	92	97	V_{DC}
A_{VTYP}	Typical DC Voltage Gain	No AC Input Signal		73		
LE_{TYP}	Typical Linearity Error	No AC Input Signal (Note 6)		2		%

Note 6: Linearity Error is the variation in DC gain from V_{IN} = 1.0V to V_{IN} = 1.6V.

Clamp Amplifier Test Circuit

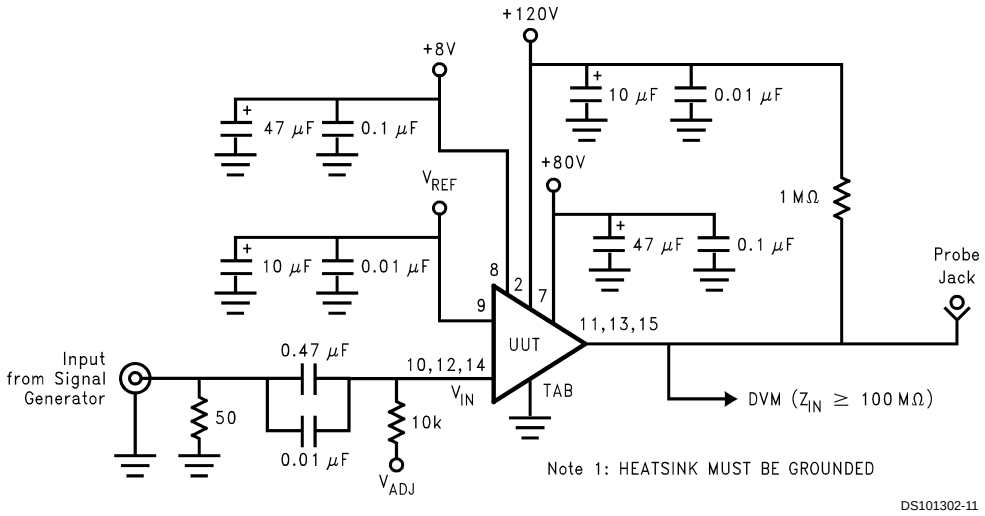

FIGURE 11. Test Circuit (One Channel)

Figure 7 shows the test circuit for evaluation of the LM2453 clamp amplifier. A high impedance VM (>100 MΩ) is used for DC measurements at the outputs.

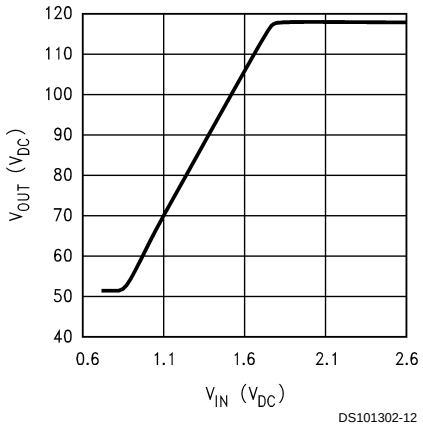

FIGURE 12. Clamp Circuit V_O vs. V_{IN}

G1 DRIVER/BOOST Electrical Characteristic Targets and Limits (See *Figure 13* for Test Circuit)

Unless otherwise noted: V_{CC} = +80V, V_{BB} = +8V, T_C = 50˚C, V_{REF} = 1.735V, HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{G1-H}	Typical G1 High Output Voltage	V_{BLANK} Input Low, See (Note 7).		49		V_{DC}
V_{G1-L}	Typical G1 Low Output Voltage	V_{BLANK} Input Low, See (Note 7).		6		V_{DC}
V_{G1PP}	Typical G1 Output Swing			43		V_{P-P}
V_{G1TH}	G1 Blanking Input Threshold			0.9		V
$V_{120BOOST}$	Typical 120V Boost Supply			123		V
I_{BOOST}	Typical 120V Boost Charge Current			50		mA

Note 7: Input from signal generator: $V_{HIGH} > 2\ V_{DC}$, $V_{LOW} < 0.5\ V_{DC}$; t_{HIGH} = 300 µs, t_{LOW} = 10 ms. Rise/fall time <0.1 µs.

120V Boost/G1 Drive Test Circuit

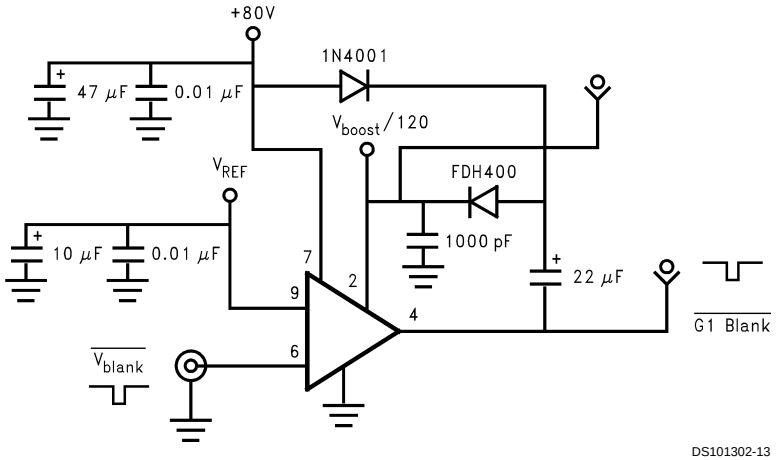

FIGURE 13. 120V Boost/G1 Drive Test Circuit

Theory of Operation

The LM2453 is a high voltage monolithic three channel CRT driver and three-channel DC clamp circuit suitable for high-resolution display applications. The device also contains a G1 blanking signal driver, which also can be used to generate a 120 VDC supply to power the DC clamp circuit. The LM2453 operates using 80V and 8V power supplies. An external supply can also be used to power the clamp circuit if the user desires to do so. The part is housed in the industry standard 15-lead TO-220 molded plastic power package.

A simplified circuit block diagram of the LM2453 is shown in *Figure 1.* A reference supply of approximately 1.7 VDC is supplied to pin 9 of the device. This provides a reference level for the minus input of the video and clamp buffer amplifiers as well as for the vertical blank comparator. The output of the buffer amplifier drives the video amplifier which provides a gain of -52 to the input signal and only amplifies the portion of the input signal that is above the reference voltage. When the input signal is at or below V_{REF} the video outputs are driven to the +80V supply rail. The output of the driver is a low impedance complimentary emitter follower circuit that minimizes the effect of capacitive load variations on transient response.

The clamp amplifier provides a gain of 73 and only amplifies the portion of the input signal that is below the reference voltage. When the input signal is at or above V_{REF} the clamp outputs are driven to the V_{boost}/120V supply rail. The vertical blank comparator drives the boost circuit, which generates a 40 V_{p-p} signal that can directly drive typical G1 capacitive loads. When the first vertical blanking pulse is received, the G1 drive output enters a current limited latched state until the 120V boost capacitor is fully charged. Thereafter, the G1 output pulses in response to the vertical blanking pulse received on the multiplexed V_{REF} signal line.

Figures 4, 11, 13 show the typical test circuits for evaluation of the LM2453.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes might be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are always critical to achieving maximum performance.

Application Hints (Continued)

IMPORTANT INFORMATION

The LM2453 performance is targeted for the high-resolution market (up to 135 MHz pixel clock frequencies). It is the first device in a new product family that is being developed by National Semiconductor. Since this device is significantly different from all our previous CRT drivers, it is very important to read all the application information supplied in this document. Should you have additional questions, please contact your local FAE or sales office.

Please refer to the NSC neck board schematic and layout that are shown in *Figures 17, 18, 19* during the following discussion.

POWER SUPPLY BYPASS

Since the LM2453 is a high bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation.

V_{CC} Bypassing— A 0.1 µF (C48) capacitor should be connected from the V_{CC} supply pin (7) to ground, as close to the supply pin and heatsink (device tab) ground point as possible. Additionally, a 47 µF electrolytic capacitor (C39) should be connected through a ferrite bead (FB2 in the schematic) to the supply pin and ground. A Fair-Rite 2743003112-TR (100Ω @ 100 MHz) or equivalent should be used.

V_{BB} Bypassing— A 0.1 µF (C8) capacitor should be connected from the V_{BB} supply to ground, as close as possible to the device with as short as possible connections. Additionally, a 47 µF electrolytic capacitor (C21) should be connected through a ferrite bead (FB1) to the supply pin and ground. A Fair-Rite 2743003112-TR (100Ω @ 100 MHz) or equivalent should be used.

REFERENCE VOLTAGE

The LM2453 receives a reference voltage from the LM1253A preamp. It is critical that a 0.1 µF bypass cap be added from the V_{REF} pin to ground. The ground connection should be as close as possible to the video input side of the device (see C30 in *Figure 17*). A 75Ω resistor should also be used between the V_{REF} pin of the LM2453 and the V_{REF} pin of the LM1253A. V_{REF} should also be bypassed close to the preamp.

THE VIDEO APPLICATION CIRCUIT

Figure 14 shows the recommended circuit topology for the video amplifiers in the LM2453. This circuit is designed to yield the best transient response and reduce radiated emissions while also protecting the amplifier from damage that can be caused by CRT Arcs. The schematic in *Figures 17, 18* shows the values that yielded best performance in the NSC reference design board. The following sections discuss arc protection and transient response in detail. Refer to *Figures 17, 18, 19* for the full application schematic and PCB layout.

ARC Protection

During normal CRT operation, internal arcing may occasionally occur. At the beginning of an arc event there is some very high frequency ringing (@ ~ 100 MHz). Spark gaps, in the range of 200V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2453. They are also ineffective at limiting the peak voltage of the initial high frequency burst. This fast, high voltage, high energy pulse can damage the LM2453 video output stages. The application circuit shown in *Figure 14* is designed to help clamp the voltage at the output of the LM2453 to a safe level. The clamp diodes should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in *Figure 14*). The ground connection of the diode and the decoupling capacitor should be very close to the LM2453 ground and should be of as low impedance as possible. This will significantly reduce the high frequency voltage transients that the LM2453 would be subjected to during an arcover condition. Resistor R2 limits the arcover current that is seen by the diodes while R1 limits the current into the LM2453 as well as the voltage stress at the video outputs of the device. R2 should be a 1/2W solid carbon type resistor. R1 can be a 1/4W metal or carbon film type resistor. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2453 would be subjected to. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. The inductor will not only help protect the device but it will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 14*. Omitting any of these components could cause serious reliability problems in production.

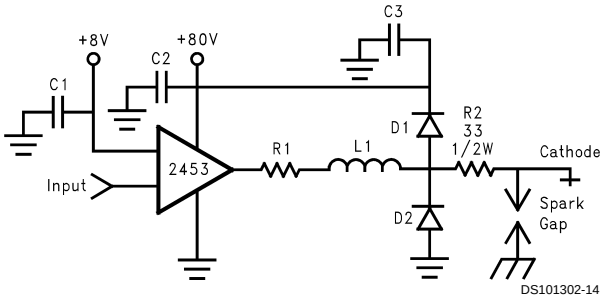

FIGURE 14. One Video Channel of the LM2453 with the Recommended Application Circuit

Optimizing Transient Response

Referring to *Figure 14*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FXXXM, where XXX specifies the value) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 17* exhibited the best overall performance in a 17 inch monitor in our lab. These can be used as a good starting point for the evaluation of the LM2453 in a new monitor application. Using a variable resistor for R1 in series with a fixed value inductor is a great way to help dial in the values needed for optimum performance in a given application. Once the optimum values are determined the variable resistors can be replaced with fixed values and corresponding inductor can be installed. In addition to the output circuit, a series inductor is used between the LM1253A video outputs and the LM2453 inputs.

Application Hints (Continued)

Effect of Load Capacitance

Figure 10 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application. It is important to note that the rise time of the series R in the test circuit in *Figure 4* along with the load capacitance will increase its contribution to the speed degradation as the load capacitance is increased. The previous section discussed how to optimize the transient response in the application with the use of a series inductor.

Effect of Offset

Figure 9 shows the variation in rise and fall times when the output offset of the device is varied from 40 VDC to 50 VDC. The rise time shows a maximum variation relative to the center data point (45 VDC) of less than 4%. The fall time shows a variation of less than 10% relative to the center data point.

It is recommended that the video black level be set about 10V below the V_{CC} power supply in the application (Black level at ~70 with V_{CC} = 80 V_{DC}). This will give the best overall performance while also minimizing the DC power dissipation.

DC CLAMP AMPLIFIERS

The portion of the multiplexed input signal that is below the reference voltage controls the DC clamp amplifiers. The DC transfer function of the amplifier is shown in *Figure 12*. *Figure 15* shows the application circuit for the clamp amplifier. Clamp diode D1 is placed as close as possible to the video node to minimize trace lengths and parasitic capacitance. Pull-up resistor R1 is required to bias the PNP output stage of the clamp circuit. Capacitor C2 provides a low impedance at high frequencies and helps minimize clamp level variation that could be caused by changes in the cathode current.

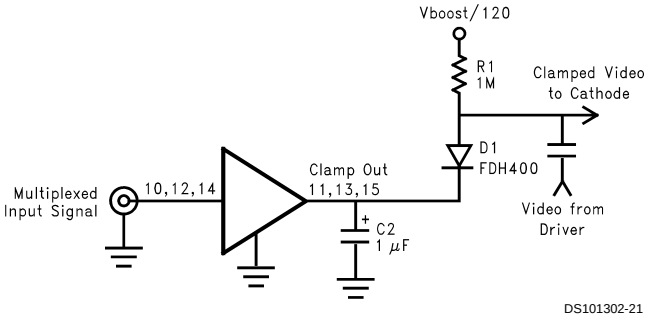

FIGURE 15. Clamp Application Circuit.

INTEGRATED BOOST SUPPLY AND G1 BLANK CIRCUIT

Upon initial power up the G1 V_{blank}/Cap Low input will sink current until the boost capacitor is charged up to approximately 74V (V_{CC1}–V_{G1-L}). After this initial charge up period, the voltage across the boost capacitor will be replenished during the vertical blank interval.

The charge cycle will be initiated by the V_{blank} input signal (negative going, logic level pulse). *Figure 16* shows the boost application circuit. During the charge cycle the voltage at pin 4 will be set to ~6V and capacitor C28 will be charged to ~74V through diode D11. When the charge cycle is completed, the voltage at pin 4 will be set to ~49V and the plus side of the boost cap will be at ~123 V_{DC}. Capacitor C29 will then be charged to ~122.3V (0.7V below 123) through D12. Diode D12 is required to avoid turning on the ESD protection diodes between the video clamp outputs and the 120V pin during the charge cycle. C29 is required to maintain the 120V at pin 2 during the charge cycle.

The 43 Vp-p pulse at pin 4 can be ac-coupled to G1 of the CRT to blank the CRT during vertical retrace. The recommended application circuit for doing this is shown in *Figure 18*.

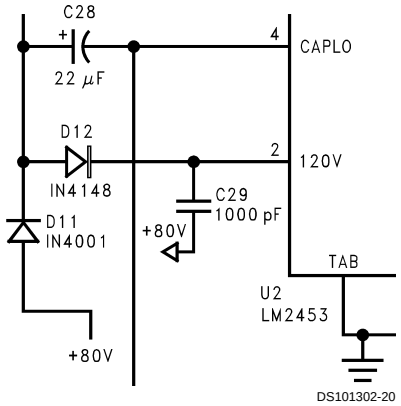

FIGURE 16. Boost Circuit Schematic

THERMAL CONSIDERATIONS

Figure 6 shows the performance of the LM2453 video amplifiers in the test circuit shown in *Figure 4* as a function of case temperature. The figure shows that the rise time of the LM2453 decreases by approximately 6% as the case temperature increases from 50˚C to 100˚C. This corresponds to a speed degradation of 1.2% for every 10˚C rise in case temperature. There is a negligible change in fall time versus temperature in the test circuit.

Figure 8 shows the total power dissipation of the LM2453 vs. frequency when all three video channels of the device are driving an 8 pF or 12 pF load with a 40 V_{p-p} signal. The graph assumes a 72% active time (device operating at the specified frequency) which is typical in a monitor application. The other 28% of the time the device is assumed to be sitting at the black level (65V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. It is important to note that the capacitive load dramatically effects the AC component of the total power dissipation.

The LM2453 case temperature must be maintained below 100˚C. If the maximum expected ambient temperature is 50˚C and the maximum power dissipation is 8.5W, then a maximum heat sink thermal resistance can be calculated:

$$R_{HS} = \frac{100^{\circ}C - 50^{\circ}C}{8.5W} = 5.9^{\circ}C \text{ Per Watt}$$

This example assumes a capacitive load of 8 pF, no resistive load and a maximum operating frequency of 50 MHz or greater.

THE NSC REFERENCE DESIGN

Figures 17, 18, 19 show the schematic and layout for the NSC Neck Board Reference Design. It contains a complete video channel from monitor input to CRT cathode. Performance is ideal for 1280 X 1024 resolution displays with pixel clock frequencies up to 135 MHz. A sample of this design along with all necessary support hardware and materials can be obtained from your local sales office.

Application Hints (Continued)

PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2453 and from the LM2453 to the CRT cathode should be as short as possible.

Due to the high gain and bandwidth of the LM2453, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

IMPORTANT LAYOUT CONSIDERATIONS

The NSC reference design can be used directly or it can be used as a guide for future layouts. Note the location of the following components:

- *C48*—V_{CC} bypass capacitor, located very close to pin 7 and the device ground.
- *C8*—V_{BB} bypass capacitor, located close to pin 8 and ground.
- *C34,C35, C46*—V_{CC} bypass capacitors, near LM2453 V_{CC} clamp diodes. Very important for arc protection. Note the direct path from the capacitor ground to the LM2453 ground.
- *C25-27*—clamp output bypass caps. Very important for a stable DC clamp voltage and for protecting the clamp outputs from damage due to a CRT arc.

The routing of the LM2453 video outputs to the CRT is very critical to achieving optimum performance. *Figure 20* shows the routing and component placement from pin 1 of the LM2453 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2453 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D16, D17, R17 and D7 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D17 is connected directly to a section of the ground plane that has a short and direct path to the LM2453 ground pins. The cathode of D16 is connected to V_{CC} very close to decoupling capacitor C34, which is connected to the same section of the ground plane as D17. The diode placement and routing is very important for minimizing the voltage stress on the LM2453 video outputs during an arc over event. Lastly, notice that S1 is placed very close to the blue cathode and is tied directly to the ground under the CRT connector.

Application Hints (Continued)

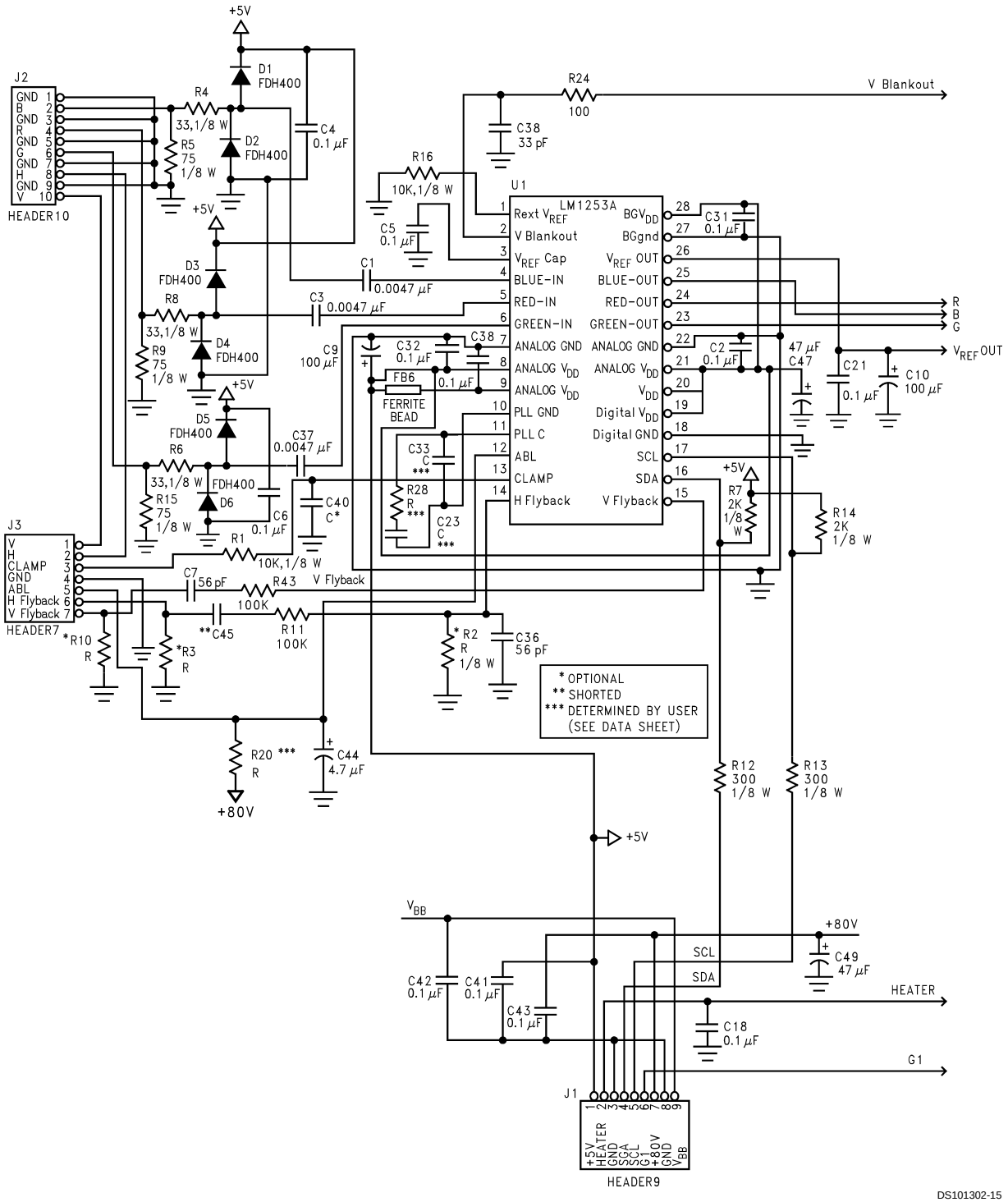

FIGURE 17. LM1253A/2453 Reference Design Schematic

Application Hints (Continued)

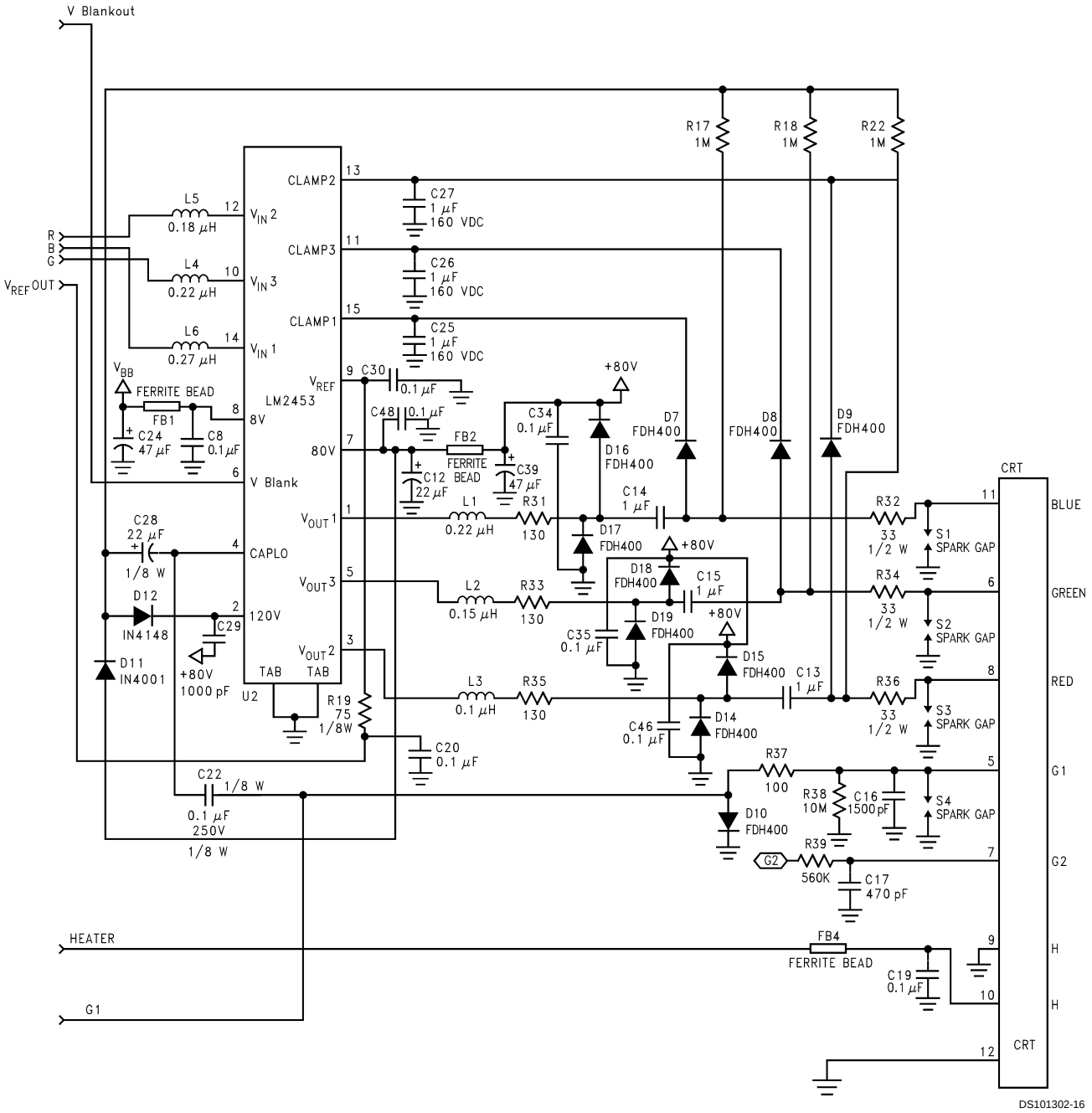

FIGURE 18. LM1253A/2453 Reference Design Schematic (continued)

Application Hints (Continued)

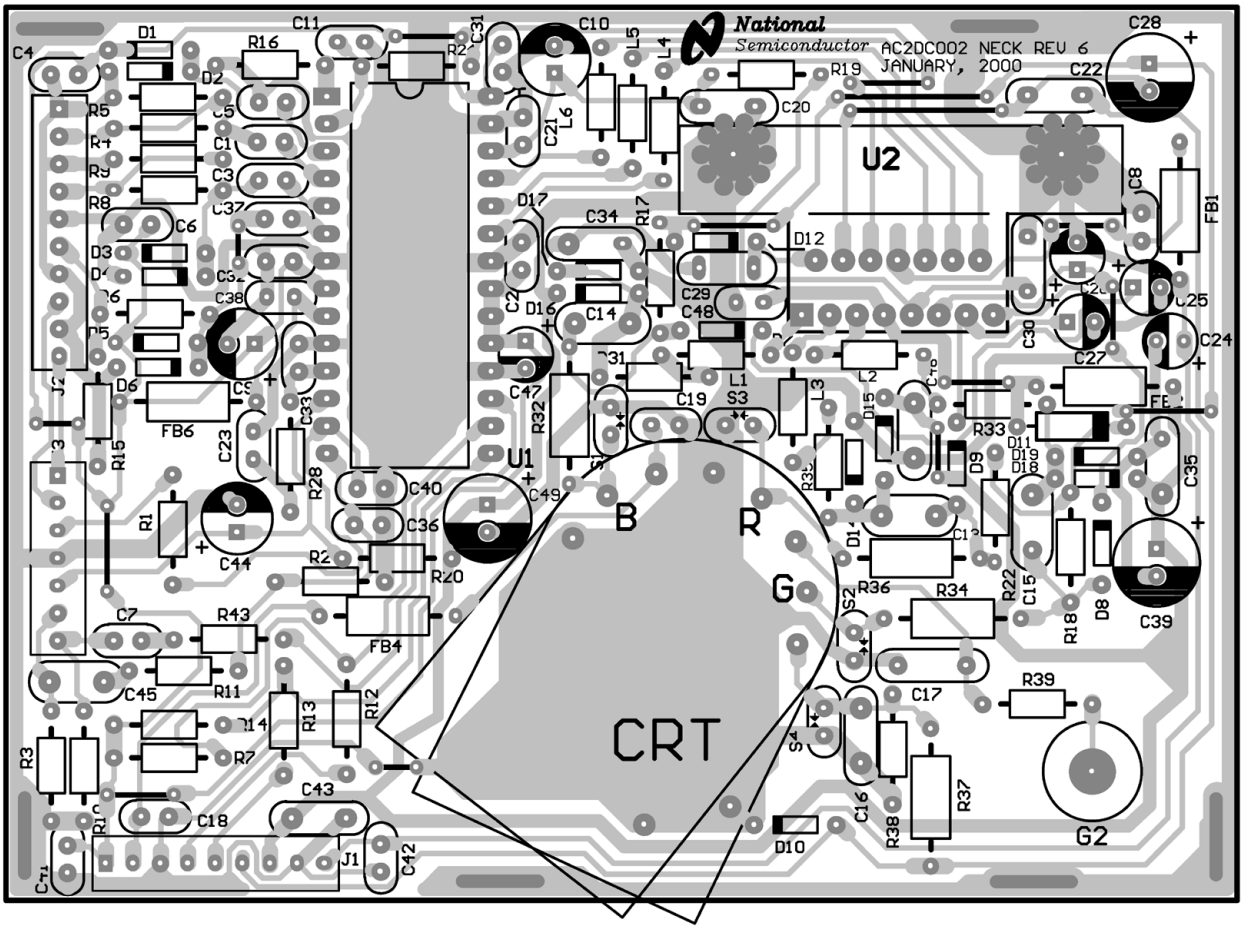

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FIGURE 19. NSC LM1253A/2453 Reference Design Layout

Application Hints (Continued)

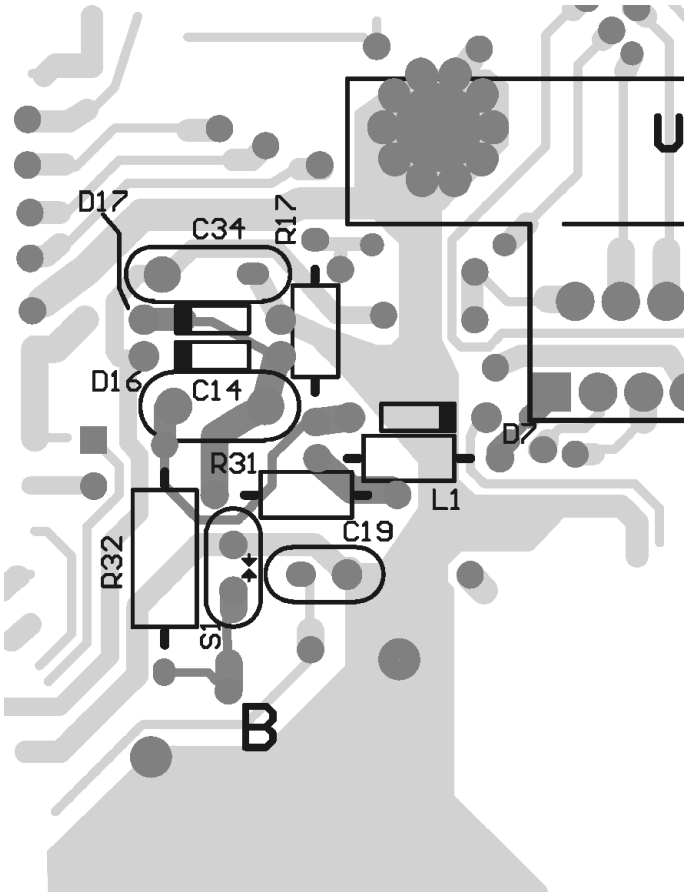
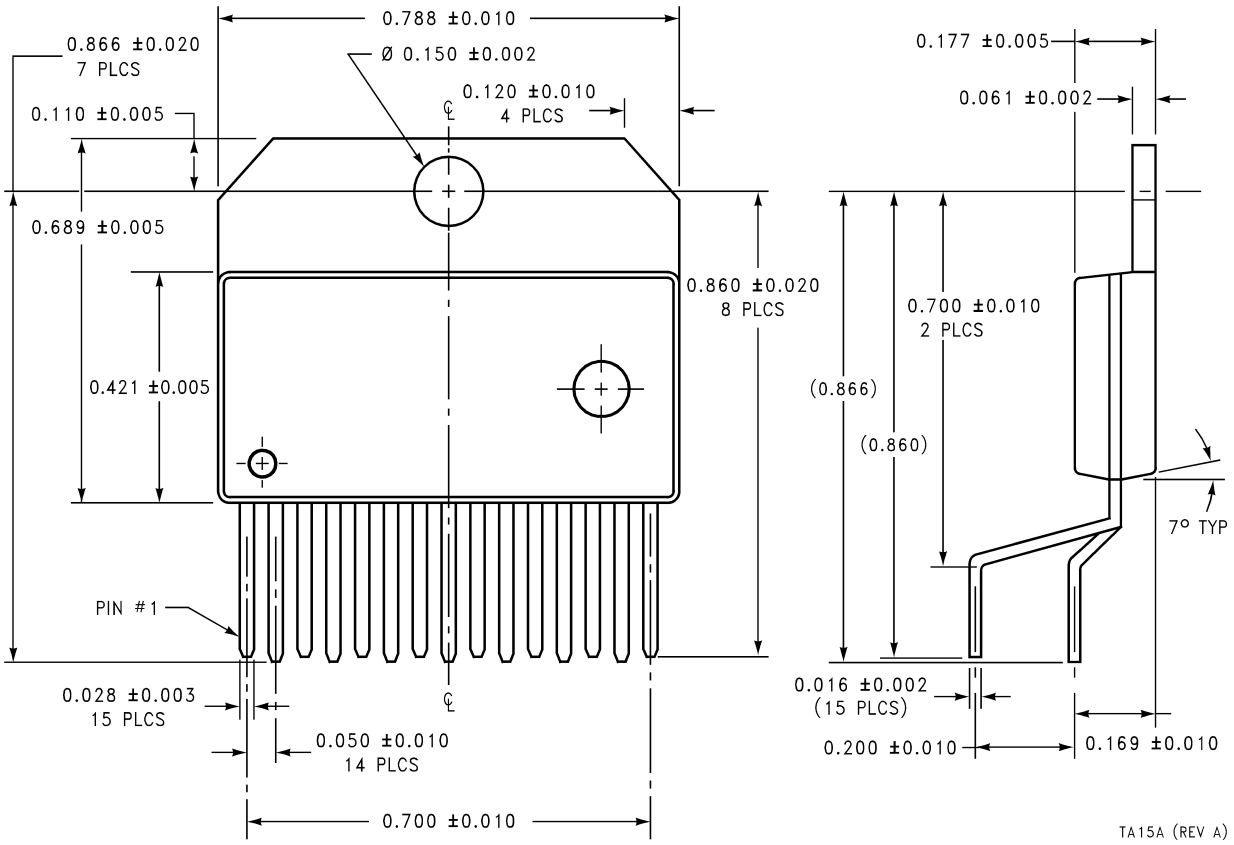


FIGURE 20. Trace Routing and Component Placement for Blue Channel Video Output.

Physical Dimensions inches (millimeters) unless otherwise noted



Note: Information contained in this data sheet is preliminary and may be subject to change without notice.

NS Package Number TA15A
Order Number LM2453TA

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