LM2638 Motherboard Power Supply Solution with a 5-Bit Programmable Switching Controller and Two Linear Regulator Controllers

Check for Samples: LM2638

FEATURES

- **Provides 3 regulated voltages**
- **Power Good flag and output enable**
- **Charge pump pin**
  - ***Switching Section***
- **Synchronous rectification**
- **5-bit DAC programmable down to 1.3V**
- **Typical ±1% DAC tolerance**
- **Switching frequency: 50 kHz to 1 MHz**
- **Over-voltage protection**
- **Two methods of over-current protection**
- **Adaptive non-overlapping FET gate drives**
- **Soft start without external capacitor**
  - ***Linear Section***
- **N-FET and NPN drive capability**
- **Ultra fast response speed**
- **Under voltage latch-off at 0.63V**
- **Output voltages default to 1.5V and 2.5V yet adjustable**

APPLICATIONS

- **Embedded power supplies for motherboards**
- **Triple DC/DC power supplies**
- **Programmable high current DC/DC power supply**

DESCRIPTION

The LM2638 provides a comprehensive embedded power supply solution for motherboards hosting high performance MPUs such as Pentium™ II, M II™, K6™-2 and other similar high performance MPUs. The LM2638 incorporates a 5-bit programmable, synchronous buck switching controller and two high-speed linear regulator controllers in a 24-pin SO package. In a typical application, the switching controller supplies the MPU core, and the linear regulator controllers supply the GTL+ bus and the clock or graphics chip core. A charge pump pin helps provide the necessary voltage to power the linear sections when 12V is shut off during system standby such as STR mode.

Switching Section — The switching regulator controller features an Intel-compatible, 5-bit programmable output voltage, over-current and over-voltage protection, a power good signal, and a logic-controlled output enable. There are two user-selectable over-current protection methods. One provides accurate over-current protection with the use of an external sense resistor. The other saves cost by taking advantage of the r_{DS_ON} of the high-side FET. When there is an over voltage, the controller turns off the high side FET and turns on the low side.

Linear Section — The two linear regulator controllers feature wide control bandwidth, N-FET and NPN transistor driving capability and an adjustable output. The wide control bandwidth makes meeting the GTL+ bus transient response requirement an easy job. In minimum configuration, the two controllers default to 1.5V and 1.25V respectively.

Both linear controllers have under voltage latch-off.

Pin Configuration

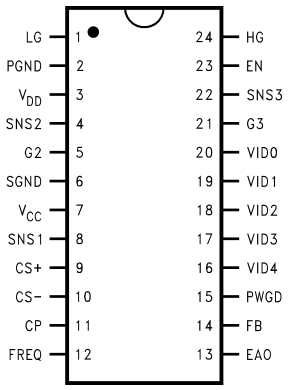


Figure 1. 24-Lead SOIC (Top View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_{CC}	7V
V_{DD}	17V
Junction Temperature	150°C
Power Dissipation (2)	1.6W
Storage Temperature	−65°C to +150°C
ESD Susceptibility	3 kV
Soldering Time, Temperature (10 sec.)	300°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. **Operating Ratings** do not imply guaranteed performance limits.

(2) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for LM2638 is 78°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 1.6W.

Operating Ratings (1)

V_{CC}	4.75V to 5.25V
Junction Temperature Range	0°C to +125°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. **Operating Ratings** do not imply guaranteed performance limits.

Electrical Characteristics

V_{CC} = 5V, V_{DD} = 12V unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the 0°C to +70°C range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{EN}	EN Pin Internal Pull-up Current		**60**	90	**140**	µA
I_{CC}	Operating V_{CC} Current	EN = 5V, VID = 10111		6	**7.5**	mA
I_{Q_VCC}	V_{CC} Shutdown Current	EN = 0V, VID Pins Floating		1.5	**3**	mA
I_{Q_VDD}	V_{DD} Shutdown Current	EN = 0V, VID Pins Floating		4		µA
R_{DS_CP}	CP Pin Resistance	High Side FET		100		Ω
		Low Side FET		10		
SWITCHING SECTION						
V_{DACOUT}	5-Bit DAC Output Voltage	(1)	***N***−1.5%	***N***	***N***+1.5%	V
I_{VID}	VID Pins Internal Pull-up Current		**60**	90	**140**	µA
f_{OSC}	Oscillator Frequency	RT = 100 kΩ	**204**	245	**286**	kHz
		RT = 25 kΩ		1000		
D_{MAX}	Maximum Duty Cycle			100		%
D_{MIN}	Minimum Duty Cycle			0		%
R_{SNS1}	SNS1 Pin Resistance to Ground		**8.5**	10	**13**	kΩ
R_{DS_SRC}	Gate Driver Resistance When Sourcing Current			6		Ω
R_{DS_SINK}	Gate Driver Resistance When Sinking Current			1.5		Ω
V_{CC_TH1}	V_{CC} Power-On-Reset Threshold			4.0	**4.3**	V
V_{CC_TH2}	V_{CC} Shutdown Threshold		**3.0**	3.6		V
V_{DAC_IH}	DAC Input High Voltage		**3.5**			V
V_{DAC_IL}	DAC Input Low Voltage				**1.3**	V
GA	Error Amplifier DC Gain			76		dB
BW_{EA}	Error Amplifier Unity Gain Bandwidth			5		MHz
V_{RAMP_L}	Ramp Signal Valley Voltage			1.25		V
V_{RAMP_H}	Ramp Signal Peak Voltage			3.25		V
t_{SS}	Soft Start Time			4096		Clock Cycles
D_{STEP_SS}	Duty Cycle Step Change during Soft Start			12.5		%
t_{PWGD}	PWGD Response Time	SNS1 Rises from 0V to Rated Output Voltage	**2**	8.4	**15**	µs
t_{PWBAD}	PWGD Response Time	SNS1 Falls from Rated Output Voltage to 0V	**2**	3.4	**10**	µs
V_{PWGD_HI}	PWGD High Trip Point	% Above Rated Output Voltage When Output Voltage↑		11.5	**13**	%
		% Above Rated Output Voltage When Output Voltage↓ (2)	**5**	7	**9**	
V_{PWGD_LO}	PWGD Low Trip Point	% Below Rated Output Voltage When Output Voltage↑		2.6	**6**	%
		% Below Rated Output Voltage When Output Voltage↓ (2)	**6**	9.5	**13**	
V_{OVP_TRP}	Over-Voltage Trip Point	% SNS1 Above Rated Output	**15**	25	**35**	%
I_{CS+}	CS+ Pin Sink Current	CS+ = 5V, CS− = 4.8V	**126**	185	**244**	µA

(1) The letter ***N*** stands for the typical output voltages appearing in ***italic boldface*** type in Table 1.
(2) The output level of the PWGD pin is a logic AND of the power good function of the switching section, the 1.5V section and the 1.25V section. For the switching section, the power good is a window. For the two linear sections, the power good is a threshold with some hysteresis.

Electrical Characteristics (continued)

V_{CC} = 5V, V_{DD} = 12V unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the 0°C to +70°C range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OCP}	Over-Current Trip Point (CS+ and CS− Differential Voltage)	CS+ = 2V, CS− Drops from 2V	**41**	55	**69**	mV
1.5V LDO CONTROLLER SECTION						
V_{SNS2}	SNS2 Voltage	V_{DD} = 12V, V_{CC} = 4.75V to 5.25V, I_{G2} = 0 mA to 20 mA	**1.463**	1.5	**1.538**	V
R_{OUT2}	Output Resistance			200		Ω
I_{SNS2}	SNS2 Pin Bias Current	When Regulating		21		µA
V_{PWGD_HI}	PWGD High Trip Point	(2)		0.63		V
V_{PWGD_LO}	PWGD Low Trip Point	(2)		0.44		V
1.25V LDO CONTROLLER SECTION						
V_{SNS3}	SNS3 Voltage	V_{DD} = 12V, V_{CC} = 4.75V to 5.25V, I_{G3} = 0 mA to 20 mA	**1.219**	1.25	**1.281**	V
R_{OUT3}	Output Resistance			200		Ω
I_{SNS3}	SNS3 Pin Bias Current	When Regulating		0		µA
V_{PWGD_HI}	PWGD High Trip Point	(2)		0.63		V
V_{PWGD_LO}	PWGD Low Trip Point	(3)		0.44		V

(3) The output level of the PWGD pin is a logic AND of the power good function of the switching section, the 1.5V section and the 1.25V section. For the switching section, the power good is a window. For the two linear sections, the power good is a threshold with some hysteresis.

Table 1. 5-Bit DAC Output Voltage Table(V_{CC} = 5V, V_{DD} = 12V ±5%, T_A = 25°C, Test Mode)

Symbol	Parameter	Conditions	Typical	Units
V_{DACOUT}	5-Bit DAC Output Voltages for Different VID Codes	VID4:0 = 01111	***1.30***	V
		VID4:0 = 01110	1.35	
		VID4:0 = 01101	***1.40***	
		VID4:0 = 01100	1.45	
		VID4:0 = 01011	***1.50***	
		VID4:0 = 01010	***1.55***	
		VID4:0 = 01001	***1.60***	
		VID4:0 = 01000	1.65	
		VID4:0 = 00111	***1.70***	
		VID4:0 = 00110	1.75	
		VID4:0 = 00101	***1.80***	
		VID4:0 = 00100	1.85	
		VID4:0 = 00011	***1.90***	
		VID4:0 = 00010	1.95	
		VID4:0 = 00001	***2.00***	
		VID4:0 = 00000	2.05	
		VID4:0 = 11111	(shutdown)	
		VID4:0 = 11110	2.1	
		VID4:0 = 11101	***2.2***	
		VID4:0 = 11100	2.3	
		VID4:0 = 11011	2.4	
		VID4:0 = 11010	2.5	
		VID4:0 = 11001	2.6	
		VID4:0 = 11000	2.7	
		VID4:0 = 10111	***2.8***	
		VID4:0 = 10110	2.9	
		VID4:0 = 10101	3.0	
		VID4:0 = 10100	3.1	
		VID4:0 = 10011	3.2	
		VID4:0 = 10010	***3.3***	
		VID4:0 = 10001	3.4	
		VID4:0 = 10000	3.5	

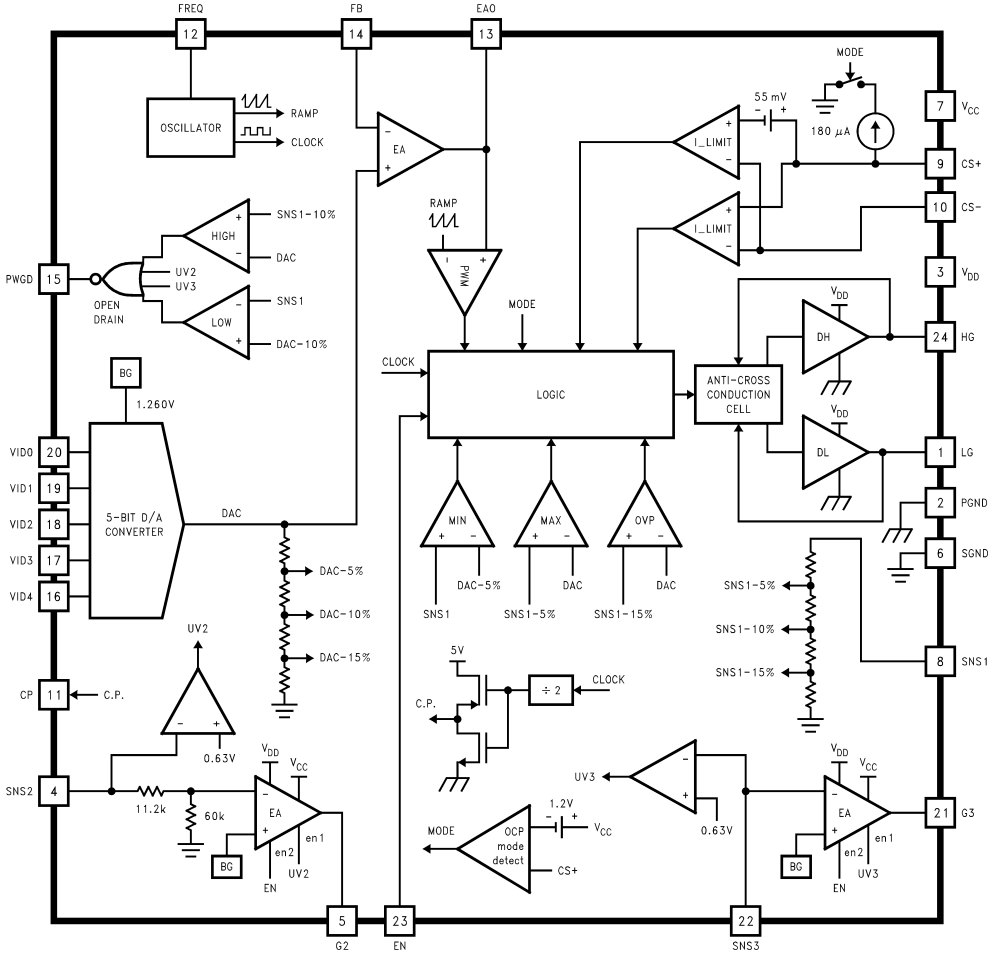
Table 2. Pin Description

Pin	Pin Name	Pin Function
1	LG	Low side N-FET gate driver output.
2	PGND	Ground for the two FET drivers of the switching section.
3	V_{DD}	Supply for the FET gate drivers. Usually tied to +12V.
4	SNS2	Feedback pin for the 1.5V linear regulator.
5	G2	Gate drive output for the external N-MOS of the fast 1.5V linear regulator.
6	SGND	Ground for internal signal circuitry and system ground reference.
7	V_{CC}	Supply voltage. Usually +5V.
8	SNS1	Output voltage monitor input for the switching regulator.
9	CS+	Switching regulator current sense input, positive node.
10	CS−	Switching regulator current sense input, negative node.
11	CP	Charge pump. Output is a square wave with 50% duty cycle. Amplitude is close to V_{CC} voltage.
12	FREQ	Switching frequency adjustment pin. An external resistor is needed to set the desired frequency.

Table 2. Pin Description (continued)

Pin	Pin Name	Pin Function
13	EAO	Output of the error amplifier. Used for compensating the switching regulator.
14	FB	Inverting input of the error amplifier. Used for compensating the switching regulator.
15	PWGD	Open collector Power Good signal.
16	VID4	5-Bit DAC input, MSB.
17	VID3	5-Bit DAC input.
18	VID2	5-Bit DAC input.
19	VID1	5-Bit DAC input.
20	VID0	5-Bit DAC input, LSB.
21	G3	Gate drive pin for the external N-MOS of the 1.25V linear regulator.
22	SNS3	Feedback pin for the 1.25V linear regulator.
23	EN	Output Enable. A logic low shuts the whole chip down.
24	HG	High side N-FET gate driver output.

Block Diagram



Test Circuit

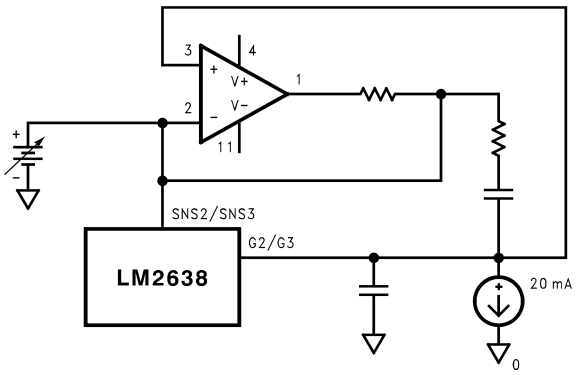


Figure 2. LDO Controller Test Circuit

Typical Application

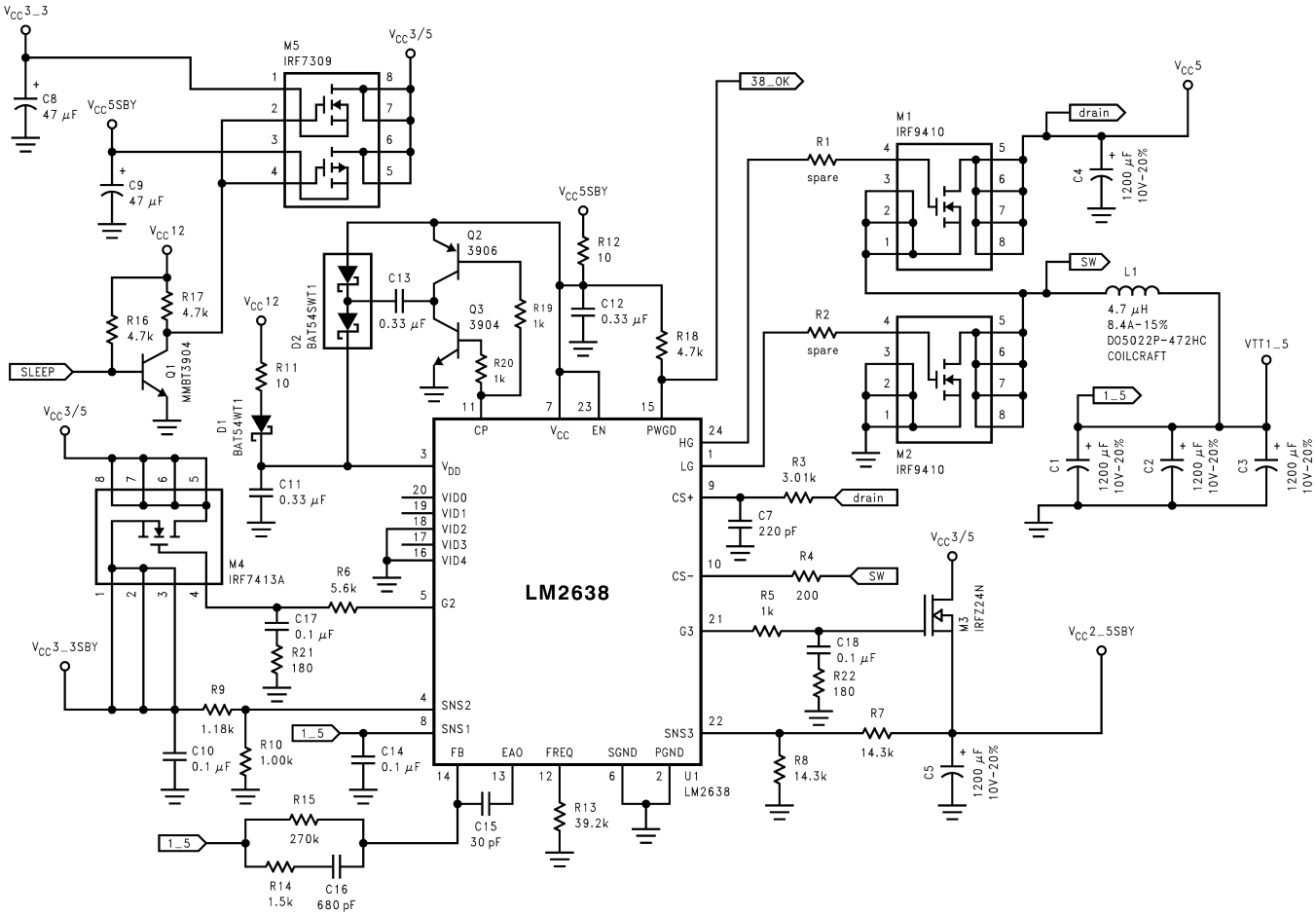


Figure 3. Using LM2638 to Supply GTL+ Bus (VTT, 1.5V, 5.6A), 2.5V Standby (V_{CC}2_5SBY, 2A Full Power and 180 mA Suspend) and 3.3V Standby (V_{CC}3_3SBY, 1.5A Full Power, 0.5A Suspend)

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