

LM27222 High-Speed 4.5A Synchronous MOSFET Driver

Check for Samples: [LM27222](#)

FEATURES

- Adaptive Shoot-through Protection
- 10ns Dead Time
- 8ns Propagation Delay
- 30ns Minimum On-time
- 0.4Ω Pull-down and 0.9Ω Pull-up Drivers
- 4.5A Peak Driving Current
- MOSFET Tolerant Design
- 5μA Quiescent Current
- 30V Maximum Input Voltage in Buck Configuration
- 4V to 6.85V Operating Voltage
- SOIC-8 and WSON Packages

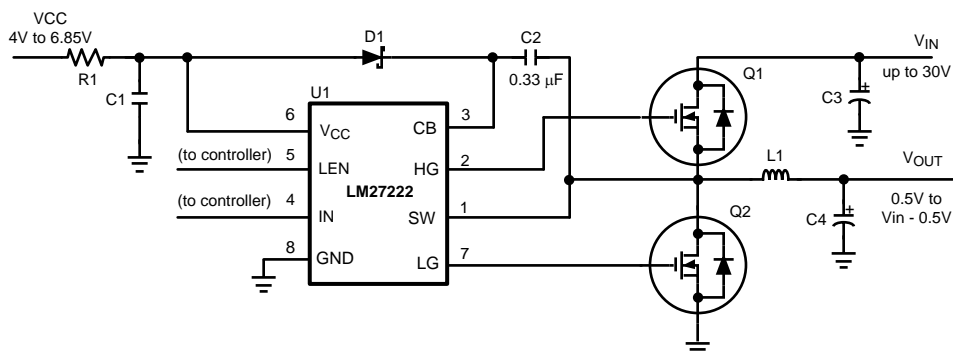
APPLICATIONS

- High Current Buck And Boost Voltage Converters
- Fast Transient DC/DC Power Supplies
- Single Ended Forward Output Rectification
- CPU And GPU Core Voltage Regulators

DESCRIPTION

The LM27222 is a dual N-channel MOSFET driver designed to drive MOSFETs in push-pull configurations as typically used in synchronous buck regulators. The LM27222 takes the PWM output from a controller and provides the proper timing and drive levels to the power stage MOSFETs. Adaptive shoot-through protection prevents damaging and efficiency reducing shoot-through currents, thus ensuring a robust design capable of being used with nearly any MOSFET. The adaptive shoot-through protection circuitry also reduces the dead time down to as low as 10ns, ensuring the highest operating efficiency. The peak sourcing and sinking current for each driver of the LM27222 is about 3A and 4.5Amps respectively with a V_{gs} of 5V. System performance is also enhanced by keeping propagation delays down to 8ns. Efficiency is once again improved at all load currents by supporting synchronous, non-synchronous, and diode emulation modes through the LEN pin. The minimum output pulse width realized at the output of the MOSFETs is as low as 30ns. This enables high operating frequencies at very high conversion ratios in buck regulator designs. To support low power states in notebook systems, the LM27222 draws only 5μA from the 5V rail when the IN and LEN inputs are low or floating.

Typical Application



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Connection Diagram

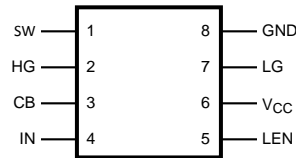
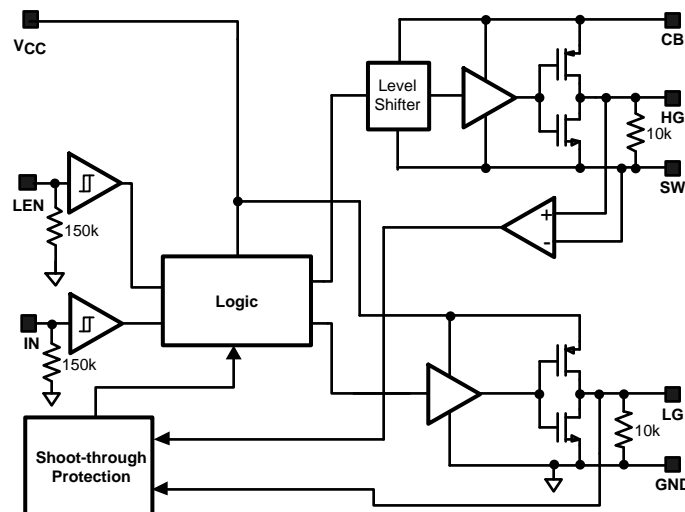


Figure 1. Top View
SOIC-8 (Package # D0008A) $\theta_{JA} = 172^{\circ}\text{C/W}$
or
WSON-8 (Package # NGT0008A) $\theta_{JA} = 39^{\circ}\text{C/W}$

PIN DESCRIPTIONS

| Pin # | Pin Name | Pin Function |
|-------|-----------------|---|
| 1 | SW | High-side driver return. Should be connected to the common node of high and low-side MOSFETs. |
| 2 | HG | High-side gate drive output. Should be connected to the high-side MOSFET gate. Pulled down internally to SW with a 10K resistor to prevent spurious turn on of the high-side MOSFET when the driver is off. |
| 3 | CB | Bootstrap. Accepts a bootstrap voltage for powering the high-side driver. |
| 4 | IN | Accepts a PWM signal from a controller. Active High. Pulled down internally to GND with a 150K resistor to prevent spurious turn on of the high-side MOSFET when the controller is inactive. |
| 5 | LEN | Low-side gate enable. Active High. Pulled down internally to GND with a 150K resistor to prevent spurious turn-on of the low-side MOSFET when the controller is inactive. |
| 6 | V _{CC} | Connect to +5V supply. |
| 7 | LG | Low-side gate drive output. Should be connected to low-side MOSFET gate. Pulled down internally to GND with a 10K resistor to prevent spurious turn on of the low-side MOSFET when the driver is off. |
| 8 | GND | Ground. |

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

| | |
|--|--------------------------------------|
| V _{CC} to GND | -0.3V to 7V |
| CB to GND | -0.3V to 36V |
| CB to SW | -0.3V to 7V |
| SW to GND ⁽²⁾ | -2V to 36V |
| LEN, IN, LG to GND | -0.3V to V _{CC} + 0.3V ≤ 7V |
| HG to GND | -0.3V to 36V |
| Junction Temperature | +150°C |
| Power Dissipation ⁽³⁾ | 720mW |
| Storage Temperature | -65° to 150°C |
| ESD Susceptibility Human Body Model | 2kV |

- (1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply ensured performance limits.
- (2) The SW pin can have -2V to -0.5 volts applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30 Volts.
- (3) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_{MAX} = (T_{JMAX} - T_A) / θ_{JA}. The junction-to-ambient thermal resistance, θ_{JA}, for the LM27222M, it is 165°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 0.76W. The θ_{JA} for the LM27222SD is 42°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 3W.

Operating Ratings ⁽¹⁾

| | |
|----------------------------|---------------|
| VCC | 4V to 6.85V |
| Junction Temperature Range | -40° to 125°C |
| CB (max) | 33V |

- (1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply ensured performance limits.

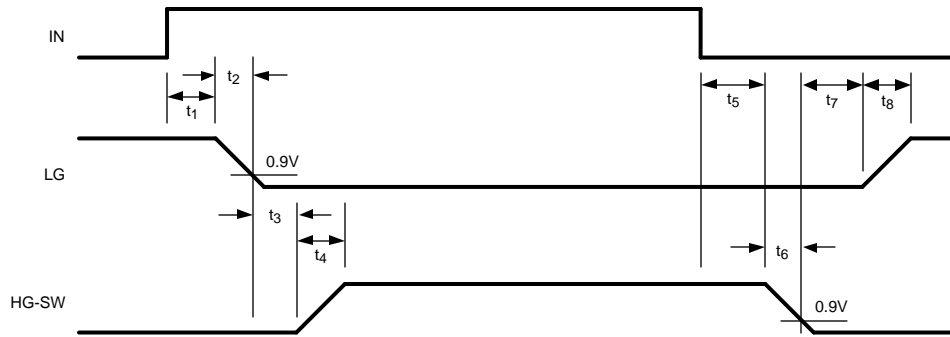
Electrical Characteristics ⁽¹⁾

VCC = CB = 5V, SW = GND = 0V, unless otherwise specified. Typical and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range (-40°C ≤ T_J ≤ 125°C).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------|-------------------------------------|---|-----------|-----------|------------|----------------------|
| POWER SUPPLY | | | | | | |
| I _{q_op} | Operating Quiescent Current | IN = 0V, LEN = 0V | | 5 | 15 | μA |
| | | | | 30 | | |
| | | IN = 0V, LEN = 5V | 500 | 540 | 650 | μA |
| | | | | | 825 | |
| HIGH-SIDE DRIVER | | | | | | |
| | Peak Pull-up Current | | | 3 | | A |
| R _{H-pu} | Pull-up Rds_on | I _{CB} = I _{HG} = 0.3A | | 0.9 | 2.5 | Ω |
| | Peak Pull-down Current | | | 4.5 | | A |
| R _{H-pd} | Pull-down Rds_on | I _{SW} = I _{HG} = 0.3A | | 0.4 | 1.5 | Ω |
| t ₄ | Rise Time | Timing Diagram, C _{LOAD} = 3.3nF | | 17 | | ns |
| t ₆ | Fall Time | Timing Diagram, C _{LOAD} = 3.3nF | | 12 | | ns |
| t ₃ | Pull-up Dead Time | Timing Diagram | | 9.5 | | ns |
| t ₅ | Pull-down Delay | Timing Diagram | | 16.5 | | ns |
| t _{on_min} | Minimum Positive Output Pulse Width | | | 30 | | ns |
| LOW-SIDE DRIVER | | | | | | |
| | Peak Pull-up Current | | | 3.2 | | A |
| R _{L-pu} | Pull-up Rds_on | I _{VCC} = I _{LG} = 0.3A | | 0.9 | 2.5 | Ω |
| | Peak Pull-down Current | | | 4.5 | | A |
| R _{L-pd} | Pull-down Rds_on | I _{GND} = I _{LG} = 0.3A | | 0.4 | 1.5 | Ω |
| t ₈ | Rise Time | Timing Diagram, C _{LOAD} = 3.3nF | | 17 | | ns |
| t ₂ | Fall Time | Timing Diagram, C _{LOAD} = 3.3nF | | 14 | | ns |
| t ₇ | Pull-up Dead Time | Timing Diagram | | 11.5 | | ns |
| t ₁ | Pull-down Delay | Timing Diagram | | 7.7 | | ns |
| PULL-DOWN RESISTANCES | | | | | | |
| | HG-SW Pull-down Resistance | | | 10k | | Ω |
| | LG-GND Pull-down Resistance | | | 10k | | Ω |
| | LEN-GND Pull-down Resistance | | | 150K | | Ω |
| | IN-GND Pull-down Resistance | | | 150K | | Ω |
| LEAKAGE CURRENTS | | | | | | |
| I _{leak_IN} | IN pin Leakage Current | IN = 0V, Source Current | | 50 | | nA |
| | | IN = 5V, Sink Current | | 33 | | μA |
| I _{leak_LEN} | LEN pin Leakage Current | LEN = 0V, Source Current | | 200 | | nA |
| | | LEN = 5V, Sink Current | | 33 | | μA |
| LOGIC | | | | | | |
| V _{IH_LEN} | LEN Low to High Threshold | Low to High Transition | | | 65 | % of V _{CC} |
| V _{IL_LEN} | LEN High to Low Threshold | High to Low Transition | 30 | | | % of V _{CC} |
| V _{IH_IN} | IN Low to High Threshold | Low to High Transition | | | 65 | % of V _{CC} |
| V _{IL_IN} | IN High to Low Threshold | High to Low Transition | 30 | | | % of V _{CC} |
| | Threshold Hysteresis | | | 0.7 | | V |

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Timing Diagram



Typical Waveforms

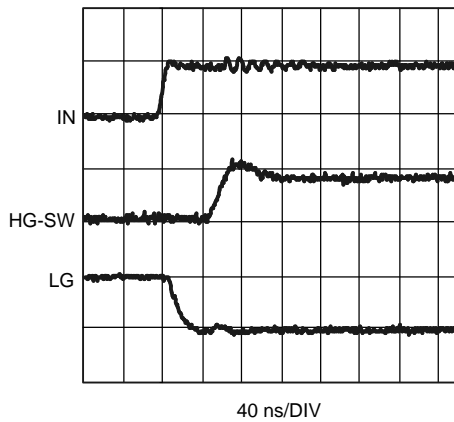


Figure 2. PWM Low-to-High Transition at IN Input

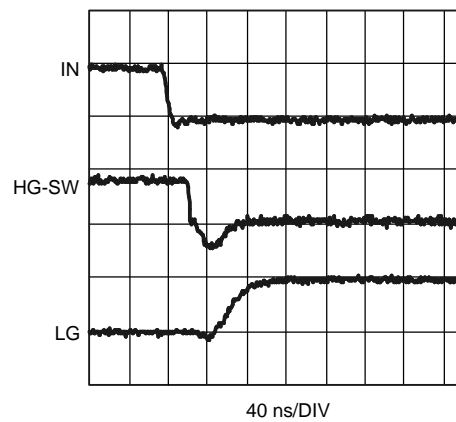


Figure 3. PWM High-to-Low Transition at IN Input

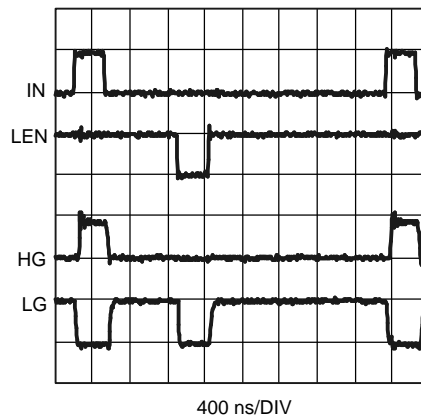


Figure 4. LEN Operation

The typical waveforms are from a circuit similar to [Typical Application](#) with:

Q1: 2 x Si7390DP

Q2: 2 x Si7356DP

L1: 0.4 μ H

V_{IN} : 12V

APPLICATION INFORMATION

GENERAL

The LM27222 is designed for high speed and high operating reliability. The driver can handle very narrow, down to zero, PWM pulses in a specified, deterministic way. Therefore, the HG and LG outputs are always in predictable states. No latches are used in the HG and LG control logic so the drivers cannot get "stuck" in the wrong state. The driver design allows for powering up with a pre-biasing voltage being present at the regulator output. To reduce conduction losses in DC-DC converters with low duty factors the LM27222 driver can be powered from a $6.5V \pm 5\%$ power rail.

It is recommended to use the same power rail for both the controller and driver. If two different power rails are used, never allow the PWM pulse magnitude at the IN input or the control voltage at the LEN input to be above the driver V_{CC} voltage or unpredictable HG and LG outputs pulse widths may result.

MINIMUM PULSE WIDTH

As the input pulse width to the IN pin is decreased, the pulse width of the high-side gate drive (HG-SW) also decreases. However, for input pulse widths 60ns and smaller, the HG-SW remains constant at 30ns. Thus the minimum pulse width of the driver output is 30ns. Figure 5 shows an input pulse at the IN pin 20ns wide, and the output of the driver, as measured between the nodes HG and SW is a 30ns wide pulse. Figure 6 shows the variation of the SW node pulse width vs IN pulse width. At the IN pin, if a falling edge is followed by a rising edge within 5ns, the HG may ignore the rising edge and remain low until the IN pin toggles again. If a rising edge is followed by a falling edge within 5ns, the pulse may be completely ignored.

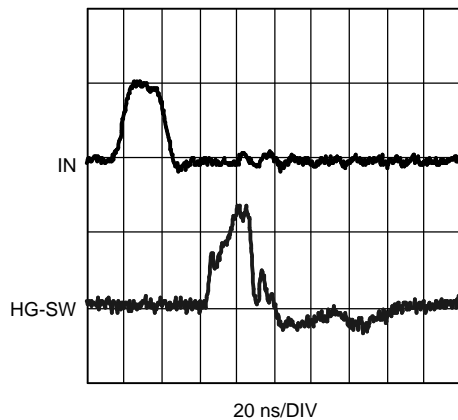


Figure 5. Min On Time

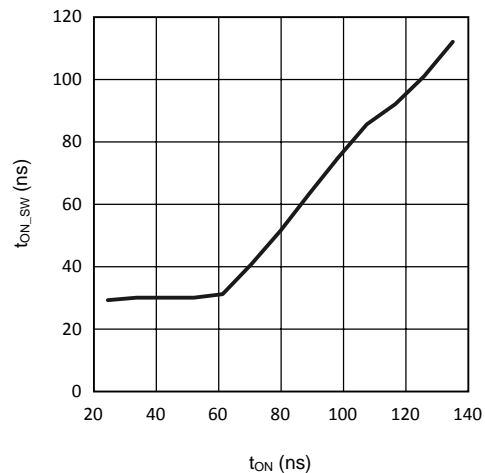


Figure 6.

ADAPTIVE SHOOT-THROUGH PROTECTION

The LM27222 prevents shoot-through power loss by ensuring that both the high- and low-side MOSFETs are not conducting at the same time. When the IN signal rises, LG is first pulled down. The adaptive shoot-through protection circuit waits for LG to reach 0.9V before turning on HG. Similarly, when IN goes low, HG is pulled down first, and the circuit turns LG on only after the voltage difference between the high-side gate and the switch node, i.e., HG-SW, has fallen to 0.9V.

It is possible in some applications that at power-up the driver's SW pin is above 3V in either buck or boost converter applications. For instance, in a buck configuration a pre-biasing voltage can be either a voltage from another power rail connected to the load, or a leakage voltage through the load, or it can be an output capacitor pre-charged above 3V while no significant load is present. In a boost application it can be an input voltage rail above 3V.

In the case of insufficient initial CB-SW voltage (less than 2V) such as when the output rail is pre-biased, the shoot-through protection circuit holds LG low for about 170ns, beginning from the instant when IN goes high. After the 170ns delay, the status of LG is dictated by LEN and IN. Once LG goes high and SW goes low, the bootstrap capacitor will be charged up (assuming SW is grounded for long enough time). As a result, CB-SW will be close to 5V and the LM27222 will now fully support synchronous operation.

The dead-time between the high- and low-side pulses is kept as small as possible to minimize conduction through the body diode of the low-side MOSFET(s).

POWER DISSIPATION

The power dissipated in the driver IC when switching synchronously can be calculated as follows:

$$P = \frac{f_{SW} \times V_{CC}}{2} \left\{ Q_{G-H} \left[\frac{R_{H-pu}}{R_{H-pu} + R_{G-H}} + \frac{R_{H-pd}}{R_{H-pd} + R_{G-H}} \right] + Q_{G-L} \left[\frac{R_{L-pu}}{R_{L-pu} + R_{G-L}} + \frac{R_{L-pd}}{R_{L-pd} + R_{G-L}} \right] \right\}$$

where

- where f_{SW} = switching frequency
- V_{CC} = voltage at the V_{CC} pin
- Q_{G-H} = total gate charge of the (parallel combination of the) high-side MOSFET(s)
- Q_{G-L} = total gate charge of the (parallel combination of the) low-side MOSFET(s)
- R_{G-H} = gate resistance of the (parallel combination of the) high-side MOSFET(s)
- R_{G-L} = gate resistance of the (parallel combination of the) low-side MOSFET(S)
- R_{H-pu} = pull-up R_{DS_ON} of the high-side driver
- R_{H-pd} = pull-down R_{DS_ON} of the high-side driver
- R_{L-pu} = pull-up R_{DS_ON} of the low-side driver
- R_{L-pd} = pull-down R_{DS_ON} of the low-side driver

(1)

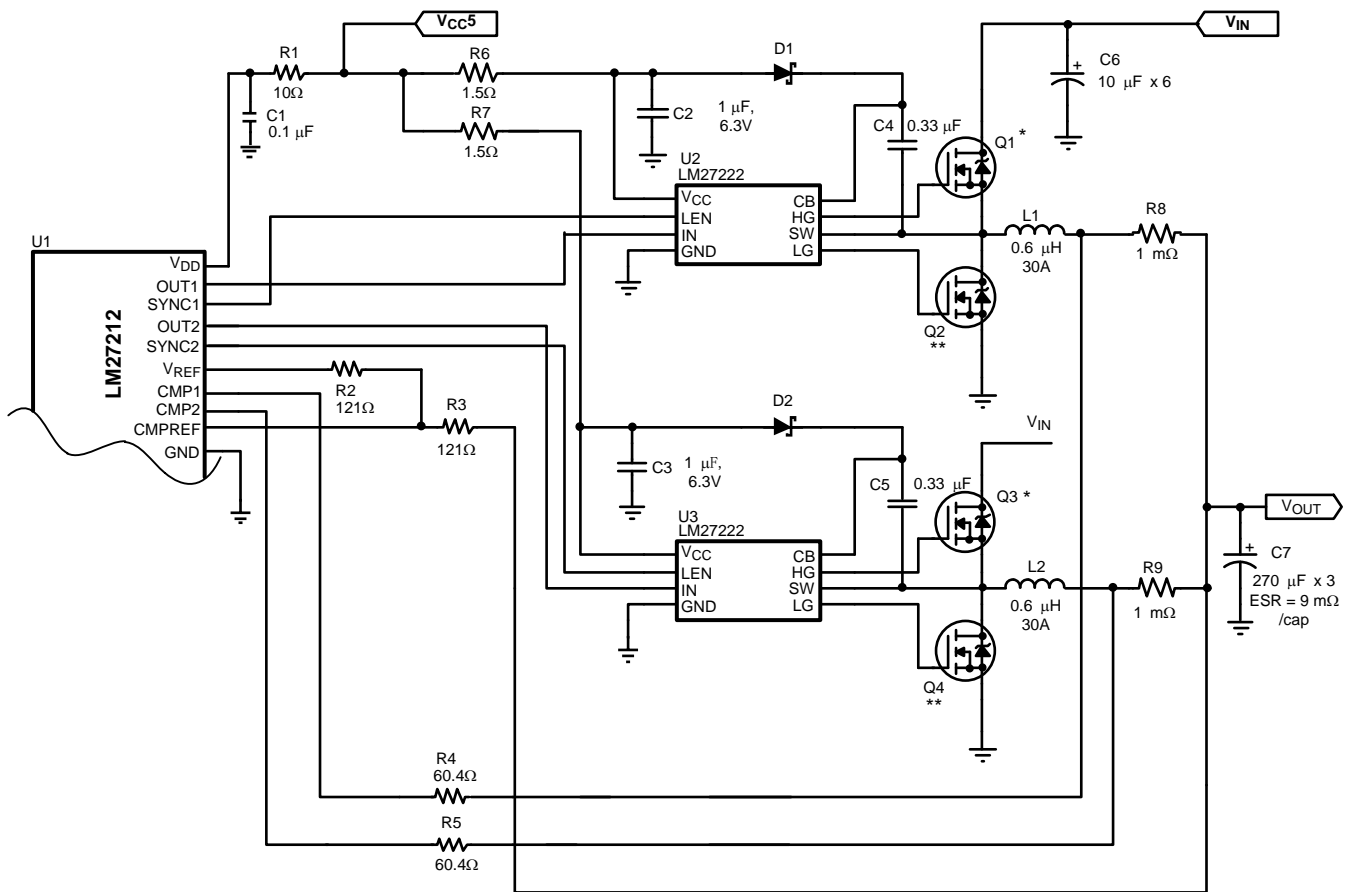
PC BOARD LAYOUT GUIDELINES

1. Place the driver as close to the MOSFETs as possible.
2. HG, SW, LG, GND: Run short, thick traces between the driver and the MOSFETs. To minimize parasitics, the traces for HG and SW should run parallel and close to each other. The same is true for LG and GND.
3. Driver V_{CC} : Place the decoupling capacitor close to the V_{CC} and GND pins.
4. The high-current loop between the high-side and low-side MOSFETs and the input capacitors should be as small as possible.
5. There should be enough copper area near the MOSFETs and the inductor for heat dissipation. Vias may also be added to carry the heat to other layers.

TYPICAL APPLICATION CIRCUIT DESCRIPITON

The Application Example on the following page shows the LM27222 being used with the LM27212, a 2-phase hysteretic current mode controller. Although this circuit is capable of operating from 5V to 28V, the components are optimized for an input voltage range of 9V to 28V. The high-side FET is selected for low gate charge to reduce switching losses. For low duty cycles, the average current through the high-side FET is relatively small and thus we trade off higher conduction losses for lower switching losses. The low-side FET is selected solely on R_{DS_ON} to minimize conduction losses. If the input voltage range were 4V to 6V, the MOSFET selection should be changed. First, much lower voltage FETs can be used, and secondly, high-side FET R_{DS_ON} becomes a larger loss factor than the switching losses. Of course with a lower input voltage, the input capacitor voltage rating can be reduced and the inductor value can be reduced as well. For a 4V to 6V application, the inductor can be reduced to 200nH to 300nH. The switching frequency of the LM27212 is determined by the allowed ripple current in the inductor. This circuit is set for approximately 300kHz. At lower input voltages, higher frequencies are possible without suffering a significant efficiency loss. Although the LM27222 can support operating frequencies up to 2MHz in many applications, the LM27212 should be limited to about 1MHz. The control architecture of the LM27212 and the low propagation times of the LM27222 potentially gives this solution the fastest transient response in the industry.

Application Example



* Q1, Q3: 2 x Si7390DP
 ** Q2, Q4: 2 x Si7356DP

REVISION HISTORY

| Changes from Revision A (March 2013) to Revision B | Page |
|--|----------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 8 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM27222M | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | 27222 M | |
| LM27222M/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | 27222 M | Samples |
| LM27222MX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | 27222 M | Samples |
| LM27222SD/NOPB | ACTIVE | WSO8 | NGT | 8 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L27222S | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM27222MX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM27222SD/NOPB | WSO | NGT | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

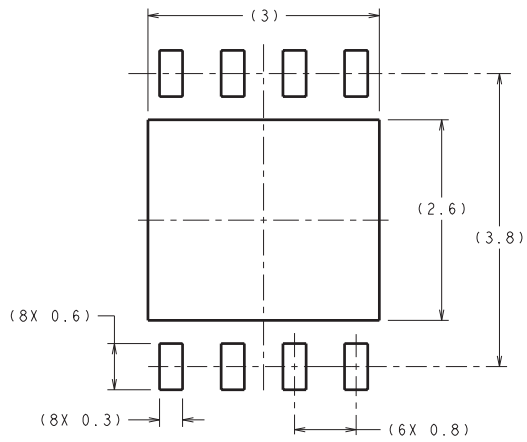
TAPE AND REEL BOX DIMENSIONS



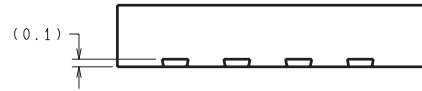
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM27222MX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM27222SD/NOPB | WSON | NGT | 8 | 1000 | 210.0 | 185.0 | 35.0 |

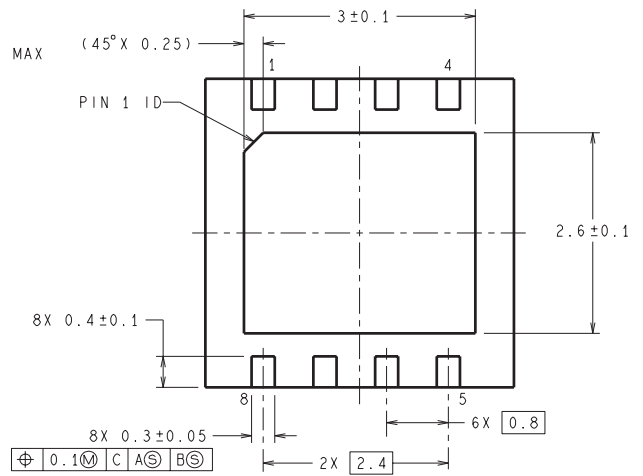
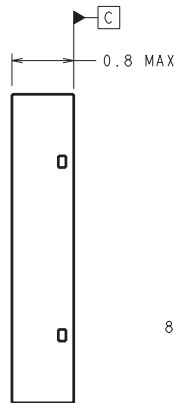
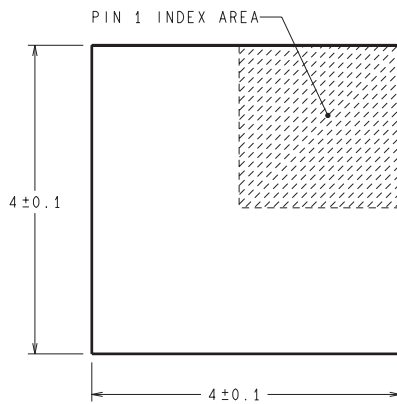
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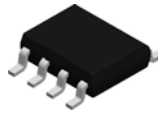
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



SDC08A (Rev A)



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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