Power MOSFETS

DATASHEET

LM2AB25NHK8A

N-Channel

Enhancement Mode MOSFET

Leadpower-semiconductor Corp., Ltd

sales@leadpower-semi.com

(03) 6577339 FAX：(03) 6577229

www.leadpower-semi.com

Quality Management Systems

ISO 9001:2015 Certificate

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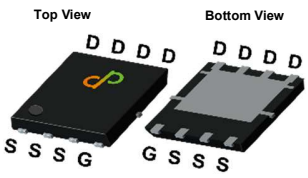
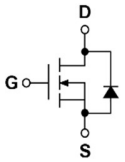
N-Channel Enhancement Mode MOSFET

Pin Description

PDFN5*6



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	200	V
$R_{DS(ON)-Max}$	225	mΩ
ID	9.8	A

Feature

- Lower Qg and Qgd for high-speed switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- DC-DC Converter
- Motor Control

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM2AB25NHK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	2AB25 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V_{DSS}	Drain-Source Voltage		200	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_C=25°C	45.5	A
I_{DM}①	Pulse Drain Current Tested	T_C=25°C	24.5	A
I_D	Continuous Drain Current	T_C=25°C	9.8	A
		T_C=100°C	6.2	
P_D	Maximum Power Dissipation	T_C=25°C	50	W
		T_C=100°C	20	
I_D	Continuous Drain Current	T_A=25°C	2.2	A
		T_A=70°C	1.8	
P_D	Maximum Power Dissipation	T_A=25°C	2.5	W
		T_A=70°C	1.6	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	4.5	A
		L=0.5mH	4	
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	1	mJ
		L=0.5mH	4	

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	2.5	°C/W
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	50	°C/W

Note ①：Max. current is limited by bonding wire

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C

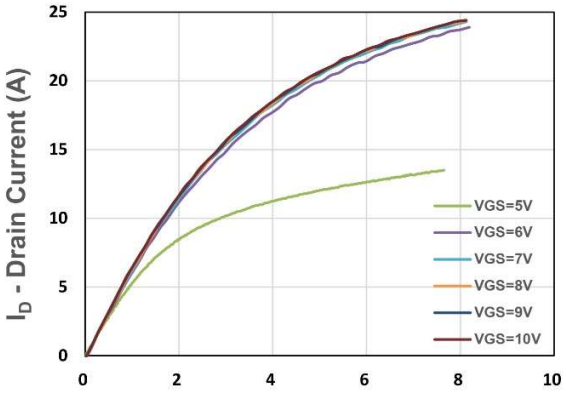
Note ③：Surface Mounted on 1in^2 FR-4 board with 1oz

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	200	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=160V, V_{GS}=0V	-	-	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250uA	2	3	4	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=9A	-	188	225	mΩ
gfs	Forward Transconductance	V_{DS}=4.5V, I_{DS}=10A	-	4.2	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	3.8	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=100V, Freq.=1MHz	-	709	-	pF
C_{oss}	Output Capacitance		-	43	-	
C_{rss}	Reverse Transfer Capacitance		-	24	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=10V,V_{DS}=30V, I_D=1A,R_{GEN}=6Ω	-	6.2	-	nS
t_r	Turn-on Rise Time		-	17.2	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	26.7	-	
t_f	Turn-off Fall Time		-	67.7	-	
Q_g	Total Gate Charge	V_{GS}=6V,V_{DS}=100V I_D=9A	-	11	-	nC
Q_g	Total Gate Charge	V_{GS}=10V,V_{DS}=100V, I_D=9A	-	16.9	-	
Q_{gs}	Gate-Source Charge		-	4	-	
Q_{gd}	Gate-Drain Charge		-	5.7	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=4.5A, V_{GS}=0V	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	I_F=4.5A, V_R=100V dI$_F$/dt=100A/μs	-	72	-	nS
Q_{rr}	Reverse Recovery Charge		-	236	-	nC

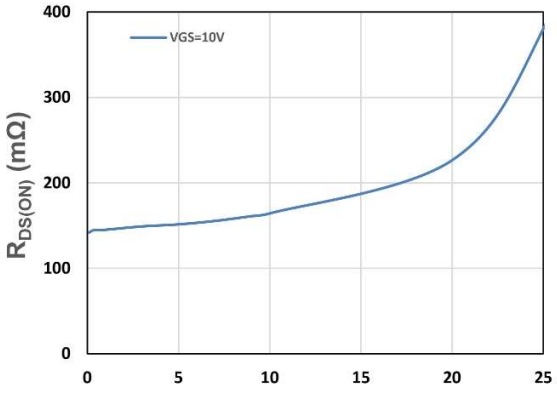
Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics



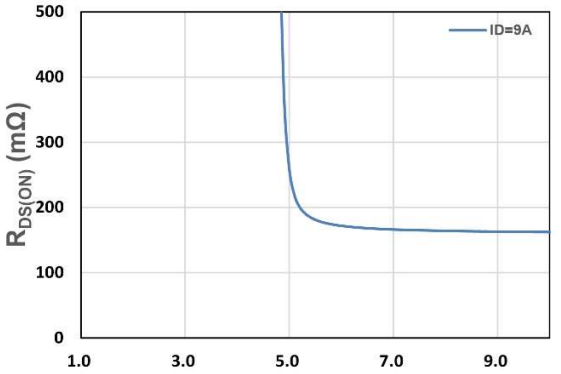
V_{DS} - Drain - Source Voltage (V)

Figure 1. Output Characteristics



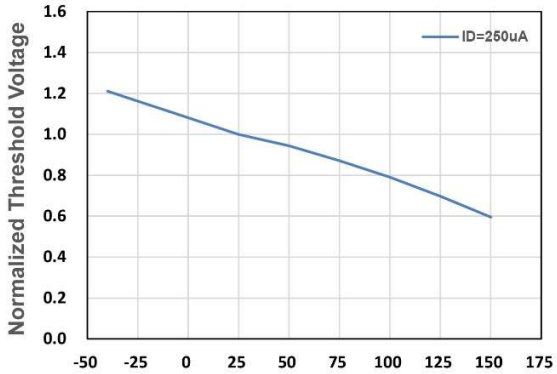
I_D- Drain Current (A)

Figure 2. On-Resistance vs. ID



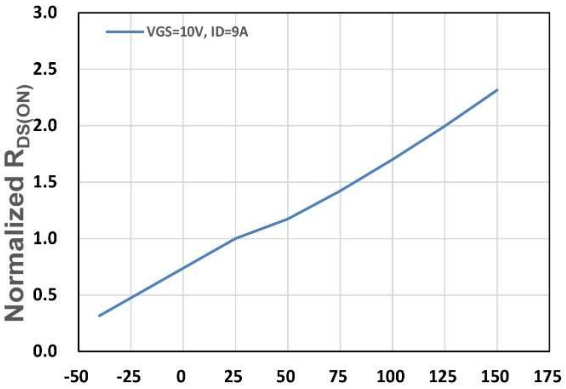
V_{GS} - Gate - Source Voltage (V)

Figure 3. On-Resistance vs. VGS



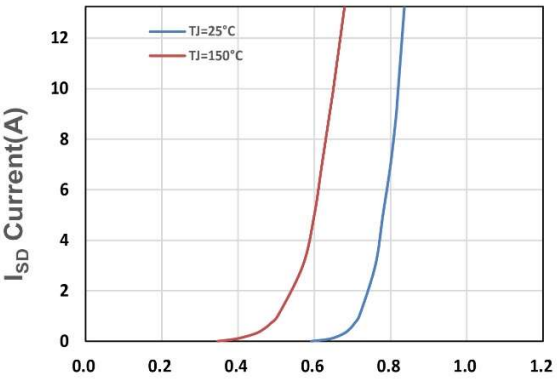
Tj, Junction Temperature(˚C)

Figure 4. Gate Threshold Voltage



Tj , Junction Temperature(˚C)

Figure 5. Drain-Source On Resistance



V_{SD}, Source-Drain Voltage(V)

Figure 6. Source-Drain Diode Forward

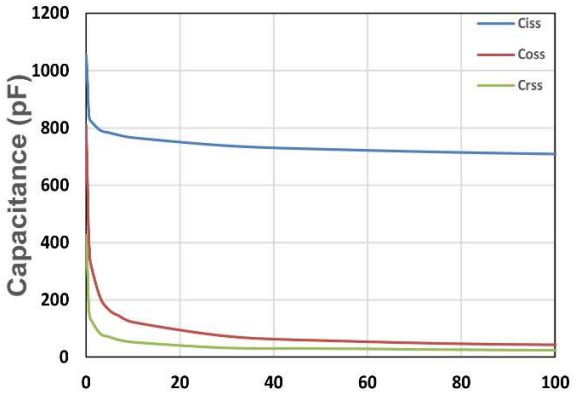


Figure 7. Capacitance

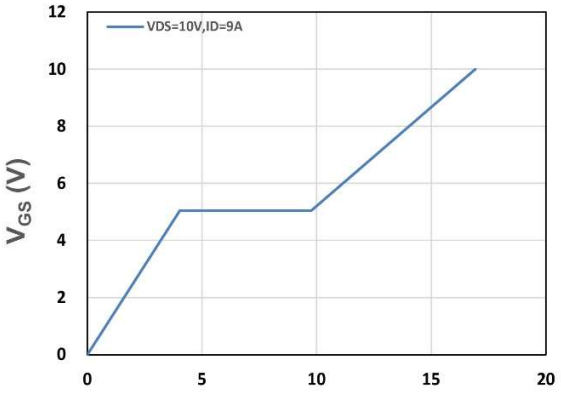


Figure 8. Gate Charge Characteristics

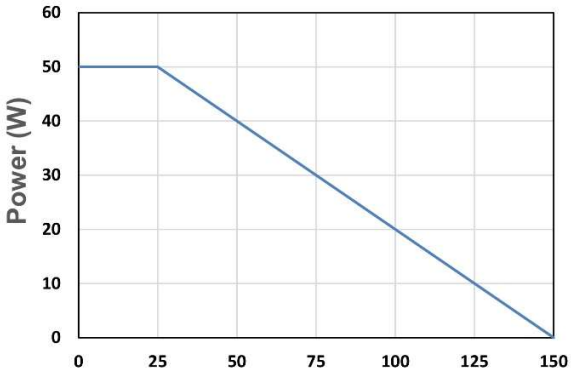


Figure 9. Power Dissipation

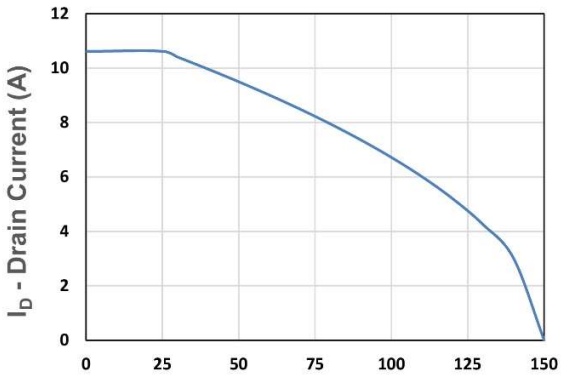


Figure 10. Drain Current

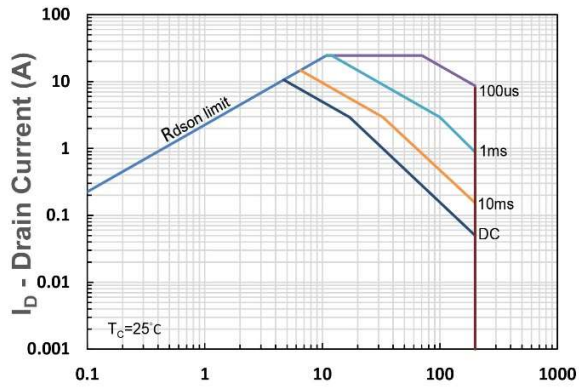


Figure 11. Safe Operating Area

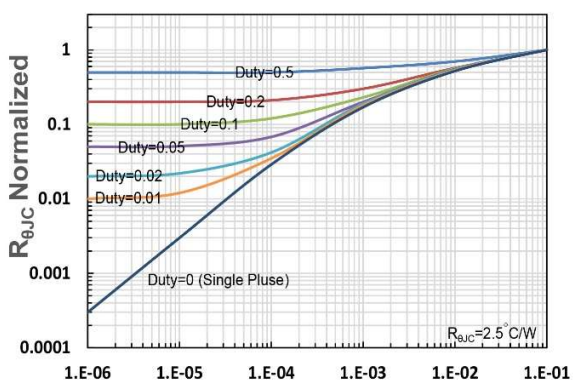


Figure 12. RθJC Transient Thermal Impedance