Voltage Comparators

LM139A/LM239A/LM339A low offset voltage quad comparators

general description

The LM139A series consists of four independent precision voltage comparators with an offset voltage specification of 2 mV max. for all four comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139A series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM339A will directly interface with MOS logic—where the low power drain of the LM339A is a distinct advantage over standard comparators.

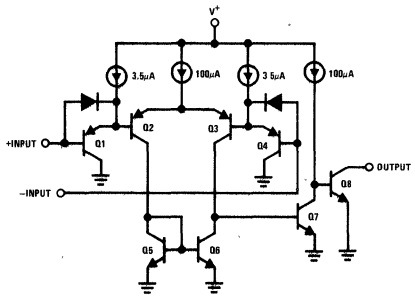
advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

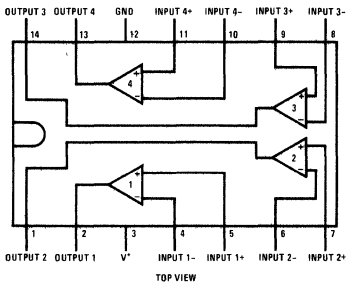
features

- Wide single supply
  Voltage range $2\,V_{DC}$ to $36\,V_{DC}$
  or dual supplies $\pm1\,V_{DC}$ to $\pm18\,V_{DC}$
- Very low supply current drain (0.8 mA)—independent of supply voltage (1 mW/comparator at $+5\,V_{DC}$)
- Low input biasing current 35 nA
- Low input offset current 3 nA
  and maximum offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5μA
  saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams

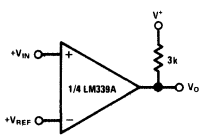


Dual-In-Line and Flat Package

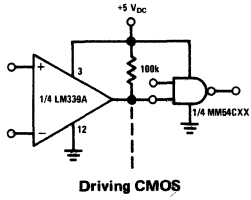


Order Number LM139AF
See Package 4
Order Number LM139AD, LM239AD or LM339AD
See Package 1
Order Number LM339AN
See Package 22

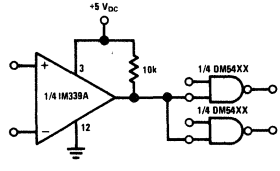
typical applications ($V^+ = 5.0\,V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

absolute maximum ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP (LM339AN)	570 mW
Cavity DIP (LM139AD, LM239AD, and LM339AD)	900 mW
Flat Pack (LM139AF)	800 mW
Output Short-Circuit to GND (Note 2)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA
Operating Temperature Range	
LM339A	0°C to +70°C
LM239A	−25°C to +85°C
LM139A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($V^+ = +5.0\ V_{DC}$, see Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = +25°C$ (Note 9)		±1	±2 0		±1	±2.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = +25°C$		25	100		25	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = +25°C$		±3	±25		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	$T_A = +25°C$	0		V^+−1 5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators $T_A = +25°C$		0 8	2.0		0 8	2.0	mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $T_A = +25°C$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing)	50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = +1.4\ V_{DC}$, $V_{\overline{R}_L} = 5\ V_{DC}$, $R_L = 5\ 1\ k\Omega$ and $T_A = +25°C$		300			300		ns
Response Time (Note 7)	$V_{R_L} = 5\ V_{DC}$ and $R_L = 5\ 1\ k\Omega$, $T_A = +25°C$		1 3			1 3		µs
Output Sink Current	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$, and $V_O \leq +1.5\ V_{DC}$, $T_A = +25°C$	6 0	16		6 0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$, and $I_{SINK} \leq 4\ mA$, $T_A = +25°C$		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1\ V_{DC}$, $V_{IN(-)} = 0$ and $V_O = 5\ V_{DC}$, $T_A = +25°C$		0 1			0 1		nA_{DC}
Input Offset Voltage	(Note 9)			4 0			4 0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2 0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4\ mA$			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1\ V_{DC}$, $V_{IN(-)} = 0$ and $V_O = 30\ V_{DC}$			1 0			1 0	μA_{DC}
Differential Input Voltage (Note 8)	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used)			V^+			V^+	V_{DC}

Note 1: For operating at high temperatures, the LM339A must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient The LM239A and LM139A must be derated based on a +150°C maximum junction temperature The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction The maximum output current is approximately 20 mA independent of the magnitude of V^+

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0 3 V_{DC}.

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated With the LM239A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$

Note 5. The direction of the input current is out of the IC due to the PNP input stage This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines

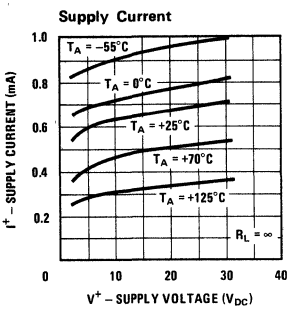
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V The upper end of the common-mode voltage range is V^+ −1.5V, but either or both inputs can go to +30 V_{DC} without damage

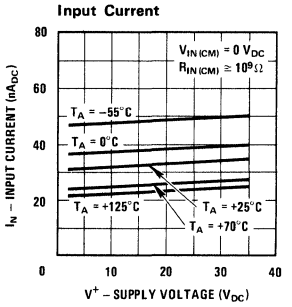
Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section

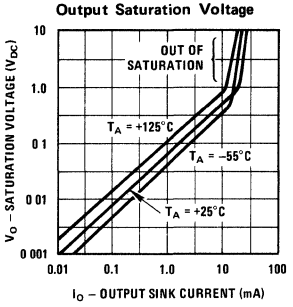
Note 8. If the voltage applied to any input exceeds V^+, all four comparator outputs will go to the high voltage level The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used)

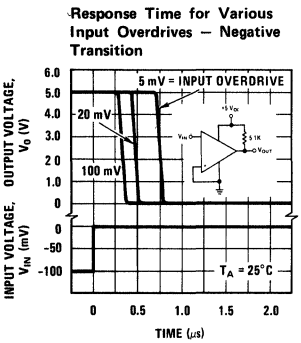
Note 9: At output switch point, $V_O \cong 1\ 4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}, and over the full input common mode range (0 V_{DC} to V^+ −1.5 V_{DC})

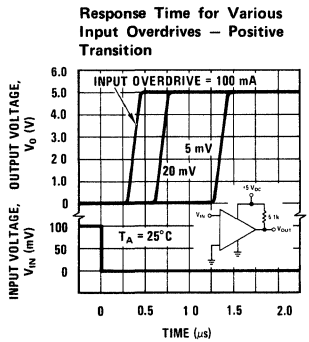
typical performance characteristics











application hints

The LM139A is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139A is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.