National Semiconductor

LM3429

PRELIMINARY
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N-Channel Controller for Constant Current LED Drivers

General Description

The LM3429 is a versatile high voltage LED driver controller. With the capability to be configured in a Buck, Boost, Buck-Boost (Flyback), or SEPIC topology, and an input and output operating voltage rating of 75V, the LM3429 is ideal for illuminating LEDs in a very diverse, large family of applications.

Adjustable high-side current sense with a typical sense voltage of 100 mV allows for tight regulation of the LED current with the highest efficiency possible. Output LED current regulation is based on peak current-mode control with predictive Off-Time Control. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

The LM3429 includes a high-voltage startup regulator that operates over a wide input range of 4.5V to 75V. The internal PWM controller is designed for adjustable switching frequencies of up to 2.0MHz, thus enabling compact solutions. Additional features include: precision reference, logic compatible DIM input suitable for fast PWM dimming, cycle-by-cycle current limit, and thermal shutdown.

The LM3429 comes in a low profile, thermally efficient TSSOP EP 14-lead package.

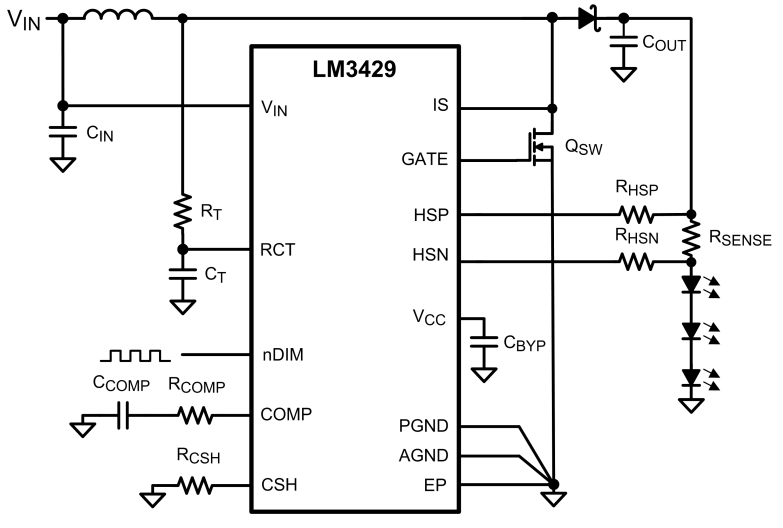
Features

- V_{IN} range from 4.5V to 75V
- 2% Internal reference voltage (1.235V)
- Current sense voltage adjustable from 20 mV
- High-side current sensing
- 2Ω MOSFET gate driver
- Dimming MOSFET gate driver
- Input under-voltage protection
- Over-voltage protection
- Low shutdown current, I_Q < 1µA
- Fast (50kHz) PWM dimming
- Cycle-by-cycle current limit
- Programmable switching frequency
- TSSOP EP 14-lead package

Applications

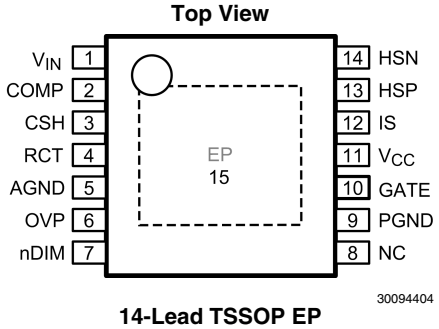
- LED Drivers
- Constant-Current Buck-Boost Regulator
- Constant-Current Boost Regulator
- Constant-Current Flyback Regulator
- Constant-Current SEPIC Regulator
- Thermo-Electric Cooler (Peltier) Driver

Typical Application Circuit



Boost LED Driver

Connection Diagram



14-Lead TSSOP EP
NS Package Number MXA14A

Ordering Information

Order Number	Spec.	Package Type	NSC Package Drawing	Supplied As
LM3429MH	NOPB	TSSOP-14 EP	MXA14A	92 Units, Rail
LM3429MHX	NOPB	TSSOP-14 EP	MXA14A	2500 Units, Tape and Reel

Pin Descriptions

LM3429	Name	Function
1	V_{IN}	Power supply input (4.5V-75V). Bypass with 100nF capacitor to AGND as close to the device as possible in the circuit board layout.
2	COMP	Compensation: PWM controller error amplifier compensation pin. This pin connects through a series resistor-capacitor network to AGND.
3	CSH	Current Sense High: Output of the high side sense amplifier and input to the main regulation loop error amplifier.
4	RCT	Resistor Capacitor Timing: External RC network sets the predictive “off-time” and thus the switching frequency. The RC network should be placed as close to the device as possible in the circuit board layout.
5	AGND	Analog Ground: The proper place to connect the compensation and timing capacitor returns. This pin should be connected via the circuit board to the PGND pin through the EP copper circuit board pad.
6	OVP	Over-Voltage Protection sense input: 1.24V threshold with hysteresis that is user programmable by the selection of the OVP Over-Voltage Lock-Out (OVLO) resistor divider network. If not used connect pin to GND.
7	nDIM	Not DIM input: Dual function pin. Primarily used as the Pulse Width Modulation (PWM) input. When driven with a resistor divider from V_{IN}, this pin also functions as a user programmable V_{IN} Under-Voltage Lock-Out (UVLO) with 1.24V threshold and programmable hysteresis by the UVLO resistor divider network. The PWM and UVLO functions can be performed simultaneously.
8	NC	No connection. Leave this pin open.
9	PGND	Power Ground: GATE and DDRV gate drive ground current return pin. This pin should be connected via the circuit board to the AGND pin through the EP copper circuit board pad.
10	GATE	Main switching MOSFET gate drive output.
11	V_{CC}	Internal Regulator Bypass: 6.9V low dropout linear regulator output. Bypass with a 2.2 µF–3.3 µF, ceramic type capacitor to PGND.
12	IS	Main Switch Current Sense input: This pin is used for current mode control and cycle-by-cycle current limit. This pin can be tied to the drain of the main N-channel MOSFET switch for $R_{DS(ON)}$ sensing or tied to a sense resistor installed in the source of the same device.
13	HSP	High Side Sense Positive: LED current sense positive input. An external resistor sets a reference current flowing into this pin from the programmed high-side sense voltage. Although the current into this pin can be set to values ranging from 10 µA through 1 mA, a value of 100 µA is recommended. This pin is a virtual ground whose potential is set by the voltage on the HSN pin.

LM3429	Name	Function
14	HSN	High Side Sense Negative: This pin sets the reference voltage for the HSP input. An external resistor of the same value as that used on the HSP pin should be connected from this pin to the negative side of the current sense resistor.
EP (15)	EP	EP: Star ground, connecting AGND and PGND. For thermal considerations please refer to (Note 4) of the Electrical Characteristics table.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, nDIM	-0.3V to 76.0V -1mA continuous
OVP, HSP, HSN	-0.3V to 76.0V -100 µA continuous
RCT	-0.3V to 76.0V -1 mA to +5 mA continuous
IS	-0.3V to 76.0V -2V for 100 ns -1 mA continuous
V_{CC}	-0.3V to 8.0V
COMP, CSH	-0.3V to 6.0V -200 µA to +200 µA Continuous
GATE	-0.3V to V_{CC} -2.5V for 100 ns V_{CC}+2.5V for 100 ns -1 mA to +1 mA continuous
PGND	-0.3V to 0.3V -2.5V to 2.5V for 100 ns
Maximum Junction Temperature (Internally Limited)	165°C
Storage Temperature Range	–65°C to +150°C
Maximum Lead Temperature (Soldering) (Note 5)	300°C
Continuous Power Dissipation (Note 4)	Internally Limited
ESD Susceptibility (Note 6)	
Human Body Model	2 kV

Operating Conditions (Notes 1, 2)

Operating Junction Temperature Range (Note 7)	–40°C to +150°C
Input Voltage V_{IN}	4.5V to 75V

Electrical Characteristics (Note 2)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = –40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions	**Min** (Note 7)	**Typ** (Note 8)	**Max** (Note 7)	Units
STARTUP REGULATOR						
V_{CCREG}	V_{CC} Regulation	I_{CC} = 0 mA	**6.30**	6.90	**7.35**	V
I_{CCLIM}	V_{CC} Current Limit	V_{CC} = 0V	**20**	25		mA
I_Q	Quiescent Current	Static		1.5	**3**	mA
V_{CC} SUPPLY						
V_{CCUV}	V_{CC} UVLO Threshold	V_{CC} Increasing		4.17	**4.50**	V
		V_{CC} Decreasing	**3.70**	4.08		V
V_{CCHYS}	V_{CC} UVLO Hysteresis			0.1		V
OV THRESHOLDS						
OVP_{CB}	OVP OVLO Threshold	OVP Increasing	**1.185**	1.240	**1.285**	V
OVP_{HYS}	OVP Hysteresis Source Current	OVP Active (high)	**10**	20	**30**	µA
ERROR AMPLIFIER						
V_{REF}	CSH Reference Voltage	With Respect to AGND	**1.210**	1.235	**1.260**	V
	Error Amplifier Input Bias Current		-0.6	0	0.6	µA
	COMP Sink / Source Current		**10**	26	**40**	µA
	Transconductance			100		µA/V
	Linear Input Range	(Note 9)		±125		mV
	Transconductance Bandwidth (Note 9)	-6dB Unloaded Response	0.5	1.0		MHz
OFF TIMER						
	Minimum Off-time	RCT = 1V through 1 kΩ		35	**75**	ns
R_{RCT}	RCT Reset Pull-down Resistance			36	**120**	Ω
V_{RCT}	V_{IN}/25 Reference Voltage	V_{IN} = 14V	**540**	565	**585**	mV

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 8)	Max (Note 7)	Units
f	Continuous Conduction Switching Frequency	2.2 nF > C_T > 470 pF		25/($C_T R_T$)		Hz
PWM COMPARATOR						
	COMP to PWM Offset		**700**	800	**900**	mV
CURRENT LIMIT (IS)						
I_{LIM}	Current Limit Threshold		**215**	245	**275**	mV
	I_{LIM} Delay to Output			35	**75**	ns
	Leading Edge Blanking Time		**75**	250	**450**	
HIGH SIDE TRANSCONDUCTANCE AMPLIFIER						
	Input Bias Current			10		µA
	Transconductance		**20**	119		mA/V
	Input Offset Current		**-1.5**	0	**1.5**	µA
	Input Offset Voltage		**-7**	0	**7**	mV
	Transconductance Bandwidth (Note 9)	I_{CSH} = 100 µA	250	500		kHz
GATE DRIVER (GATE)						
$R_{SRC(GATE)}$	GATE Sourcing Resistance	GATE = High		2.0	**6.0**	Ω
$R_{SNK(GATE)}$	GATE Sinking Resistance	GATE = Low		1.3	**4.5**	
DIM DRIVER (nDIM)						
$nDIM_{VTH}$	nDIM / UVLO Threshold		**1.180**	1.240	**1.280**	V
$nDIM_{HYS}$	nDIM Hysteresis Current		**10**	20	**30**	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			165		°C
T_{HYS}	Thermal Shutdown Hysteresis			25		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient (Note 4)	14L TSSOP EP		38		°C/W
θ_{JC}	Junction to Exposed Pad (EP)	14L TSSOP EP		2.8		°C/W

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All voltages are with respect to the potential at the AGND pin, unless otherwise specified.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=165°C (typical) and disengages at T_J=140°C (typical).

Note 4: Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for a reference layout wherein the 14L TSSOP package has its EP pad populated with 6 vias. In applications where high maximum power dissipation exists, namely driving a large MOSFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$. In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be TBD °C/W for the 14L TSSOP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

Note 5: Refer to National's packaging website for more detailed information and mounting techniques. http://www.national.com/packaging/

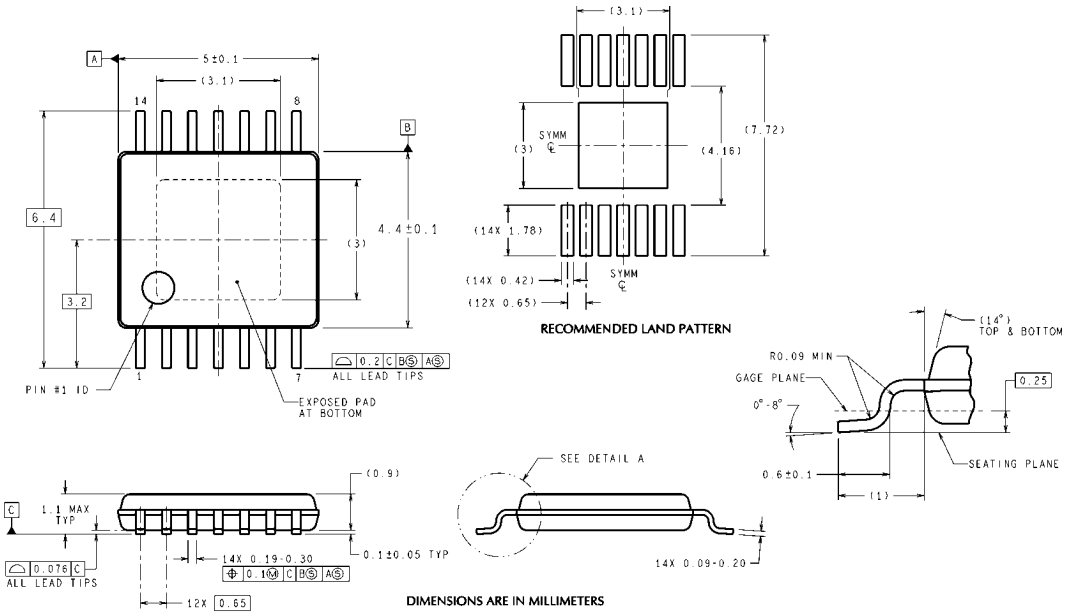
Note 6: Human Body Model, applicable std. JESD22-A114-C.

Note 7: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 8: Typical numbers are at 25°C and represent the most likely norm.

Note 9: These electrical parameters are guaranteed by design, and are not verified by test.

Physical Dimensions inches (millimeters) unless otherwise noted



MXA14A (Rev A)

TSSOP-14 Pin EP Package (MXA)
For Ordering, Refer to Ordering Information Table
NS Package Number MXA14A

Notes

Notes

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