March 29, 2010

LM3434

Common Anode Capable High Brightness LED Driver with High Frequency Dimming

General Description

The LM3434 is an adaptive constant on-time DC/DC buck (step-down) constant current controller (a true current source). The LM3434 provides a constant current for illuminating high power LEDs. The output configuration allows the anodes of multiple LEDs to be tied directly to the ground referenced chassis for maximum heat sink efficacy. The high frequency capable architecture allows the use of small external passive components and no output capacitor while maintaining low LED ripple current. Two control inputs are used to modulate LED brightness. An analog current control input is provided so the LM3434 can be adjusted to compensate for LED manufacturing variations and/or color temperature correction. The other input is a logic level PWM control of LED current. The PWM functions by shorting out the LED with a parallel switch allowing high PWM dimming frequencies. High frequency PWM dimming allows digital color temperature control, interference blanking, field sequential illumination, and brightness control. Additional features include thermal shutdown, V_{CC} under-voltage lockout, and logic level shutdown mode. The LM3434 is available in a low profile LLP-24 package.

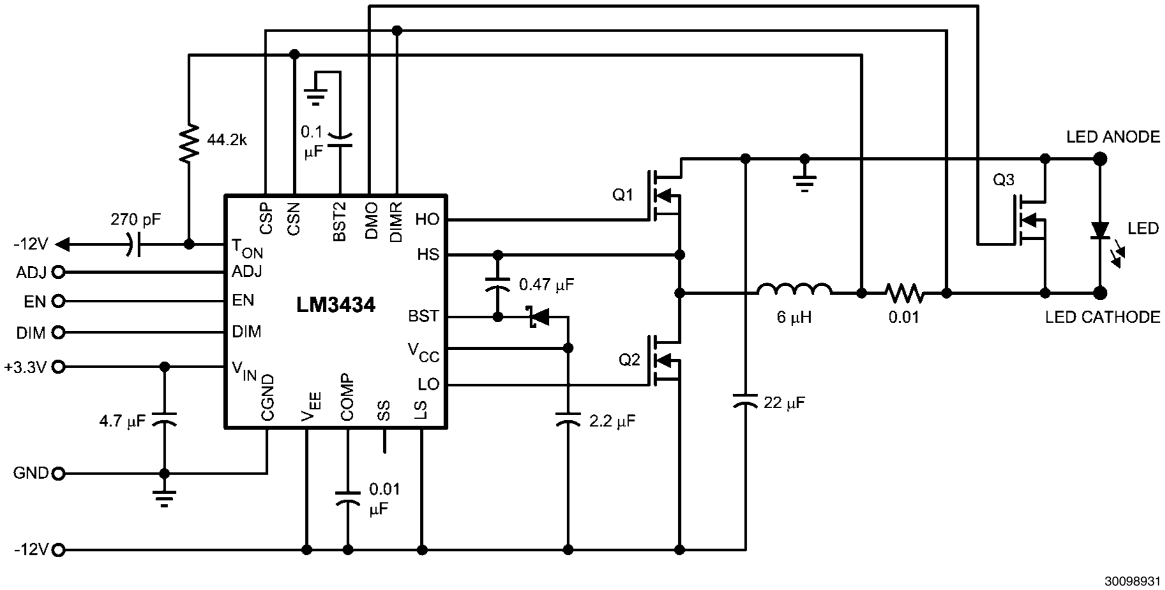
Features

- Operating input voltage range of -9V to -30V w.r.t. LED anode
- Control inputs are referenced to the LED anode
- Output current greater than 6A
- Greater than 30kHz PWM frequency capable
- Negative output voltage capability allows LED anode to be tied directly to chassis for maximum heat sink efficacy
- No output capacitor required
- Up to 1MHz switching frequency
- Low I_Q, 1mA typical
- Soft start
- Adaptive programmable ON time allows for constant ripple current
- LLP-24 package

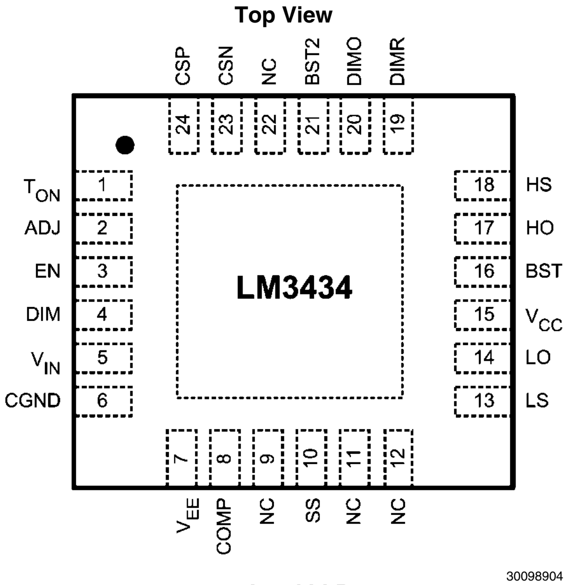
Applications

- Projection systems
- Solid state lighting
- Automotive lighting

Typical Application Circuit



Connection Diagram



24-Lead LLP
NS Package Number SQA24A

Ordering Information

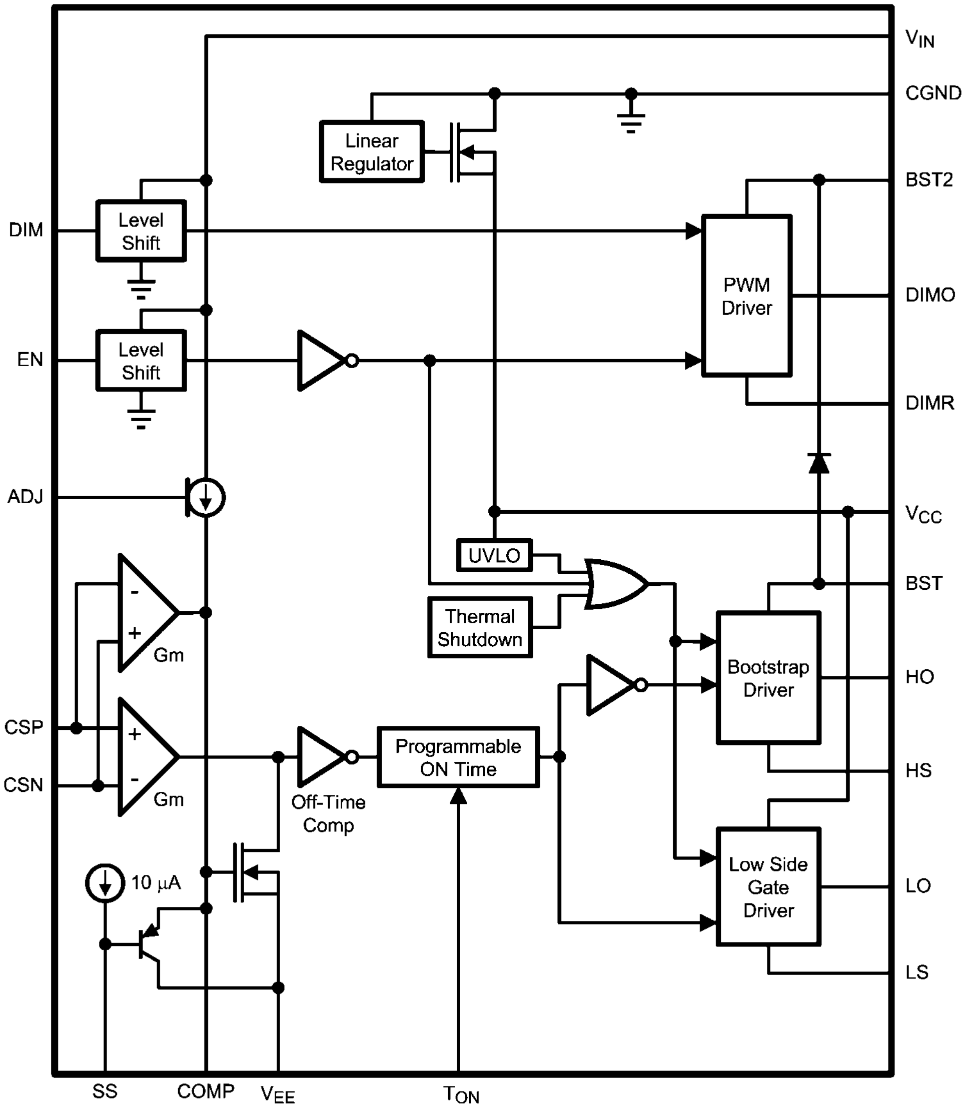
Order Number	Spec.	Package Type	NSC Package Drawing	Supplied As
LM3434SQ	NOPB	LLP-24	SQA24A	1000 Units, Tape and Reel
LM3434SQX	NOPB	LLP-24	SQA24A	4500 Units, Tape and Reel

Pin Descriptions

Pin	Name	Function
1	T_{ON}	On-time programming pin. Tie an external resistor (R_{ON}) from T_{ON} to CSN, and a capacitor (C_{ON}) from T_{ON} to V_{EE}. This sets the nominal operating frequency when the LED is fully illuminated.
2	ADJ	Analog LED current adjust. Tie to V_{IN} for fixed 60mV average current sense resistor voltage. Tie to an external reference to adjust the average current sense resistor voltage (programmed output current). Refer to the "V_{SENSE} vs. ADJ Voltage" graphs in the *Typical Performance Characteristics* section and the *Design Procedure* section of the datasheet.
3	EN	Enable pin. Connect this pin to logic level HI or V_{IN} for normal operation. Connect this pin to CGND for low current shutdown. EN is internally tied to V_{IN} through a 100k resistor.
4	DIM	Logic level input for LED PWM dimming. DIM is internally tied to CGND through a 100k resistor.
5	V_{IN}	Logic power input: Connect to positive voltage between +3.0V and +5.8V w.r.t. CGND.
6	CGND	Chassis ground connection.
7	V_{EE}	Negative voltage power input: Connect to voltage between –30V to –9V w.r.t. CGND.
8	COMP	Compensation pin. Connect a capacitor between this pin and V_{EE}.
9	NC	No internal connection. Tie to V_{EE} or leave open.
10	SS	Soft Start pin. Tie a capacitor from SS to V_{EE} to reduce input current ramp rate. Leave pin open if function is not used. The SS pin is pulled to V_{EE} when the device is not enabled.
11	NC	No internal connection. Tie to V_{EE} or leave open.
12	NC	No internal connection. Tie to V_{EE} or leave open.
13	LS	Low side FET gate drive return pin.
14	LO	Low side FET gate drive output. Low in shutdown.

Pin	Name	Function
15	V_{CC}	Low side FET gate drive power bypass connection and boost diode anode connection. Tie a 2.2µF capacitor between V_{CC} and V_{EE}.
16	BST	High side "synchronous" FET drive bootstrap rail.
17	HO	High side "synchronous" FET gate drive output. Pulled to HS in shutdown.
18	HS	Switching node and high side "synchronous" FET gate drive return.
19	DIMR	LED dimming FET gate drive return. Tie to LED cathode.
20	DIMO	LED dimming FET gate drive output. DIMO is a driver that switches between DIMR and BST2.
21	BST2	DIMO high side drive supply pin. Tie a 0.1µF between BST2 and CGND.
22	NC	No internal connection. Tie to V_{EE} or leave open.
23	CSN	Current sense amplifier inverting input. Connect to current sense resistor negative terminal.
24	CSP	Current sense amplifier non-inverting input. Connect to current sense resistor positive terminal.
EP	V_{EE}	Exposed Pad on the underside of the device. Connect this pad to a PC board plane connected to V_{EE}.

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, EN, DIM, ADJ to CGND	-0.3V to +7V
COMP, SS to V_{EE}	-0.3V to +7V
BST to HS	-0.3V to +7V
V_{CC} to V_{EE}	-0.3V to +7.5V
CGND, DIMR, CSP, CSN, T_{ON} to V_{EE}	-0.3V to +33V
HS to V_{EE} (Note 2)	-0.3V to +33V
LS to V_{EE}	-0.3V to +0.3V
HO output	HS-0.3V to BST+0.3V
DIMO to DIMR	-0.3V to +7V
LO output	LS-0.3V to V_{CC} +0.3V
BST2 to V_{EE}	-0.3V to 40V
Maximum Junction Temperature	150°C
Power Dissipation(Note 3)	Internally Limited
ESD Susceptibility (Note 4)	
Human Body Model	2kV

Operating Conditions

Operating Junction Temperature Range (Note 5)	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Input Voltage V_{IN} w.r.t. CGND	3.0V to 5.8V
Input Voltage V_{EE} w.r.t. CGND	-9V to -30V
ADJ Input Voltage Range to CGND	0V to V_{IN}

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = –40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25ºC, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{EE} = -12.0V and V_{IN} = +3.3V with respect to CGND.

Symbol	Parameter	Conditions	Min(Note 5)	Typ(Note 6)	Max(Note 5)	Units
SUPPLY CURRENT						
$I_{IN}V_{EE}$	V_{EE} Quiescent Current	EN = CGND		142	**250**	µA
		EN = V_{IN}, Not Switching		1.0		mA
$I_{IN}V_{IN}$	V_{IN} Quiescent Current	EN = V_{IN}, Not Switching		450		µA
		EN = CGND		35	**71**	
OUTPUT CURRENT CONTROL						
V_{CS}	Current sense target voltage; $V_{CS} = V_{CSP} – V_{CSN}$	$V_{ADJ} = V_{IN}$	**57**	60	**63**	mV
G_{ADJ}	I_{ADJ} Gain = $(V_{ADJ}$-CGND)/ $(V_{CNP}-V_{CSN})$	V_{IN} = 3.3V, V_{ADJ} = 0.5V or 1.5V w.r.t. CGND	**15**	16.67	**18**	V/V
I_{CSN}	Isense Input Current	V_{ADJ} = 1V w.r.t. CGND		-50		µA
		$V_{ADJ} = V_{IN}$		10		
I_{CSP}	Isense Input Current	$V_{ADJ} = V_{IN}$		60		µA
		V_{ADJ} = 1V w.r.t. CGND		1		
Gm	CS to COMP Transconductance; Gm = $I_{COMP} / (V_{CSP} – V_{CSN} - V_{ADJ}/16.67)$		**0.6**	1.3	**2.2**	mS
ON TIME CONTROL						
T_{ONTH}	On time threshold	$V_{T_{ON}} - V_{EE}$ at terminate ON time event	**230**	287	**334**	mV
GATE DRIVE AND INTERNAL REGULATOR						
V_{CCOUT}	V_{CC} output regulation w.r.t. V_{EE}	I_{CC} = 0mA to 20mA	**6.3**	6.75	**7.1**	V
V_{CCILIM}	V_{CC} current limit	$V_{CC} = V_{EE}$		-110		mA
R_{OLH}	HO output low resistance	I = 50mA source		2		Ω
R_{OHH}	HO output high resistance	I = 50mA sink		3		
R_{OLL}	LO output low resistance	I = 50mA source		2		Ω
R_{OHL}	LO output high resistance	I = 50mA sink		3		
R_{OLP}	DIMO output low resistance	I = 5mA source		20		Ω
R_{OHP}	DIMO output high resistance	I = 5mA sink		30		
FUNCTIONAL CONTROL						

Symbol	Parameter	Conditions	Min(Note 5)	Typ(Note 6)	Max(Note 5)	Units
V_{INUVLO}	V_{IN} undervoltage lockout	With respect to CGND		1.4		V
V_{CCUVLO}	V_{CC} - V_{EE} undervoltage lockout thresholds	On Threshold	**6.0**	6.6	**7.0**	V
		Off threshold	**4.9**	5.4	**5.8**	
V_{EN}	Enable threshold, with respect to CGND	Device on w.r.t. CGND			**1.6**	V
		Device off w.r.t. CGND	**0.6**			
R_{EN}	Enable pin pullup resistor			100		kΩ
V_{DIM}	DIM logic input threshold	DIM rising threshold w.r.t. CGND			**1.6**	V
		DIM falling threshold w.r.t. CGND	**0.6**			
R_{DIM}	DIM pin pulldown resistor			100		kΩ
I_{ADJ}	ADJ pin current		-1.0		1.0	µA
I_{SS}	SS pin source current			10		µA
R_{SS}	SS pin pulldown resistance	EN = CGND		1.0		kΩ
AC SPECIFICATIONS						
T_{DTD}	LO and HO dead time	LO falling to HO rising dead time		26		ns
		HO falling to LO rising dead time		28		
T_{PDIM}	DIM to DIMO propagation delay	DIM rising to DIMO rising delay		96	**175**	ns
		DIM falling to DIMO falling delay		40	**160**	
THERMAL SPECIFICATIONS						
T_{JLIM}	Junction temperature thermal limit			175		°C
$T_{JLIM(hyst)}$	Thermal limit hysteresis			20		°C
θ_{JA}	LLP-24 package thermal resistance	JEDEC 4 layer board		39		°C/W

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The HS pin can go to -6V with respect to V_{EE} for 30ns and +22V with respect to V_{EE} for 50ns without sustaining damage.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ – T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=175°C (typ.) and disengages at T_J=155°C (typ).

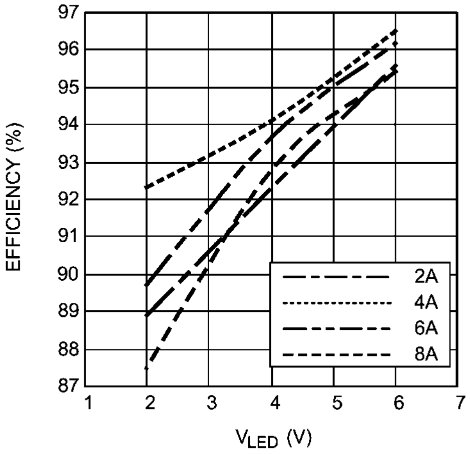
Note 4: Human Body Model, applicable std. JESD22-A114-C.

Note 5: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 6: Typical numbers are at 25°C and represent the most likely norm.

Typical Performance Characteristics

Efficiency vs. LED Forward Voltage
(V_{CGND}-V_{EE} = 9V)



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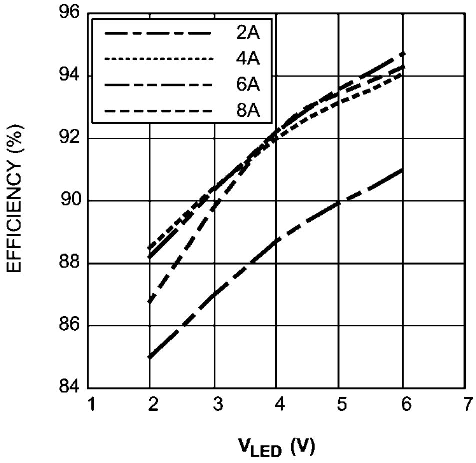
Efficiency vs. LED Forward Voltage
(V_{CGND}-V_{EE} = 12V)



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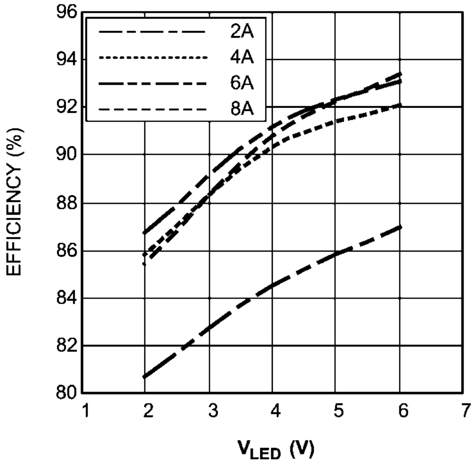
Efficiency vs. LED Forward Voltage
(V_{CGND}-V_{EE} = 14V)



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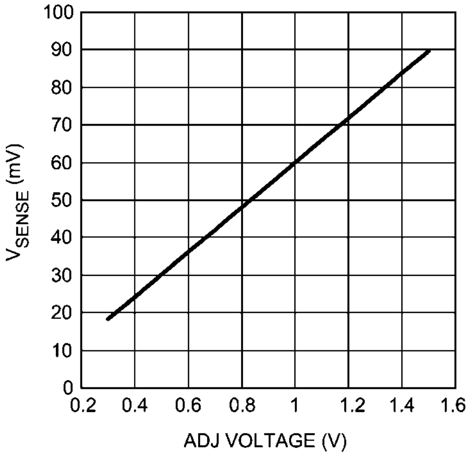
V_{SENSE} vs. V_{ADJ}
(V_{IN} = 3.3V)



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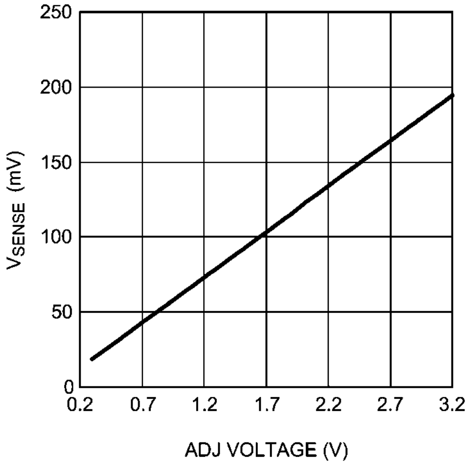
V_{SENSE} vs. V_{ADJ}
(V_{IN} = 5.0V)



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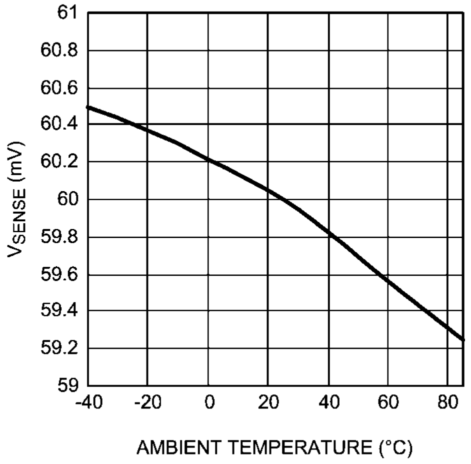
V_{SENSE} vs. Temperature
(ADJ = V_{IN})



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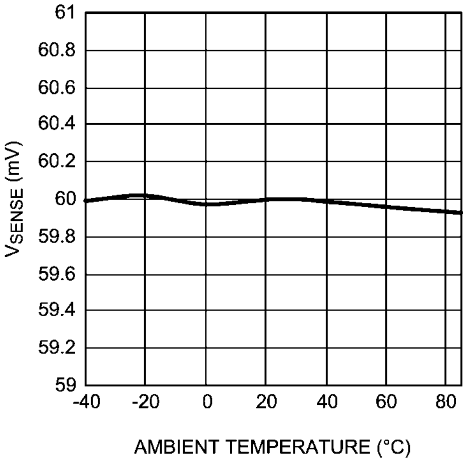
V_{SENSE} vs. Temperature (ADJ = 1.0V)



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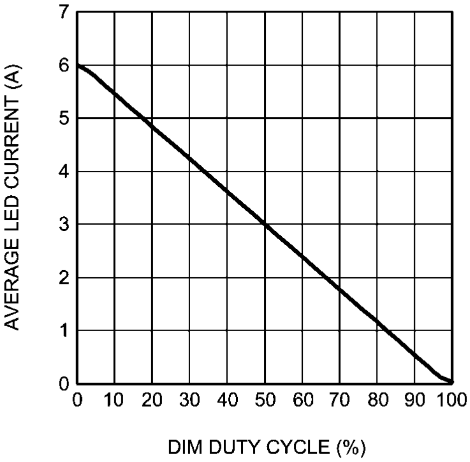
Average LED Current vs. DIM Duty Cycle (30kHz dimming, I_{LED} = 6A nominal)



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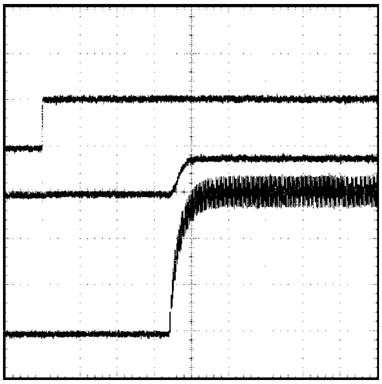
Startup Waveform



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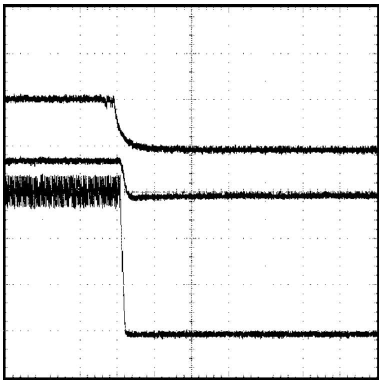
I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V, V_{LED} = 3V, SS = open
Top trace: EN input, 2V/div, DC
Middle trace: V_{EE} input current, 2A/div, DC
Bottom trace: I_{LED}, 2A/div, DC
T = 100µs/div

Shutdown Waveform



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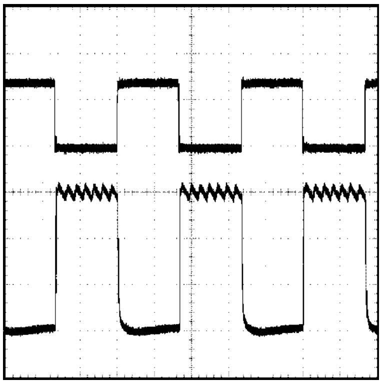
I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V, V_{LED} = 3V, SS = open
Top trace: EN input, 2V/div, DC
Middle trace: V_{EE} input current, 2A/div, DC
Bottom trace: I_{LED}, 2A/div, DC
T = 100µs/div

30kHz PWM Dimming Waveform Showing Inductor Ripple Current



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I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V
Top trace: DIM input, 2V/div, DC
Bottom trace: I_{LED}, 2A/div, DC
T = 10µs/div

Operation

CURRENT REGULATOR OPERATION

The LM3434 is a controller for a Continuous Conduction Buck Converter. Because of its buck topology and operation in the continuous mode, the output current is very well controlled. It only varies within a switching frequency cycle by the inductor ripple current. This ripple current is normally set at 10% of the DC current. Setting the ripple current lower than 10% is a useful tradeoff of inductor size for less LED light output ripple. Additional circuitry can be added to achieve any LED light ripple desired.

The LED current is set by the voltage across a sense resistor. This sense voltage is nominally 60mV but can be programmed higher or lower by an external control voltage.

The running frequency of the converter is programmed by an external RC network in conjunction with the LED's forward voltage. The frequency is nominally set around 200kHz to 500khz. Fast PWM control is available by shorting the output of the current source by a MOSFET in parallel with the LED. During the LED OFF time the running frequency is determined by the RC network and the parasitic resistance of the output circuit including the DIM FET R_{DSON}.

The LM3434 system has been evaluated to be a very accurate, high compliance current source. This is manifest in its high output impedance and accurate current control. The current is measured to vary less than 6mA out of 6A when transitioning from LED OFF (output shorted) to LED ON (output ~6V).

PROTECTION

The LM3434 has dedicated protection circuitry running during normal operation. The thermal shutdown circuitry turns off all power devices when the die temperature reaches excessive levels. The V_{CC} undervoltage lockout (UVLO) comparator protects the power devices during power supply startup and shutdown to prevent operation at voltages less than the minimum operating input voltage. The V_{CC} pin is short circuit protected to V_{EE}. The LM3434 also features a shutdown mode which decreases the supply current to approximately 35µA.

The ADJ, EN, and DIM pins are capable of sustaining up to +/-2mA. If the voltages on these pins will exceed either V_{IN} or CGND by necessity or by a potential fault, an external resistor is recommended for protection. Size this resistor to limit pin current to under 2mA. A 10k resistor should be sufficient. This resistor may be used in any application for added protection without any impact on function or performance.

DESIGN PROCEDURE

This section presents guidelines for selecting external components.

SETTING LED CURRENT CONTROL

LM3434 uses average current mode control to regulate the current delivered to the LED (I_{LED}). An external current sense resistor (R_{SENSE}) in series with the LED is used to convert I_{LED} into a voltage that is sensed by the LM3434 at the CSP and CSN pins. CSP and CSN are the inputs to an error amplifier with a programmed input offset voltage (V_{SENSE}). V_{SENSE} is used to regulate I_{LED} based on the following equation:

$$I_{LED} = V_{SENSE}/R_{SENSE}$$

FIXED LED CURRENT

The ADJ pin sets V_{SENSE}. Tie ADJ to V_{IN} to use a fixed 60mV internal reference for V_{SENSE}. Select R_{SENSE} to fix the LED current based on the following equation:

$$R_{SENSE} = 60\text{mV}/I_{LED}$$

ADJUSTABLE LED CURRENT

When tied to an external voltage the ADJ pin sets V_{SENSE} based on the following equation:

$$V_{SENSE} = (V_{ADJ} - V_{CGND})/16.667$$

When the reference on ADJ is adjustable, V_{SENSE} and I_{LED} can be adjusted within the linear range of the ADJ pin. This range has the following limitations:

$$0.3\text{V} < V_{ADJ} < (\text{The greater of } 1.5\text{V or } (V_{IN} - 1.9\text{V}))$$

When V_{ADJ} is less than this linear range the V_{SENSE} is guaranteed by design to be less than or equal to 0.3V/16.667. When V_{ADJ} is greater than this linear range and less than V_{IN} - 1V, V_{SENSE} is guaranteed by design to be less than or equal to V_{ADJ}/16.667. If V_{ADJ} is greater than V_{IN} - 1V, V_{SENSE} switches to 60mV.

INPUT CAPACITOR SELECTION

A low ESR ceramic capacitor is needed to bypass the MOSFETs. This capacitor is connected between the drain of the synchronous FET (CGND) and the source of the main switch (V_{EE}). This capacitor prevents large voltage transients from appearing at the V_{EE} pin of the LM3434. Use a 22µF value minimum with X5R or X7R dielectric. In addition to the FET bypass capacitors, additional bypass capacitors should be placed near the V_{EE} and V_{IN} pins and should be returned to CGND.

The input capacitor must also be sized to handle the dimming frequency input ripple when the DIM function is used. This ripple may be as high as 85% of the nominal DC input current (at 50% duty cycle). When dimming this input capacitor should be selected to handle the input ripple current.

RECOMMENDED OPERATING FREQUENCY AND ON TIME "TIME$_{ON}$" CALCULATION

Although the switching frequency can be set over a wide range, the following equation describes the recommended frequency selection given inexpensive magnetic materials available today:

$$f = \frac{A}{\sqrt{I_{LED}}}\ (\text{MHz})$$

In the above equation A=1.2 for powdered iron core inductors and A=0.9 or less for ferrite core inductors. This difference takes into account the fact that ferrite cores generally become more lossy at higher frequencies. Given the switching frequency f calculated above, TIME$_{ON}$ can be calculated. If V_{LED} is the forward voltage drop of the LED that is being driven, TIME$_{ON}$ can be calculated with the following equation:

$$\text{TIME}_{ON} = \frac{V_{LED}}{f|V_{EE}|}$$

TIMING COMPONENTS (R_{ON} and C_{ON})

Using the calculated value for $TIME_{ON}$, the timing components R_{ON} and C_{ON} can be selected. C_{ON} should be large enough to dominate the parasitic capacitance of the T_{ON} pin. A good C_{ON} value for most applications is 1nF. Based on calculated $TIME_{ON}$, C_{ON}, and the nominal V_{EE} and V_{LED} voltages, R_{ON} can be calculated based on the following equation:

$$R_{ON} = \frac{TIME_{ON}}{C_{ON}(0.3/(|V_{EE}|-V_{LED}))}$$

INDUCTOR SELECTION

The most critical inductor parameters are inductance, current rating, and DC resistance. To calculate the inductance, use the desired peak to peak LED ripple current (I_{RIPPLE}), R_{ON}, and C_{ON}. A reasonable value for I_{RIPPLE} is 10% of I_{LED}. The inductor value is calculated using the following equation:

$$L = \frac{0.3 \times R_{ON} \times C_{ON}}{I_{RIPPLE}}$$

For all V_{LED} and V_{EE} voltages, I_{RIPPLE} remains constant and is only dependent on the passive external components R_{ON}, C_{ON}, and L.

The I^2R loss caused by the DC resistance of the inductor is an important parameter affecting the efficiency. Lower DC resistance inductors are larger. A good tradeoff point between the efficiency and the core size is letting the inductor I^2R loss equal 1% to 2% of the output power. The inductor should have a current rating greater than the peak current for the application. The peak current is I_{LED} plus 1/2 I_{RIPPLE}.

POWER FET SELECTION

FETs should be chosen so that the I^2R_{DSON} loss is less than 1% of the total output power. Analysis shows best efficiency with around 8mΩ of R_{DSON} and 15nC of gate charge for a 6A application. All of the switching loss is in the main switch FET. An additional important parameter for the synchronous FET is reverse recovery charge (Q_{RR}). High Q_{RR} adversely affects the transient voltages seen by the IC. A low Q_{RR} FET should be used.

DIM FET SELECTION

Choose a DIM FET with the lowest R_{DSON} for maximum efficieny and low input current draw during the DIM cycle. The output voltage during DIM will determine the switching frequency. A lower output voltage results in a lower switching frequency. If the lower frequency during DIM must be bound, choose a FET with a higher R_{DSON} to force the switching frequency higher during the DIM cycle.

Placement of the Parallel Dimming FET

When using a FET in parallel with the LED for PWM dimming special consideration must be used for the location of the FET. The ideal placement of the FET is *directly* next to the LED. Any distance between this FET and the LED results in line inductance. Fast current changes through this inductance can induce large voltage spikes due to v = Ldi/dt. These can be mitigated by either reducing the distance between the FET and the LED and/or slowing the PWM edges, and therefore the dt, by using some gate resistance on the FET. In cases where the dimming FET is not placed close to the LED and/or very fast switching edges are desired the induced voltages can become great enough to damage the dimming FET and/or the LM3434 HS pin. This can also result in a large spike of current into the LED when the FET is turned off. In these cases a snubber should be placed across the dimming FET to protect the device(s).

BOOTSTRAP CAPACITORS

The LM3434 uses two bootstrap capacitors and a bypass capacitor on V_{CC} to generate the voltages needed to drive the external FETs. A 2.2µF ceramic capacitor or larger is recommended between the V_{CC} and LS pins. A 0.47µF is recommended between the HS and BST pins. A 0.1µF is recommended between BST2 and CGND.

SOFT-START CAPACITOR

The LM3434 integrates circuitry that, when used in conjunction with the SS pin, will slow the current ramp on start-up. The SS pin is used to tailor the soft-start for a specific application. A capacitor value of 0.1µF on the SS pin will yield a 12mS soft start time. For most applications soft start is not needed.

ENABLE OPERATION

The EN pin of the LM3434 is designed so that it may be controlled using a 1.6V or higher logic signal. If the enable function is not used, the EN pin may be tied to V_{IN} or left open. This pin is pulled to V_{IN} internally through a 100k pull up resistor.

PWM DIM OPERATION

The DIM pin of the LM3434 is designed so that it may be controlled using a 1.6V or higher logic signal. The PWM frequency easily accomodates more than 40kHz dimming and can be much faster if needed. If the PWM DIM pin is not used, tie it to CGND or leave it open. The DIM pin is tied to CGND internally through a 100k pull down resistor.

LAYOUT CONSIDERATIONS

The LM3434 is a high performance current driver so attention to layout details is critical to obtain maximum performance. The most important PCB board design consideration is minimizing the loop comprised by the main FET, synchronous FET, and their associated decoupling capacitor(s). Place the V_{CC} bypass capacitor as near as possible to the LM3434. Place the PWM dimming/shunt FET as close to the LED as possible. A ground plane should be used for power distribution to the power FETs. Use a star ground between the LM3434 circuitry, the synchronous FET, and the decoupling capacitor(s). The EP contact on the underside of the package must be connected to V_{EE}. The two lines connecting the sense resistor to CSN and CSP must be routed as a differential pair directly from the resistor. A Kelvin connection is recommended. It is good practice to route the DIMO/DIMR, HS/HO, and LO/LS lines as differential pairs. The most important PCB board design consideration is minimizing the loop comprised by the main FET, synchronous FET, and their associated decoupling capacitor(s). Optimally this loop should be orthogonal to the ground plane.

Application Information

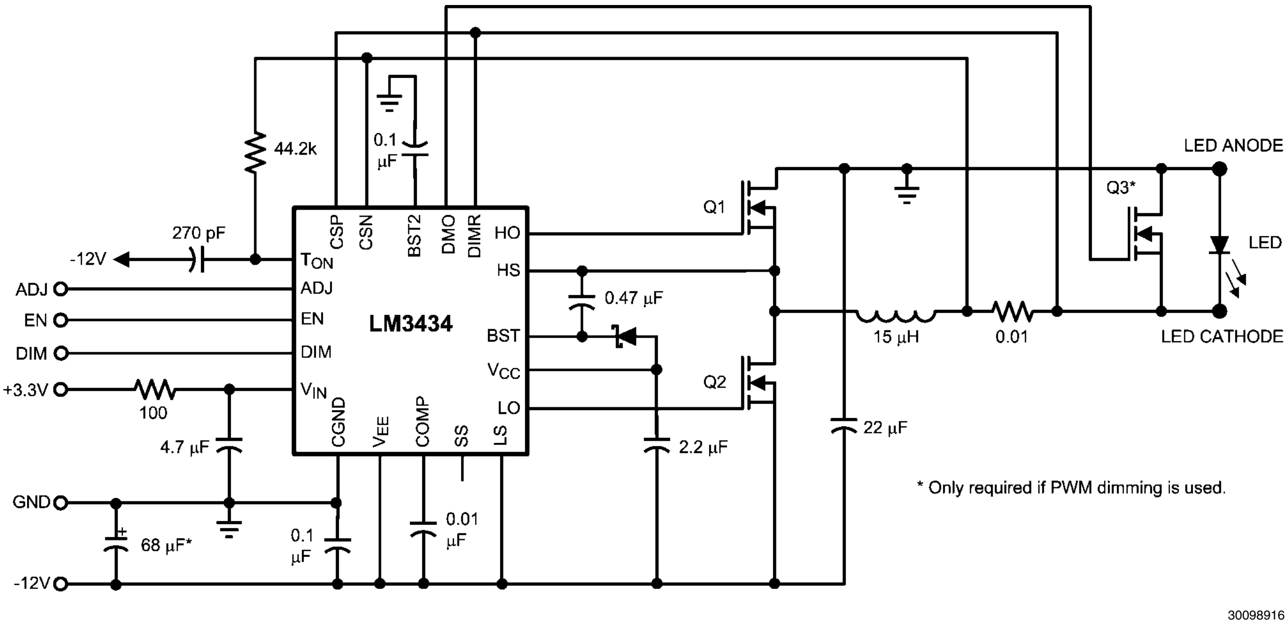


FIGURE 1. Up to 10A Output Application Circuit

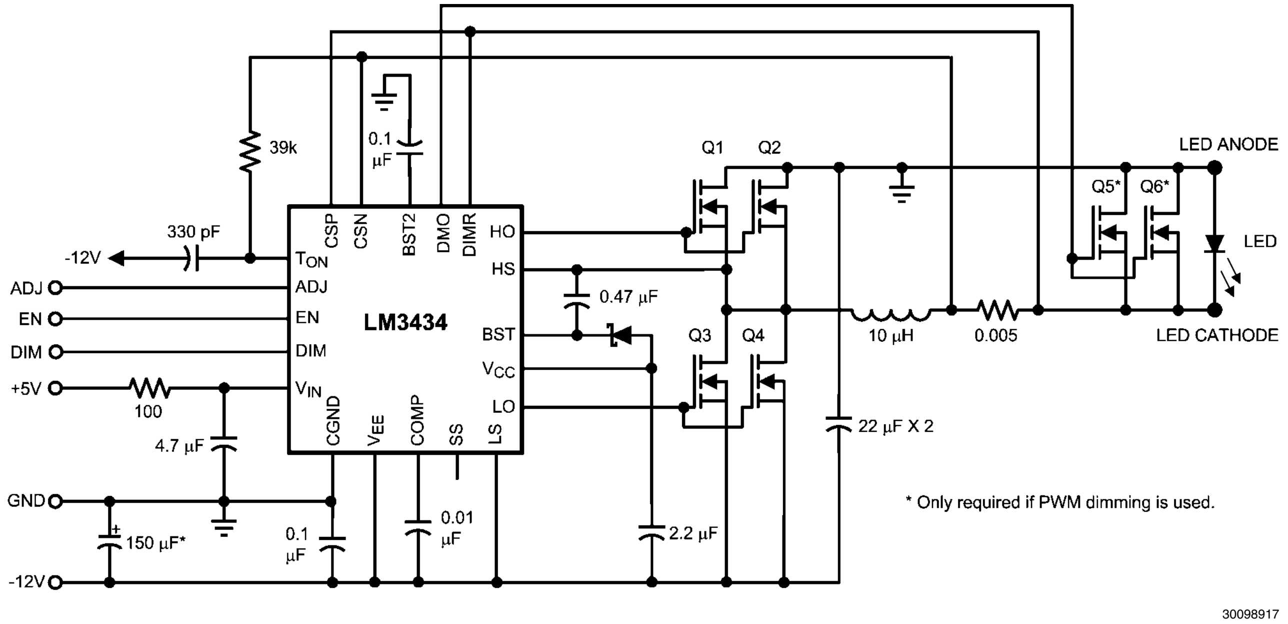


FIGURE 2. Up to 20A Output Application Circuit

Some Recommended Inductors (Others May Be Used)

Manufacturer	Inductor	Contact Information
Coilcraft	GA3252-AL series, SER1360 series, and SER2900 series	www.coilcraft.com 800-322-2645
Coiltronics	HCLP2 series	www.coiltronics.com
Pulse	PB2020 series	www.pulseeng.com

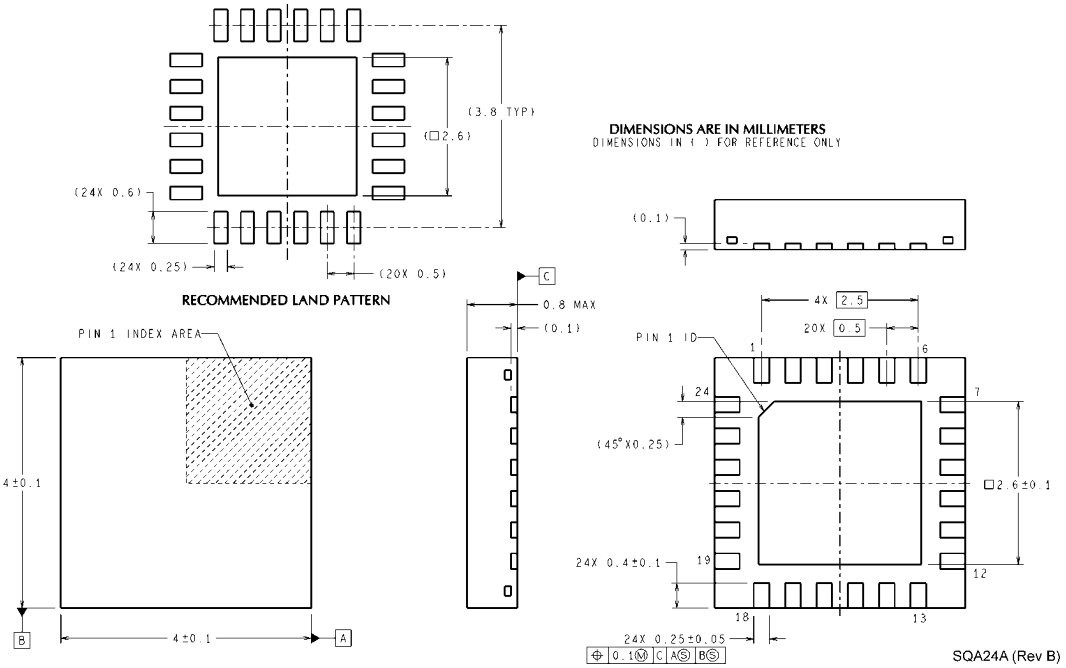
Some Recommended Input/Bypass Capacitors (Others May Be Used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com 407-324-4140
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com 408-573-4150
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
MuRata	High capacitance MLCC ceramic	www.murata.com

Some Recommended MOSFETs (Others May Be Used)

Manufacturer	MOSFET	Contact Information
Siliconix	Si7386DP (Main FET, DIM FET) Si7668ADP (Synchronous FET) Si7790DP (Main FET, Synchronous FET, DIM FET)	www.vishay.com/company/brands/siliconix/
ON Semiconductor	NTMFS4841NHT1G (Main FET, Synchronous FET, DIM FET)	www.onsemi.com

Physical Dimensions inches (millimeters) unless otherwise noted



LLP-24 Pin Package (SQA)
For Ordering, Refer to Ordering Information Table
NS Package Number SQA24A

Notes

Notes

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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
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