Operational Amplifiers

Ground Sense Operational Amplifiers

LM358F

General Description

LM358F integrate two independent Op-Amps on a single chip and features low current consumption, and wide operating voltage range of from +3V to +36V (single power supply).

Key Specification

- Operating Supply Voltage (single supply): +3.0V to +36.0V
- Temperature Range: -40°C to +85°C
- Input Offset Voltage: 4.5mV (Max)
- Input Bias Current: 20nA (Typ)

Features

- Operable with a Single Power Supply
- Wide Operating Supply Voltage Range
- Input / Output GND Sense
- High Large Signal Voltage Gain

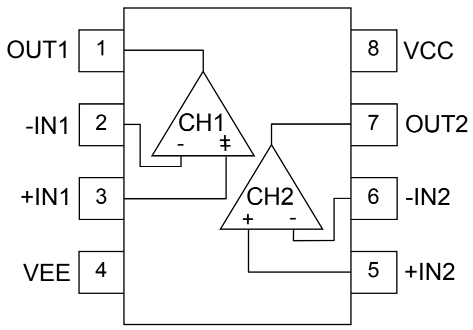
Package

Package	W(Typ) x D(Typ) x H(Max)
SOP8	5.00mm x 6.20mm x 1.71mm

Application

- Current Sense Application
- Buffer Application Amplifier
- Active Filter
- Consumer Electronics

Pin Configuration



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VEE
5	+IN2
6	-IN2
7	OUT2
8	VCC

Package
SOP8
LM358F

○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

Ordering Information

L M 3 5 8 F - E 2

Part Number	Package	Packaging and forming specification
LM358F	F : SOP8	E2: Embossed tape and reel

Line-up

T_{opr}	Channel	Input Offset Voltage (Max)	Supply Current (Typ)	Package		Orderable Part Number
-40°C to +85°C	2ch	7mV	0.5mA	SOP8	Reel of 2500	LM358F-E2

Absolute Maximum Ratings (T_A=25°C)

Parameter	Symbol		Ratings	Unit
Supply Voltage	V_{CC}-V_{EE}		+36	V
Power Dissipation	P_d	SOP8	0.68(Note 1,2)	W
Differential Input Voltage (Note 3)	V_{ID}		+36	V
Input Common-mode Voltage Range	V_{ICM}		(V_{EE}-0.3) to (V_{EE}+36)	V
Input Current(Note 4)	I_I		-10	mA
Operating Supply Voltage	V_{opr}		+3.0 to +36.0	V
Operating Temperature Range	T_{opr}		-40 to +85	°C
Storage Temperature Range	T_{stg}		-55 to +150	°C
Maximum Junction Temperature	T_{jmax}		+150	°C

(Note 1) To use at temperature above T_A=25°C reduce 5.5mW.
(Note 2) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).
(Note 3) The voltage difference between inverting input and non-inverting input is the differential input voltage.
The input pin voltage is set to more than V_{EE}.
(Note 4) An excessive input current will flow when input voltages of less than V_{EE}-0.6V are applied.
The input current can be set to less than the rated current by adding a limiting resistor.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics (Unless otherwise specified V_{CC}=+5V, V_{EE}=0V)

Parameter	Symbol	Temperature Range	Limits Min	Limits Typ	Limits Max	Unit	Condition
Input Offset Voltage(Note 5,6)	V_{IO}	25°C	-	1	4.5	mV	V_{OUT}=1.4V
		Full Range	-	-	5		V_{CC}=5 to 30V, V_{OUT}=1.4V
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	-	-	±6	-	uV/℃	V_{OUT}=1.4V
Input Offset Current(Note 5,6)	I_{IO}	25°C	-	2	50	nA	V_{OUT}=1.4V
Input Bias Current(Note 5,6)	I_B	25°C	-	20	250	nA	V_{OUT}=1.4V
Supply Current(Note 6)	I_{CC}	25°C	-	0.5	1.2	mA	R_L=∞, All Op-Amps
		Full Range	-	-	1.5		
Maximum Output Voltage(High)(Note 6)	V_{OH}	25°C	3.5	-	-	V	R_L=2kΩ
		Full Range	27	28	-		V_{CC}=30V, R_L=10kΩ
Maximum Output Voltage(Low)(Note 6)	V_{OL}	Full Range	-	5	20	mV	R_L=∞
Large Signal Voltage Gain	A_V	25°C	25	100	-	V/mV	R_L≧2kΩ, V_{CC}=15V V_{OUT}=1.4 to 11.4V
			88	100	-	dB	
Input Common-mode Voltage Range	V_{ICM}	25°C	0	-	3.5	V	V_{ICM}=V_{EE} to (V_{CC}-1.5V) V_{OUT}=1.4V
Common-mode Rejection Ratio	CMRR	25°C	65	80	-	dB	V_{OUT}=1.4V
Power Supply Rejection Ratio	PSRR	25°C	65	100	-	dB	V_{CC}=5 to 30V
Output Source Current(Note 6,7)	I_{SOURCE}	25°C	20	30	-	mA	V_{+IN}=1V, V_{-IN}=0V V_{OUT}=0V, Short Current
		Full Range	10	-	-		
Output Sink Current(Note 6,7)	I_{SINK}	25°C	20	27	-	mA	V_{+IN}=0V, V_{-IN}=1V V_{OUT}=5V, Short Current
		Full Range	5	-	-		
		25°C	12	40	-	μA	V_{+IN}=0V, V_{-IN}=1V V_{OUT}=200mV
Channel Separation	CS	25°C	-	120	-	dB	f=1kHz, Input Referred
Slew Rate	SR	25°C	-	0.3	-	V/μs	V_{CC}=15V, Av=0dB R_L=2kΩ, C_L=100pF
Gain Bandwidth	GBW	25°C	-	0.8	-	MHz	V_{CC}=30V, R_L=2kΩ C_L=100pF
Phase Margin	θ	25°C	-	80	-	deg	Av=40dB
Input Referred Noise Voltage	V_N	25°C	-	40	-	$nV/\sqrt{Hz}$	V_{CC}=15V, V_{EE}=-15V R_S=100Ω, V_{IN}=0V, f=1kHz

(Note 5) Absolute value
(Note 6) Full Range: T_A=-40°C to +85°C
(Note 7) Consider the power dissipation of the IC under high temperature when selecting the output current value.
There may be a case where the output current value is reduced due to the rise in IC temperature caused by the heat generated inside the IC.

Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Supply Voltage (V_{CC}/V_{EE})
Indicates the maximum voltage that can be applied between the VCC pin and VEE pin without deterioration or destruction of characteristics of internal circuit.

(2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting pins without damaging the IC.

(3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting pins without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

(4) Power Dissipation (P_d)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_d is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics

(1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting pin and inverting pin. It can be translated into the input voltage difference required for setting the output voltage at 0V.

(2) Input offset voltage drift ($\triangle V_{IO}/\triangle T$)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

(3) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting pins.

(4) Input Bias Current (I_B)
Indicates the current that flows into or out of the input pin. It is defined by the average of input bias currents at the non-inverting and inverting pins.

(5) Supply Current (I_{CC})
Indicates the current that flows within the IC under specified no-load conditions.

(6) Maximum Output Voltage(High) / Maximum Output Voltage(Low) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage high and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

(7) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting pin and inverting pin. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output Voltage) / (Differential Input Voltage)

(8) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

(9) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common-mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input Common-mode Voltage)/(Input Offset Fluctuation)

(10) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of Power Supply Voltage)/(Input Offset Fluctuation)

(11) Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

(12) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

(13) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.

(14) Gain Bandwidth (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.

(15) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.

(16) Input Referred Noise Voltage (V_N)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input pin.

Typical Performance Curves

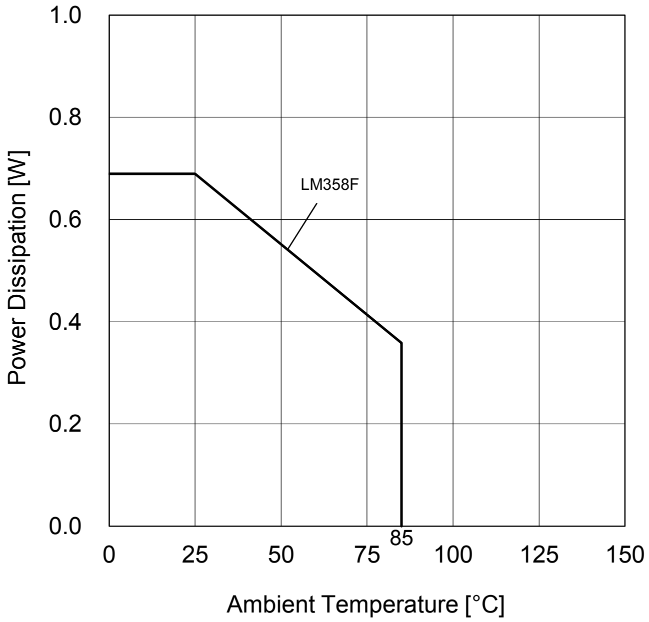


Figure 1. Power Dissipation vs Ambient Temperature
(Derating Curve)

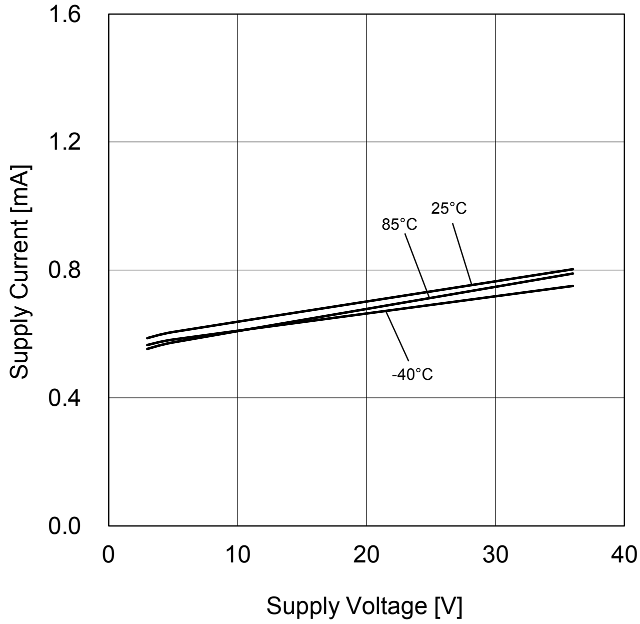


Figure 2. Supply Current vs Supply Voltage

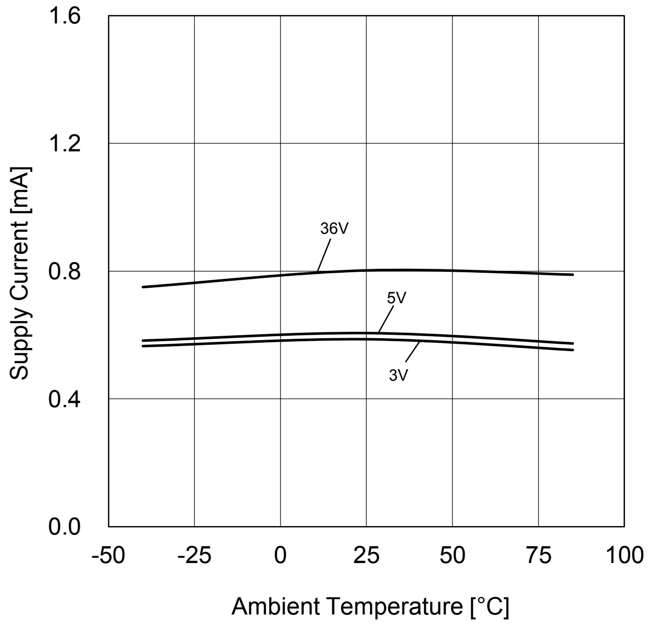


Figure 3. Supply Current vs Ambient Temperature

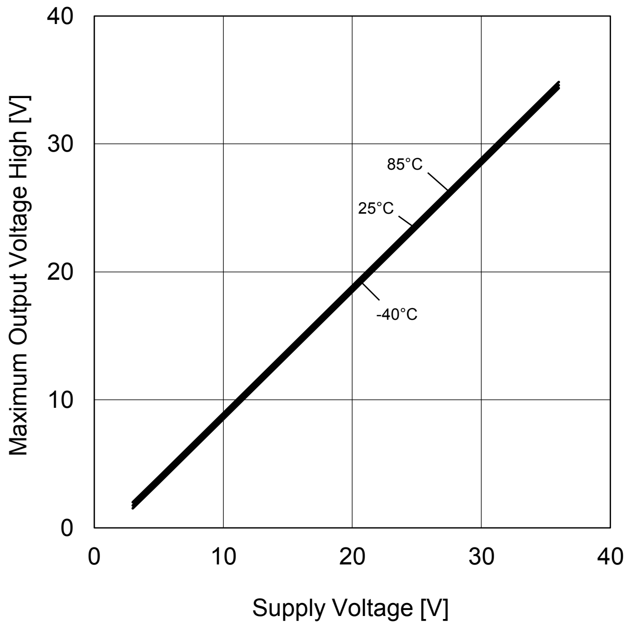


Figure 4. Maximum Output Voltage (High)
vs Supply Voltage (R_L=10kΩ)

(*) The above data are measurement value of typical sample, they are not guaranteed.

Typical Performance Curves - continued

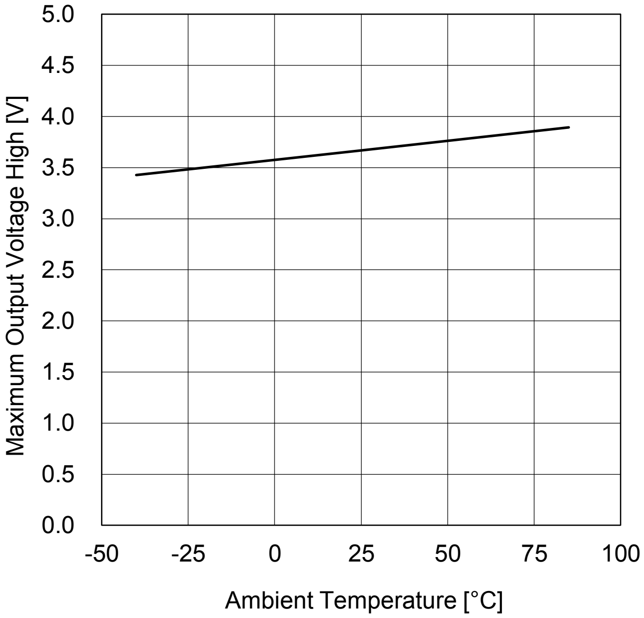


Figure 5. Maximum Output Voltage (High)
vs Ambient Temperature (V_{CC}=5V, R_L=2kΩ)

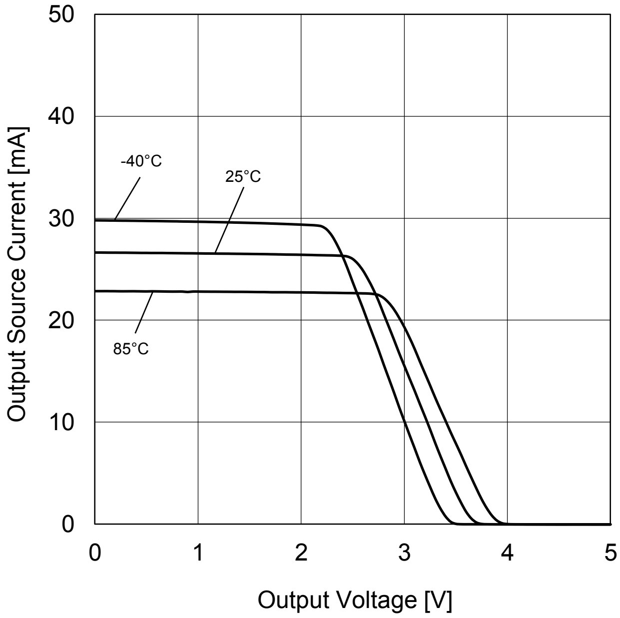


Figure 6. Output Source Current vs Output Voltage
(V_{CC}=5V)

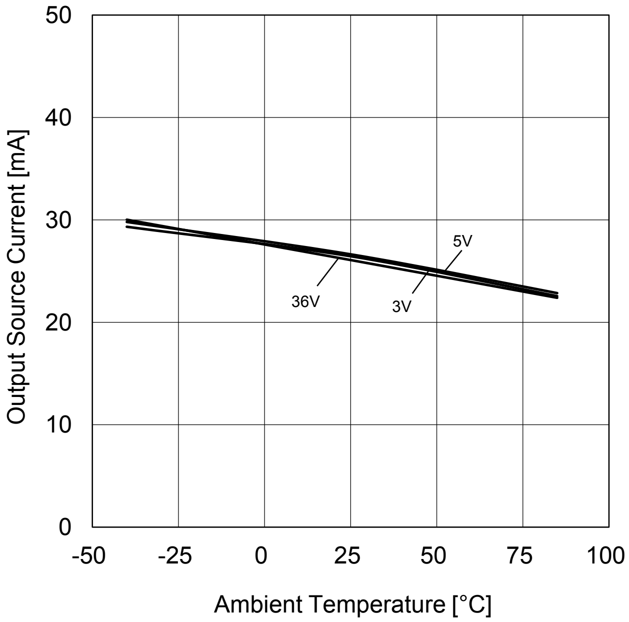


Figure 7. Output Source Current
vs Ambient Temperature (V_{OUT}=0V)

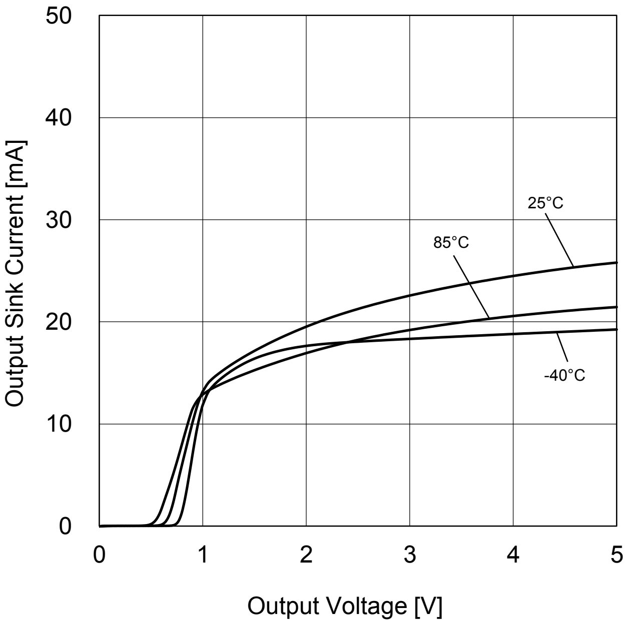


Figure 8. Output Sink Current vs Output Voltage
(V_{CC}=5V)

(*) The above data are measurement value of typical sample, they are not guaranteed.

Typical Performance Curves - continued

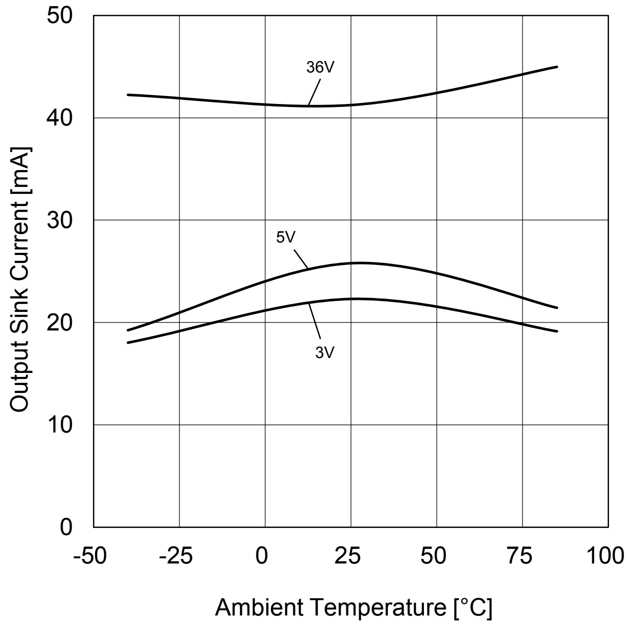


Figure 9. Output Sink Current vs Ambient Temperature (V_{OUT}=V_{CC})

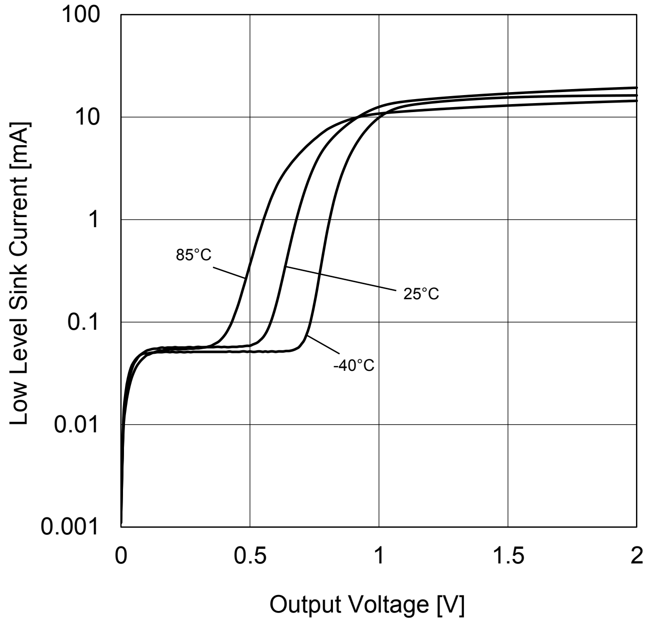


Figure 10. Low Level Sink Current vs Output Voltage (V_{CC}=5V)

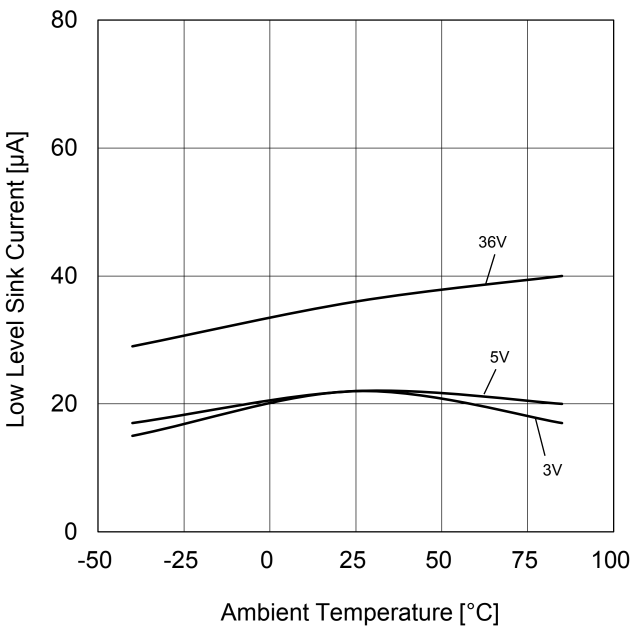


Figure 11. Low Level Sink Current vs Ambient Temperature (V_{OUT}=200mV)

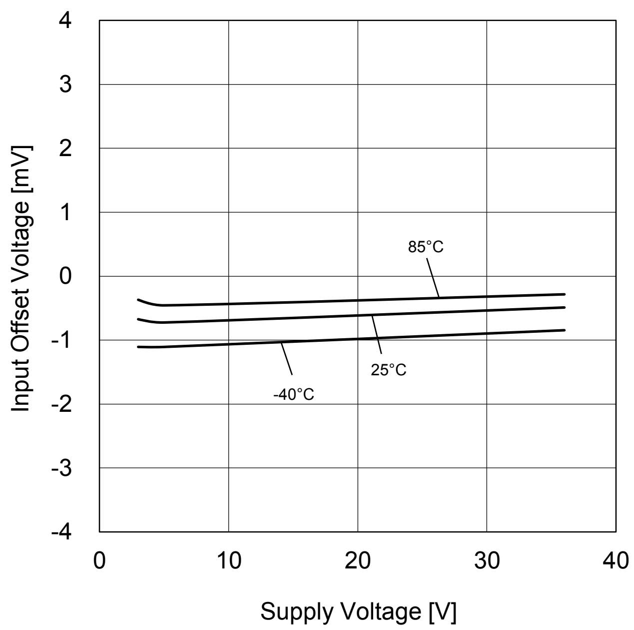


Figure 12. Input Offset Voltage vs Supply Voltage (V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

(*) The above data are measurement value of typical sample, they are not guaranteed.

Typical Performance Curves - continued

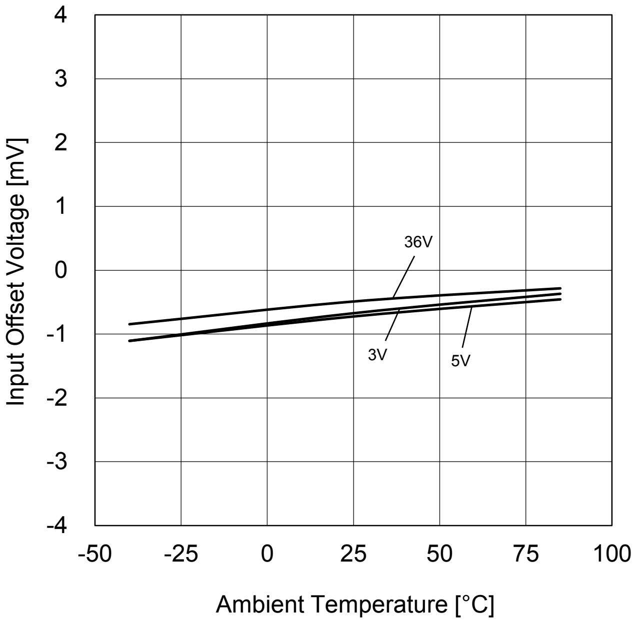


Figure 13. Input Offset Voltage vs Ambient Temperature
(V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

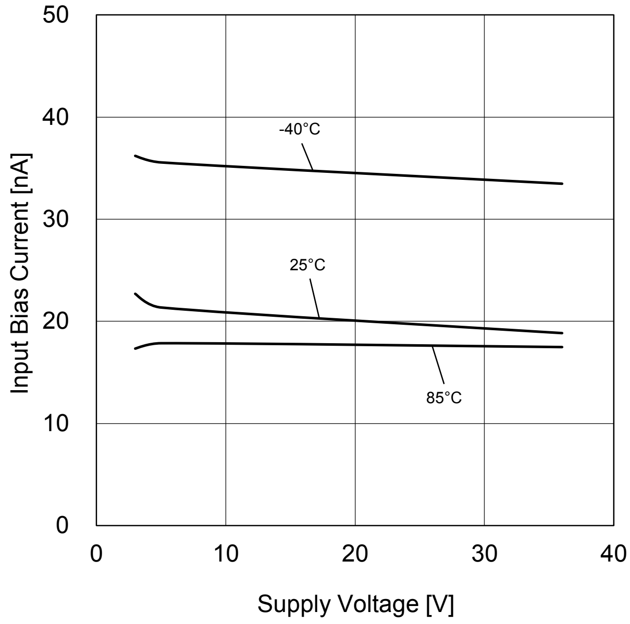


Figure 14. Input Bias Current vs Supply Voltage
(V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

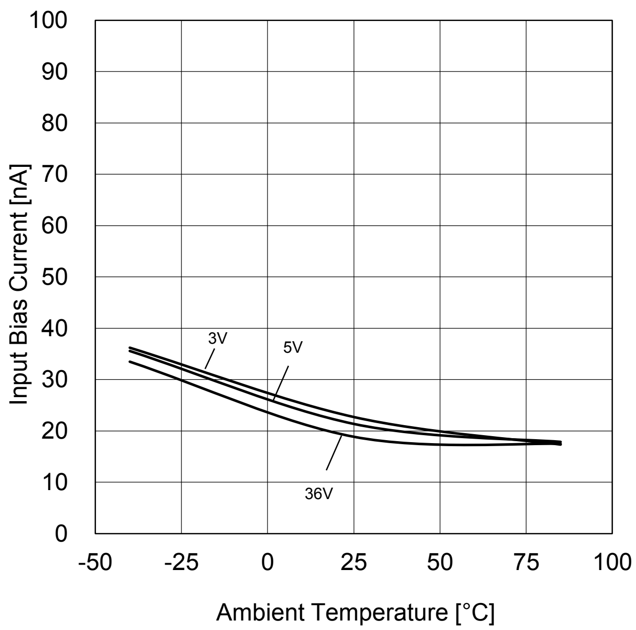


Figure 15. Input Bias Current vs Ambient Temperature
(V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

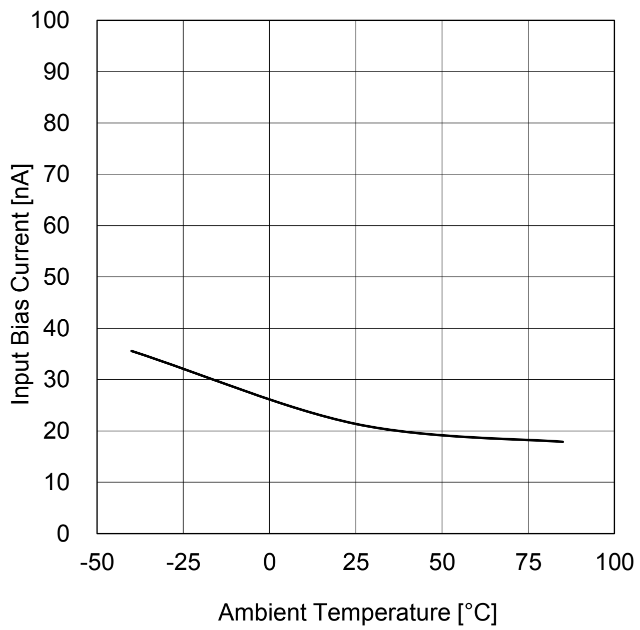


Figure 16. Input Bias Current vs Ambient Temperature
(V_{CC}=30V, V_{ICM}=28V, E_K=-1.4V)

(*) The above data are measurement value of typical sample, they are not guaranteed.

Typical Performance Curves - continued

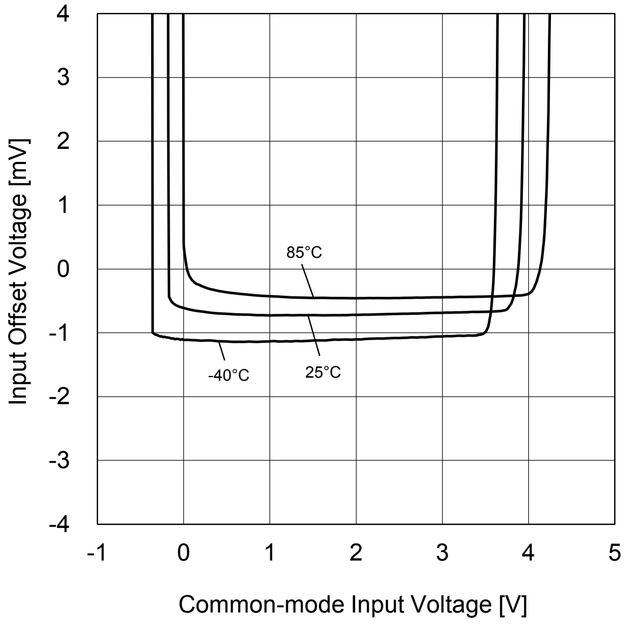


Figure 17. Input Offset Voltage vs Common-mode Input Voltage (V_{CC}=5V)

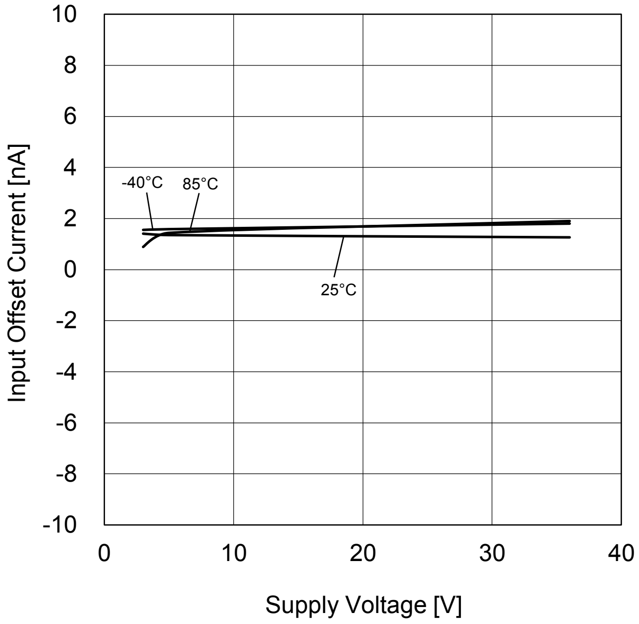


Figure 18. Input Offset Current vs Supply Voltage (V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

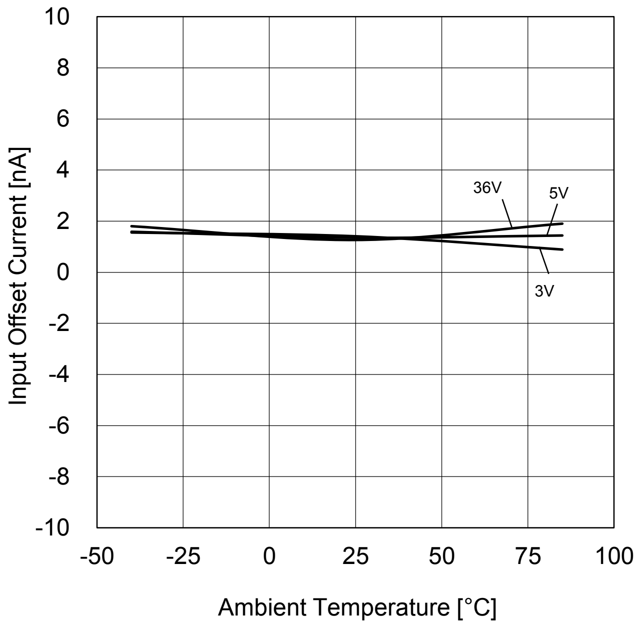


Figure 19. Input Offset Current vs Ambient Temperature (V_{ICM}=V_{CC}/2, E_K=-V_{CC}/2)

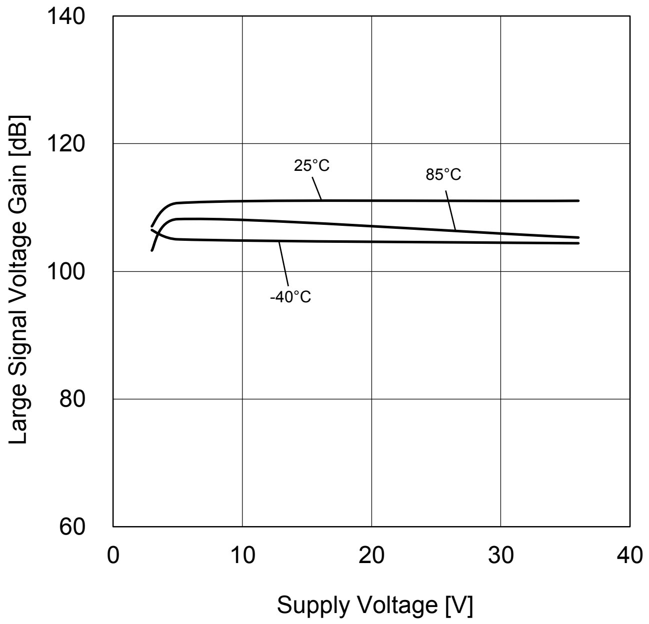


Figure 20. Large Signal Voltage Gain vs Supply Voltage (R_L=2kΩ)

(*) The above data are measurement value of typical sample, they are not guaranteed.

Typical Performance Curves - continued

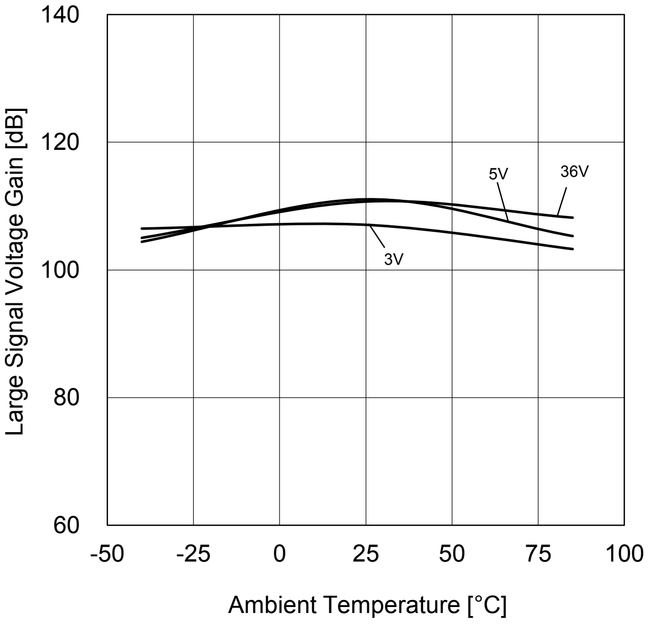


Figure 21. Large Signal Voltage Gain
vs Ambient Temperature (R_L=2kΩ)

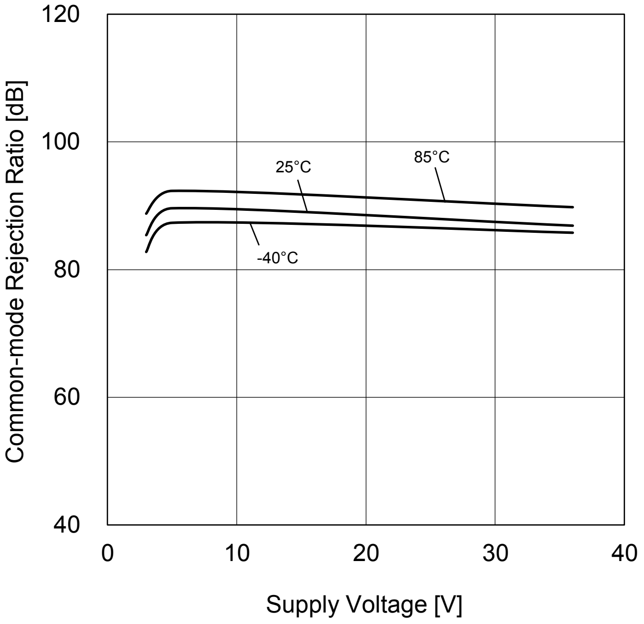


Figure 22. Common-mode Rejection Ratio
vs Supply Voltage

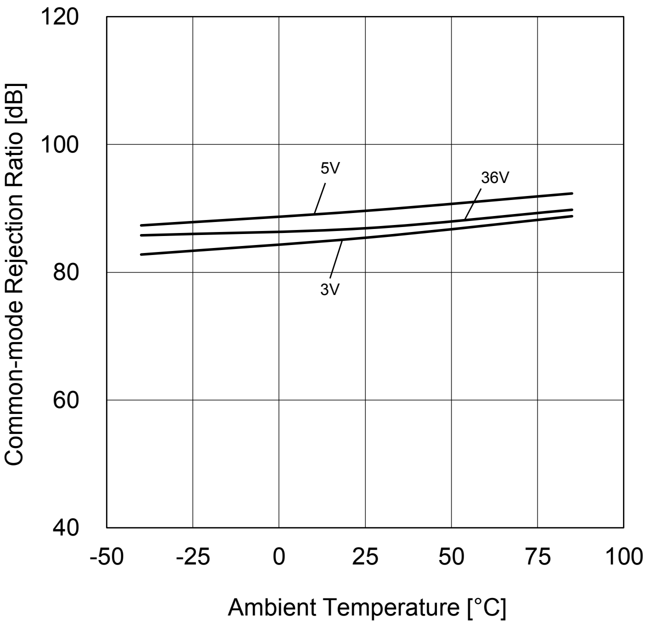


Figure 23. Common-mode Rejection Ratio
vs Ambient Temperature

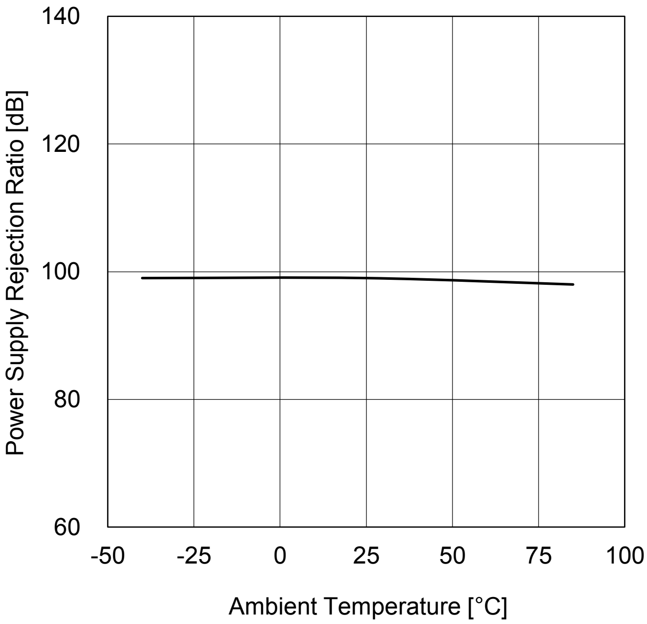


Figure 24. Power Supply Rejection Ratio
vs Ambient Temperature

(*) The above data are measurement value of typical sample, they are not guaranteed.

Application Information

NULL method condition for Test Circuit 1

VCC, VEE, E_K, V_{ICM} Unit: V

Parameter	V_F	SW1	SW2	SW3	VCC	VEE	E_K	V_{ICM}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	5 to 30	0	-1.4	0	1
Input Offset Current	V_{F2}	OFF	OFF	OFF	5	0	-1.4	0	2
Input Bias Current	V_{F3}	OFF	ON	OFF	5	0	-1.4	0	3
	V_{F4}	ON	OFF						
Large Signal Voltage Gain	V_{F5}	ON	ON	ON	15	0	-1.4	0	4
	V_{F6}						-11.4		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F7}	ON	ON	OFF	5	0	-1.4	0	5
	V_{F8}							3.5	
Power Supply Rejection Ratio	V_{F9}	ON	ON	OFF	5	0	-1.4	0	6
	V_{F10}				30				

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1 + R_F/R_S} \quad [V]$$

2. Input Offset Current (I_{IO})

$$I_{IO} = \frac{|V_{F2} - V_{F1}|}{R_I \times (1 + R_F/R_S)} \quad [A]$$

3. Input Bias Current (I_B)

$$I_B = \frac{|V_{F4} - V_{F3}|}{2 \times R_I \times (1 + R_F/R_S)} \quad [A]$$

4. Large Signal Voltage Gain (A_V)

$$Av = 20Log \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F6} - V_{F5}|} \quad [dB]$$

5. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20Log \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F8} - V_{F7}|} \quad [dB]$$

6. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20Log \frac{\Delta VCC \times (1+ R_F/R_S)}{|V_{F10} - V_{F9}|} \quad [dB]$$

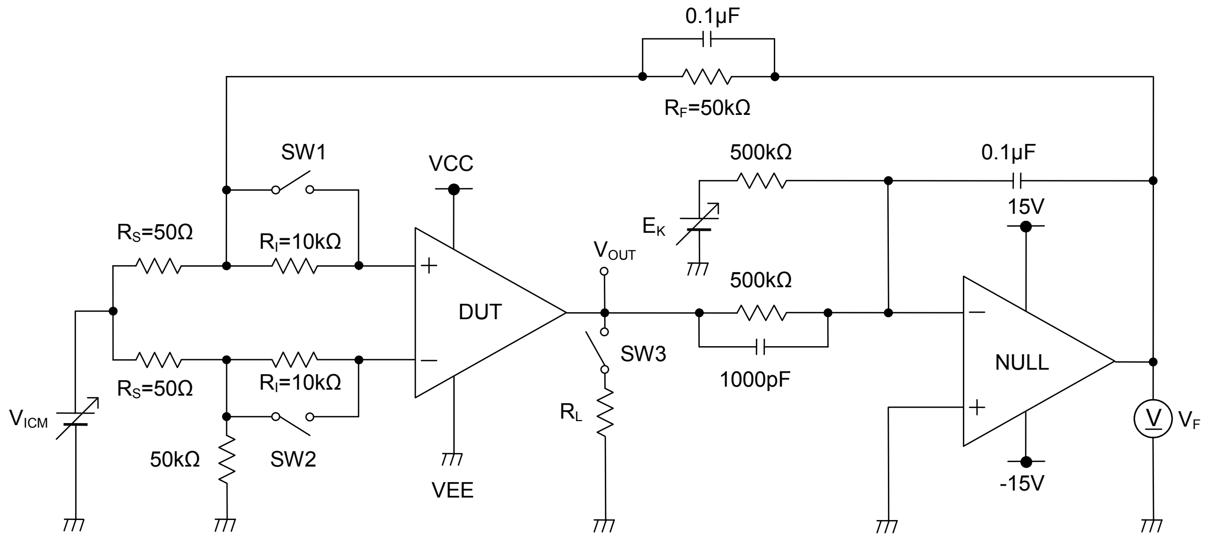


Figure 25. Test Circuit 1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage(High)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Maximum Output Voltage(Low)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
Input Referred Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF

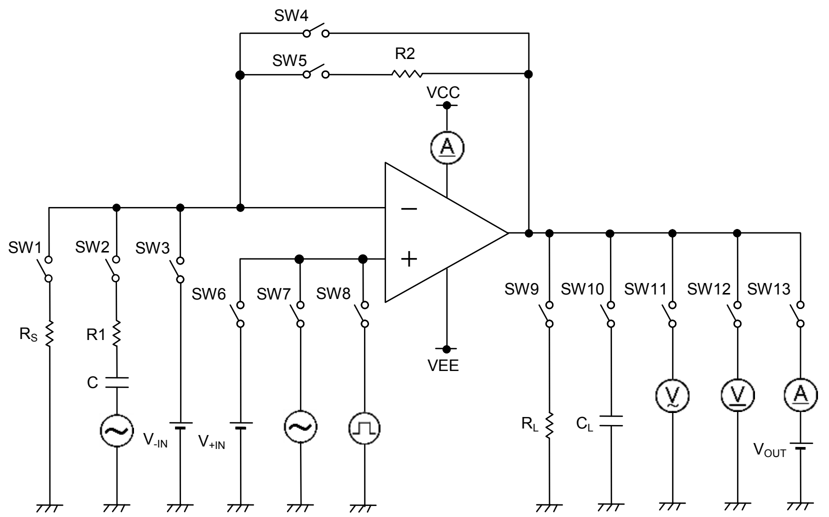


Figure 26. Test Circuit 2 (each Op-Amp)

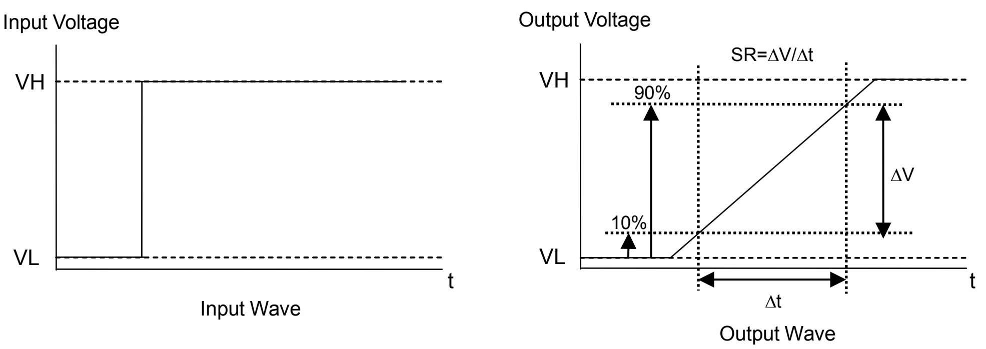


Figure 27. Slew Rate Input and Output Wave

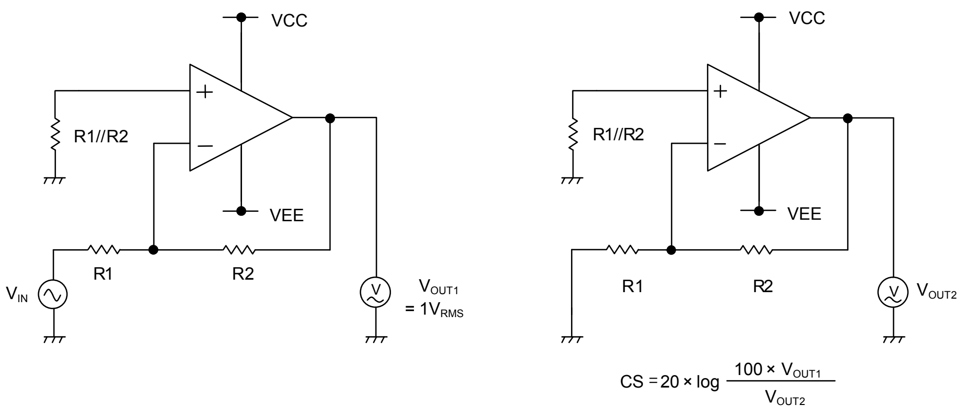


Figure 28. Test Circuit 3 (Channel Separation)
(R1=1kΩ,R2=100kΩ)

Examples of Circuit

○Voltage Follower

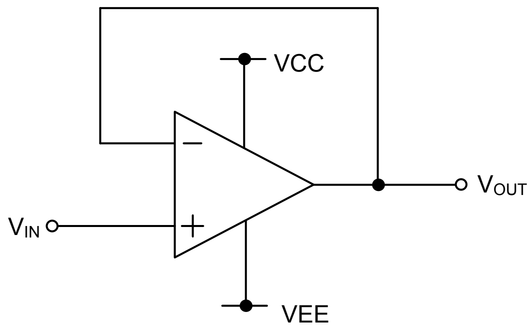


Figure 29. Voltage Follower Circuit

Voltage gain is 0dB.

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$V_{OUT}=V_{IN}$

○Inverting Amplifier

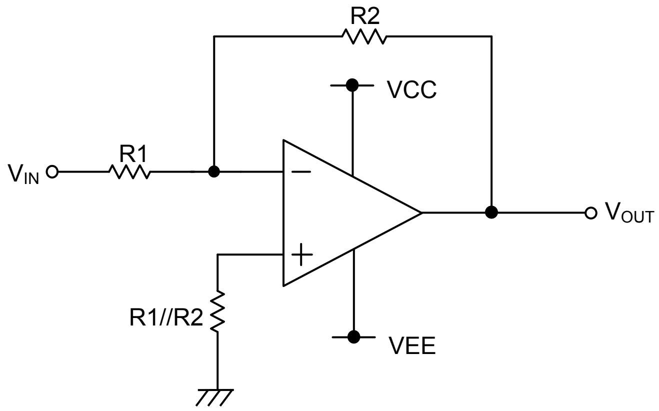


Figure 30. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

$V_{OUT}=-(R2/R1)\cdot V_{IN}$

This circuit has input impedance equal to R1.

○Non-inverting Amplifier

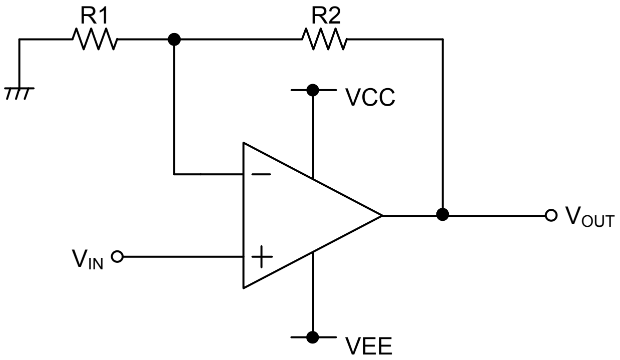


Figure 31. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$V_{OUT}=(1 + R2/R1)\cdot V_{IN}$

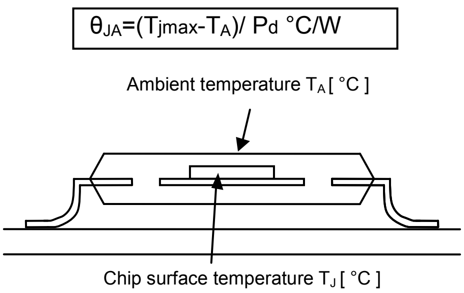
Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

Power Dissipation

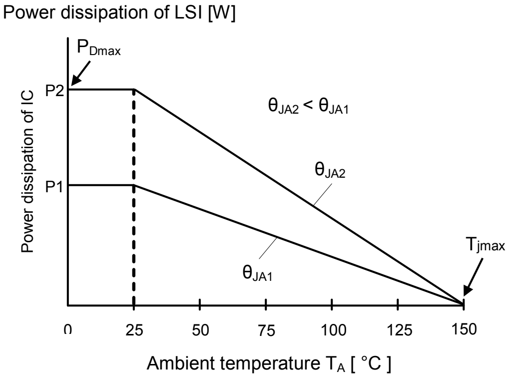
Power dissipation (total loss) indicates the power that the IC can consume at T_A=25°C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.
Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA}°C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.
Figure 32(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), maximum junction temperature (T_{jmax}), and power dissipation (P_d).

$$\theta_{JA} = (T_{jmax} - T_A) / P_d \quad °C/W$$

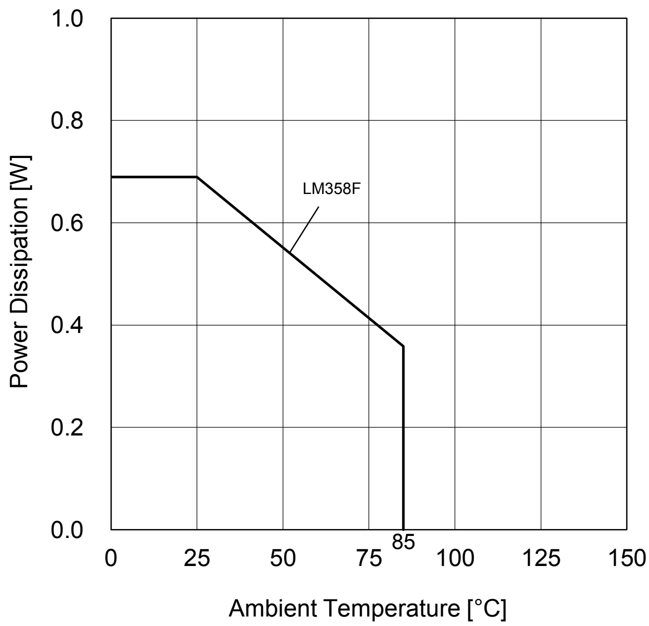
The Derating curve in Figure 32(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 32 (c) shows an example of the derating curve for LM358F.



(a) Thermal Resistance



(b) Derating Curve



(c) LM358F

5.5	mW/°C

When using the unit above T_A=25°C, subtract the value above per Celsius degree. Power dissipation is the value when FR4 glass epoxy board 70mm × 70mm × 1.6mm (copper foil area below 3%) is mounted

Figure 32. Thermal Resistance and Derating Curve

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_d stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_d rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

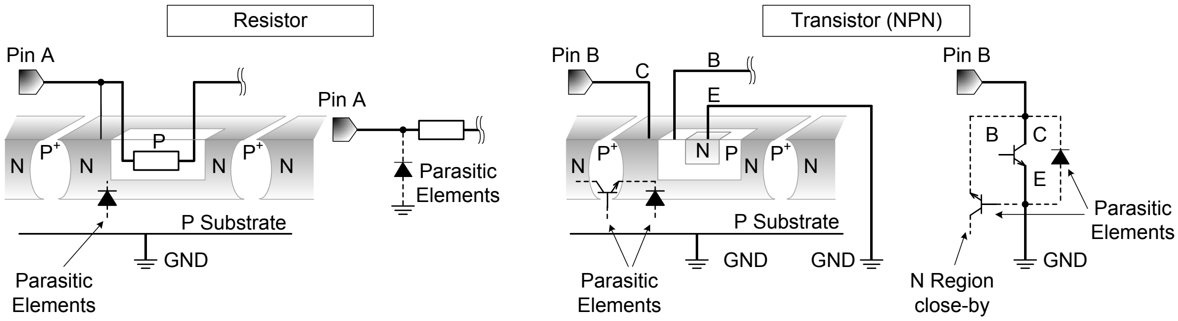


Figure 33. Example of monolithic IC structure

12. Unused circuits

It is recommended to apply the connection (see Figure 34.) and set the non-inverting input pin at a potential within the Input Common-mode Voltage Range (V_{ICM}) for any unused circuit.

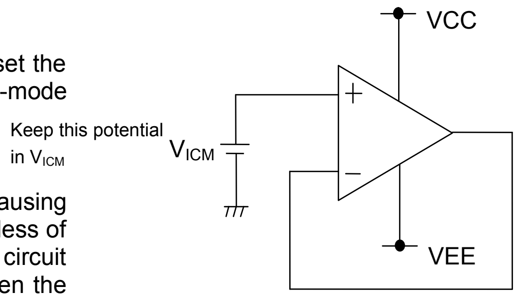


Figure 34. The Example of Application Circuit for Unused Op-amp

13. Input Voltage

Applying V_{EE}+36V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

14. Power supply (single/dual)

The operational amplifiers operate when the voltage supplied is between VCC pin and VEE pin. Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

15. IC Handling

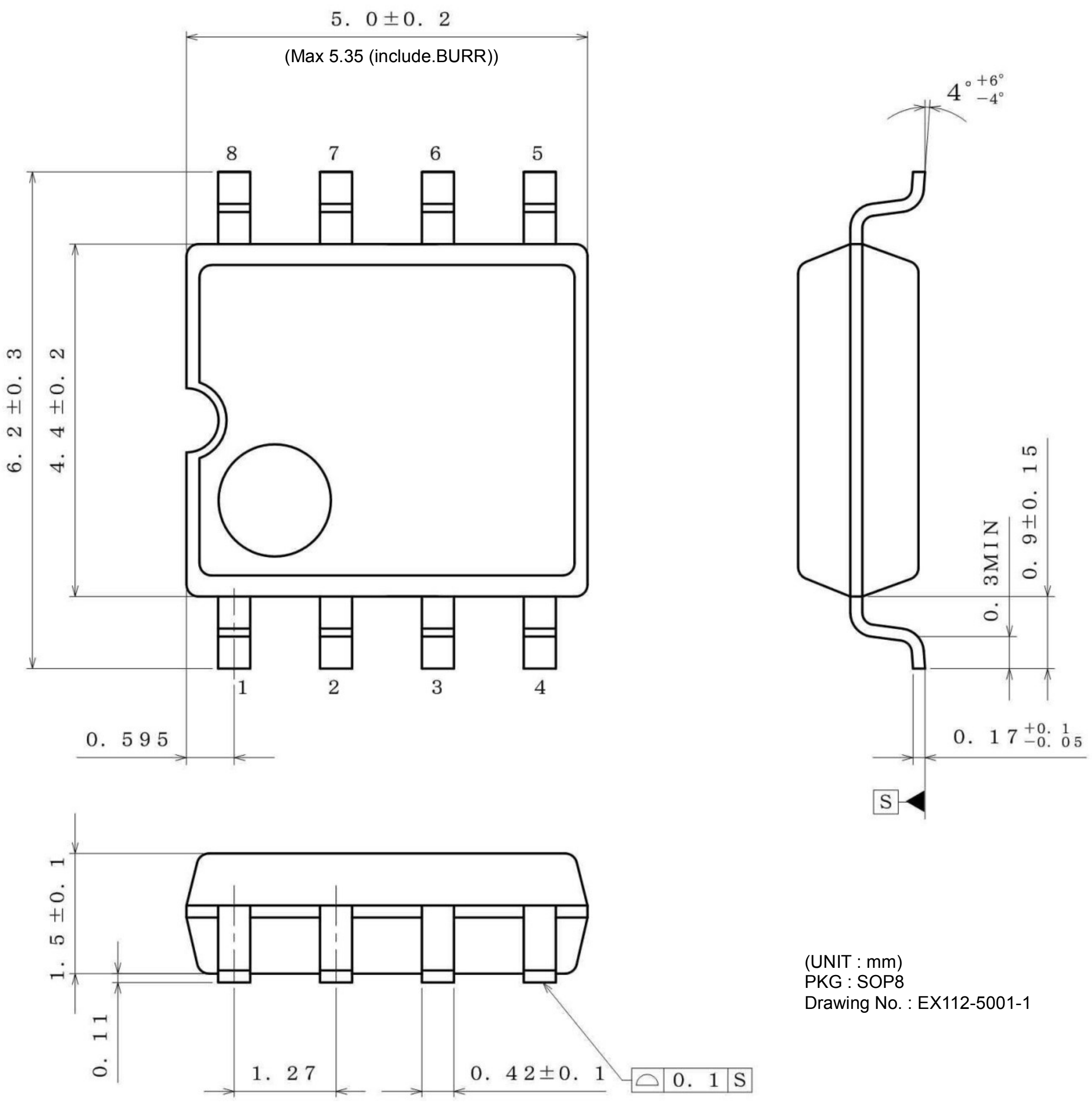
When pressure is applied to the IC through warp on the printed circuit board, the characteristics may fluctuate due to the piezo effect. Be careful with the warp on the printed circuit board.

16. The IC Destruction Caused by Capacitive Load.

The IC may be damaged when VCC pin and VEE pin is shorted with the charged output pin capacitor. When IC is used as an operational amplifier or as an application circuit where oscillation is not activated by an output capacitor, output capacitor must be kept below 0.1µF in order to prevent the damage mentioned above.

Physical Dimensions Tape and Reel Information

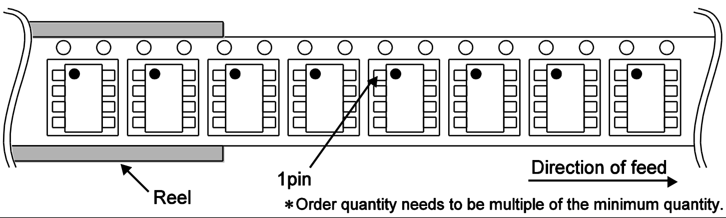
Package Name	SOP8



(UNIT : mm)
PKG : SOP8
Drawing No. : EX112-5001-1

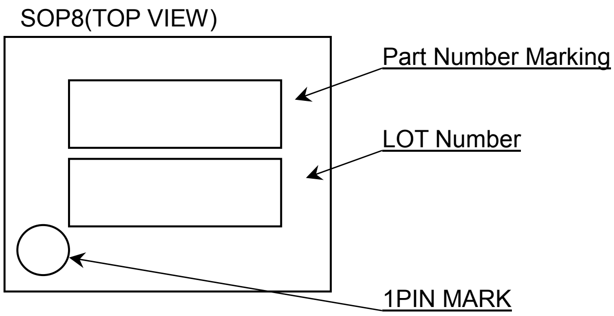
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagram



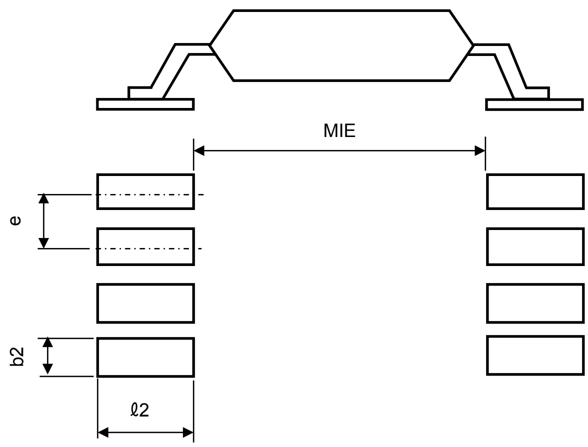
Product Name		Package Type	Marking
LM358	F	SOP8	358L

Land Pattern Data

All dimensions in mm

PKG	Land pitch e	Land space MIE	Land length ≧ℓ2	Land width b2
SOP8	1.27	4.60	1.10	0.76

SOP8



Revision History

Date	Revision	Changes
12.May.2015	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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