



LM3702/LM3703 Microprocessor Supervisory Circuits with Low Line Output and Manual Reset General Description • No external components required

The LM3702/LM3703 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3702/LM3703 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.

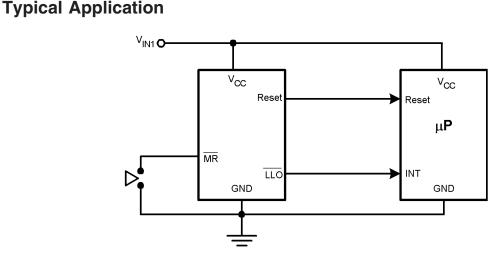
RESET (LM3702) or RESET (LM3703) outputs

Manual-Reset input

- Precision supply voltage monitor
- Factory programmable Reset Timeout Delay
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} (RESET option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring



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Connection Diagram

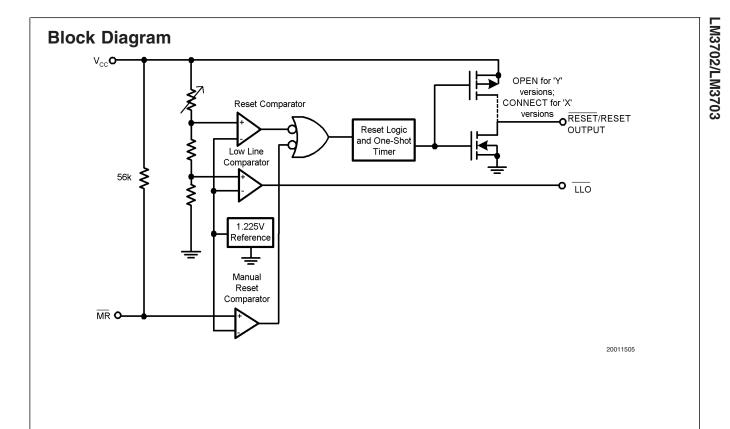
LM3702/LM3703

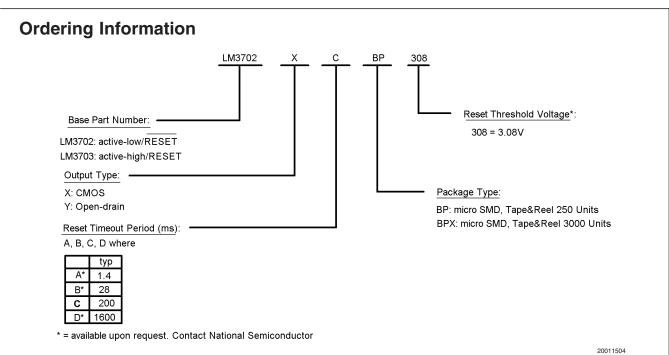
•		Top View rom the co /ID 9 Bum BPA09	oating s	
	с Reset	с v _{cc}	○ MR	1

	00	IVIIX	
С NC	C NC	С ОС	2
	C GND	C NC	3
С	В	А	
		20011	501

Pin Descriptions

Bump No.	Name	Function
A1	MR	Manual-Reset input. When MR is less than V _{MRT} (Manual Reset Threshold)
		RESET/RESET is engaged.
B1	V _{CC}	Power Supply input.
C1	RESET	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays
		low whenever V_{CC} is below the reset threshold or when \overline{MR} is below V_{MRT} . It remains low
		for t_{RP} after either V_{CC} rises above the reset threshold, or after \overline{MR} input rises above
		V _{MRT} (LM3702 only).
	RESET	Reset Logic Output. RESET is the inverse of RESET (LM3703 only).
C3	LLO	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT}
		(Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable
		Interrupt) to provide an early warning of imminent power-failure.
B3	GND	Ground reference for all signals.
A2, A3, C2	NC	No Connect.
B2	NC	No Connect. Test input used at factory only. Leave floating.





*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3702/LM3703

Part Number	Output	Reset Timeout Period	Package Marking
LM3702XCBP-308	totem-pole	200ms	%%l2
LM3702XCBPX-308	totem-pole	200ms	%%l2
LM3703XCBP-308	totem-pole	200ms	%%l3
LM3703XCBPX-308	totem-pole	200ms	%%l3
LM3703XDBP-308	totem-pole	1600ms	%%124
LM3703XDBPX-308	totem-pole	1600ms	%%124
LM3702YABP-308	open-drain	1.4ms	%%131
LM3702ABPX-308	open-drain	1.4ms	%%131
LM3702YDBP-220	open-drain	1600ms	%%125
LM3702YDBPX-220	open-drain	1600ms	%%125
% % is the detected and will your with time			

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Low Line Output
LM3702	х		X, Y*	Customized	х	x
LM3703		х	Х	Customized	х	х

* = available upon request. Contact National

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation	
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(Note 3)

LM3702/LM3703

Operating Ratings (Note 1)

Temperature Range

 $-40^{\circ}C \leq T_{J} \leq 85^{\circ}C$

Supply Voltage (V_{CC})	-0.3V to 6.0V
All Other Inputs	–0.3V to V _{CC} + 0.3V
ESD Ratings (Note 2)	
Human Body Model	1.5kV
Machine Model	150V

LM3702/LM3703 Series Electrical Characteristics

Limits in the standard typeface are for $T_J = 25^{\circ}C$ and limits in **boldface type** apply over full operating range. Unless otherwise specified: $V_{CC} = +2.2V$ to 5.5V.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
POWER S	UPPLY					
V _{CC}	Operating Voltage	LM3702	1.0		5.5	v
	Range: V _{CC}	LM3703	1.2		5.5	7 V
I _{CC}	V _{CC} Supply Current	All inputs = V_{CC} ; all outputs floating		28	50	μA
RESET TH	RESHOLD		1	1 1		-
V _{RST}	Reset Threshold	V _{CC} falling	-0.5		+0.5	
			-2	V _{RST}	+2	%
		V_{CC} falling: $T_A = 0^{\circ}C$ to $70^{\circ}C$	-1.5] [+1.5	7
V _{RSTH}	Reset Threshold Hysteresis			0.0032•V _{RST}		mV
t _{RP}	Reset Timeout	Reset Timeout Period = A	1	1.4	2	
	Period	Reset Timeout Period = B	20	28	40	
		Reset Timeout Period = C	140	200	280	ms
		Reset Timeout Period = D	1120	1600	2240	
t _{RD}	V _{CC} to Reset Delay	V _{CC} falling at 1mV/µs		20		μs
RESET (LI	W3703)					
V _{OL}	RESET	V _{CC} > 2.25V, I _{SINK} = 900µA			0.3	
		$V_{\rm CC} > 2.7V, I_{\rm SINK} = 1.2mA$			0.3	V
		$V_{\rm CC} > 4.5V, I_{\rm SINK} = 3.2mA$			0.4	1
V _{OH}	RESET	$V_{CC} > 1.2V, I_{SOURCE} = 50\mu A$	0.8 V _{cc}			
		$V_{CC} > 1.8V$, $I_{SOURCE} = 150\mu A$	0.8 V _{cc}			1
		$V_{CC} > 2.25V, I_{SOURCE} = 300\mu A$	0.8 V _{cc}			V
		$V_{CC} > 2.7V$, $I_{SOURCE} = 500\mu A$	0.8 V _{cc}			1
		$V_{CC} > 4.5V, I_{SOURCE} = 800\mu A$	V _{cc} – 1.5V			1
I _{LKG}	Output Leakage	$V_{\text{BESET}} = 5.5 V$			1.0	μA
	Current					
RESET (LI	M3702)					
V _{OL}	RESET	$V_{\rm CC} > 1.0V, I_{\rm SINK} = 50\mu A$			0.3	
		$V_{CC} > 1.2V, I_{SINK} = 100\mu A$			0.3	1
		V _{CC} > 2.25V, I _{SINK} = 900µA			0.3	1
		$V_{\rm CC} > 2.7V, I_{\rm SINK} = 1.2mA$			0.3	
		$V_{\rm CC} > 4.5V, I_{\rm SINK} = 3.2mA$			0.4	- V
V _{OH}	RESET	$V_{\rm CC} > 2.25V, I_{\rm SOURCE} = 300\mu A$	0.8 V _{cc}			1
5		$V_{CC} > 2.7V, I_{SOURCE} = 500\mu A$	0.8 V _{cc}			1
		$V_{CC} > 4.5V, I_{SOURCE} = 800\mu A$	V _{cc} - 1.5V			1

LM3702/LM3703 Series Electrical Characteristics (Continued)

Limits in the standard typeface are for $T_J = 25^{\circ}C$ and limits in **boldface type** apply over full operating range. Unless otherwise specified: $V_{CC} = +2.2V$ to 5.5V.

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
MR				•	•		
V _{MRT}	MR Input	MR, Low			0.8		
	Threshold	MR, High	2.0			V	
V _{MRTH}	MR Threshold	$\overline{\text{MR}}$ falling: V _{CC} = V _{RST MAX} to 5.5V		0.0032•V _{RST}		mV	
	Hysteresis						
R _{MR}	MR Pull-up		35	56	75	kΩ	
	Resistance						
t _{MD}	MR to Reset			12		μS	
	Delay						
t _{MR}	MR Pulse Width		25			μS	
LLO	1		1	•	•		
V _{OL}	LLO Output	$V_{\rm CC} > 2.25 V, I_{\rm SINK} = 900 \mu A$			0.3		
	Voltage	V _{CC} > 2.7V, I _{SINK} = 1.2mA			0.3		
		$V_{\rm CC} > 4.5V, I_{\rm SINK} = 3.2mA$			0.4	v	
V _{OH}		$V_{CC} > 2.25V, I_{SOURCE} = 300\mu A$	0.8 V _{cc}				
		$V_{CC} > 2.7V$, $I_{SOURCE} = 500\mu A$	0.8 V _{cc}				
		$V_{CC} > 4.5V$, $I_{SOURCE} = 800\mu A$	V _{cc} – 1.5V				
	TUT						
V _{LLOT}	LLO Output		1.01•V _{RST}	1.02•V _{RST}	1.03•V _{RST}	V	
	Threshold						
	$(V_{LLO} - V_{RST}, V_{CC})$						
	falling)						
V_{LLOTH}	Low-Line			0.0032•V _{RST}		mV	
	Comparator						
	Hysteresis						
t _{CD}	Low-Line	V _{CC} falling at 1mV/µs		20		μs	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

Note 2: The Human Body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A} , and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_{J}(MAX) - T_{A}}{\theta_{J-A}}$$

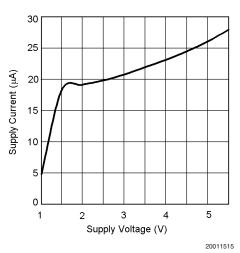
Where the value of $\theta_{J\text{-}A}$ for the micro SMD package is 220°C/W.

Comparator Delay

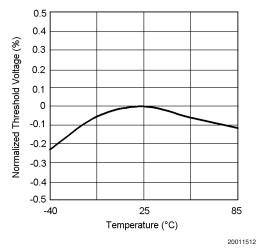


Typical Performance Characteristics

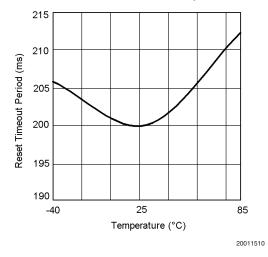
Supply Current vs Supply Voltage

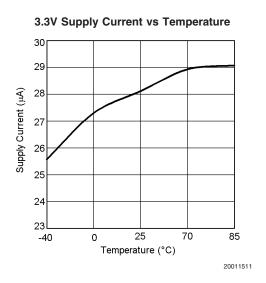


Normalized Reset Threshold Voltage vs Temperature

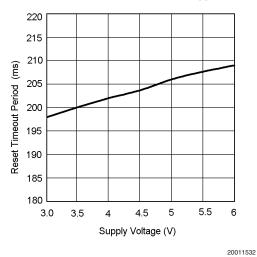


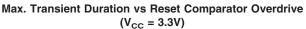
Reset Timeout Period vs Temperature

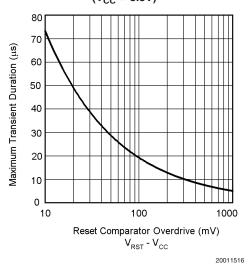






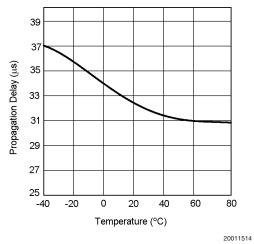






Typical Performance Characteristics (Continued)

Low-Line Comparator Propagation Delay vs Temperature



Circuit Information

RESET OUTPUT

The Reset input of a μP initializes the device into a known state. The LM3702/LM3703 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

RESET is guaranteed valid for $V_{CC} > 1V$. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3702 offers an active-low RESET; The LM3703 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input $(\overline{\text{MR}})$ will initiate a forced reset also. See the *Manual Reset Input* section.

RESET THRESHOLD

The LM3702/LM3703 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact National Semiconductor for details.

MANUAL RESET INPUT (MR)

Many μ P-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 k Ω pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 μ s, reset is asserted after a typical delay of 12 μ s. Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset

timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT}. Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

LOW-LINE OUTPUT (LLO)

The low-line output comparator is typically used to provide a non-maskable interrupt to a μ P when V_{CC} begins falling. LLO monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

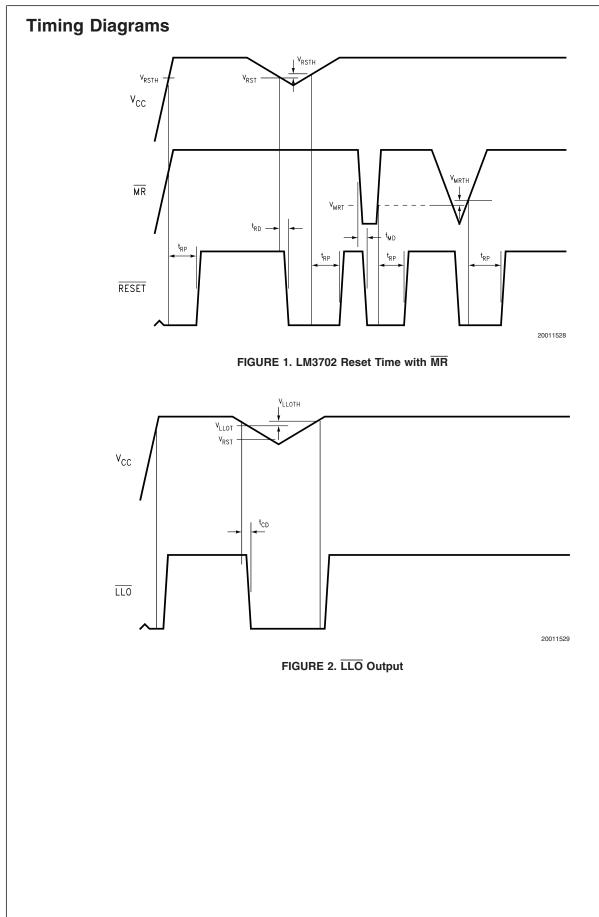
SPECIAL PRECAUTIONS FOR THE MICRO SMD PACKAGE

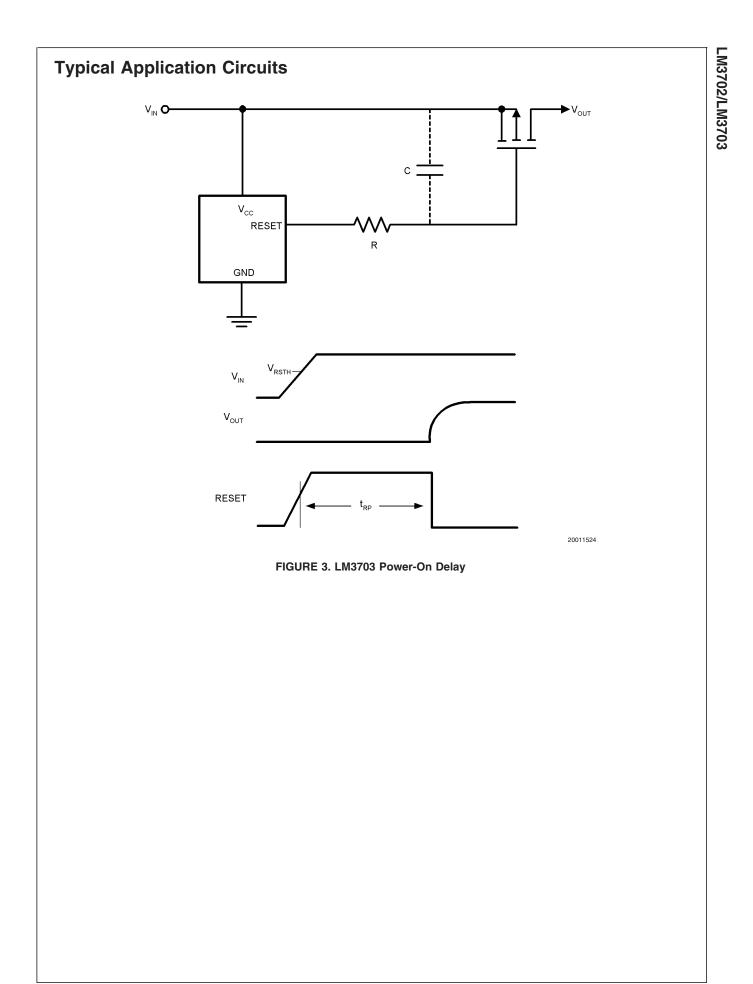
As with most integrated circuits, the LM3702 and LM3703 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the micro SMD package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

MICRO SMD MOUNTING

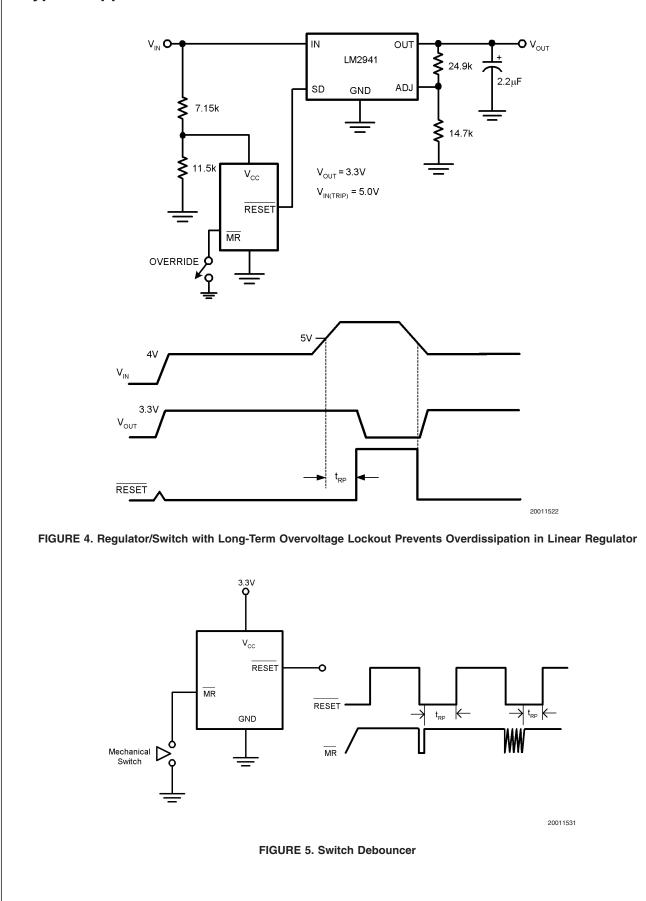
The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note AN-1112. Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

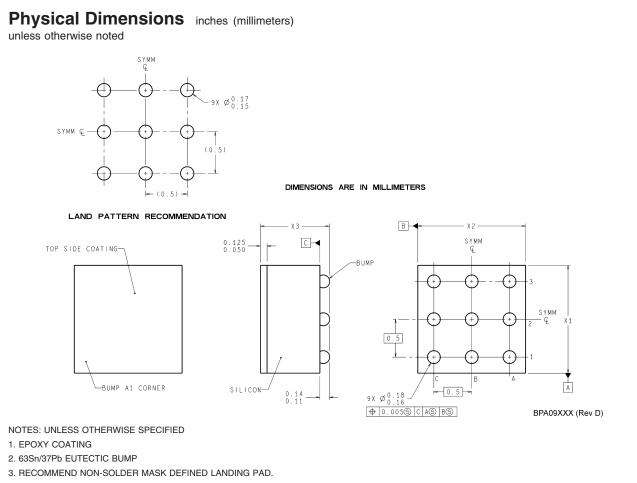
For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.





Typical Application Circuits (Continued)





4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.

5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

6.NO JEDEC REGISTRATION AS OF AUG.1999.

9 bump micro SMD Package NS Package Number BPA09FFB The dimensions of X1, X2 and X3 are given below X1 = 1.412mm X2 = 1.412mm X3 = 0.850mm

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