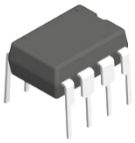
CURRENT MODE PWM CONTROLLER LM3842A/3A/4A/5A

FEATURES

- Automatic feed forward compensation
- Optimized for offline converter
- Double pulse suppression
- Current mode operation to 500kHz
- High gain totem pole output
- Internally trimmed bandgap reference
- Undervoltage lockout with hysteresis
- Low start up current: < 0.3mA
- Moisture Sensitivity Level 3

SOP-8 PKG

DIP-8 PKG



ORDERING INFORMATION

Device	Package
LM3842A/3A/4A/5AD	SOP-8
LM3842A/3A/4A/5AN	DIP-8

DESCRIPTION

The LM384xA are fixed frequency current-mode PWM controller. They are specially designed for Off-Line and DC-to-DC converter applications with minimal external components.

These integrated circuits features a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET.

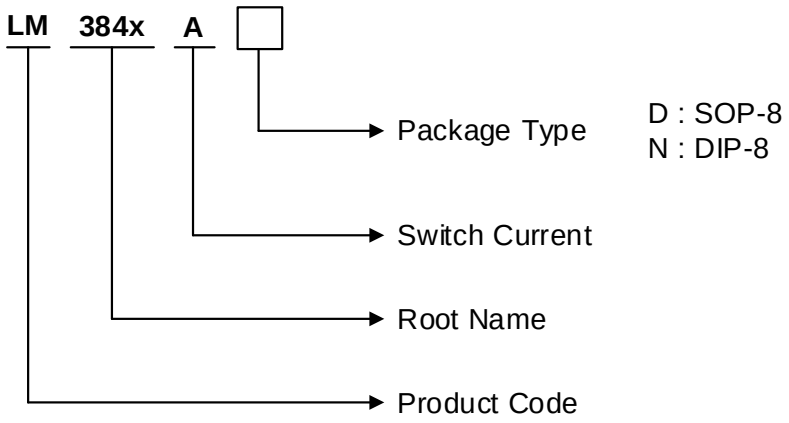
Protection circuitry includes built in under-voltage lockout and current limiting.

ABSOLUTE MAXIMUM RATINGS

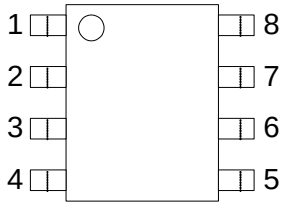
CHARACTERISTIC	SYMBOL	Value	UNIT
Supply Voltage	V_{CC}	30	V
Output Current	I_O	±1	A
Input Voltage	V_I	-0.3 to 5.5	V
ERR AMP Output Sink Current	I_{SINK}	10	mA
Lead temperature	T_{SOL}	260	°C
Storage temperature range	T_{STG}	-65 to 150	°C
Operating temperature range	T_J	-40 to 125	°C

ORDERING INFORMATION

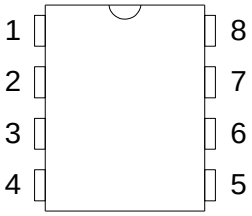
Package	Order No.	Package Marking	Supplied As	Status
SOP-8	LM3842AD	3842A	Reel	Active
DIP-8	LM3842AN	3842A	Tube	Active
SOP-8	LM3843AD	3843A	Reel	Active
DIP-8	LM3843AN	3843A	Tube	Active
SOP-8	LM3844AD	3844A	Reel	Contact Us
DIP-8	LM3844AN	3844A	Tube	Contact Us
SOP-8	LM3845AD	3845A	Reel	Contact Us
DIP-8	LM3845AN	3845A	Tube	Contact Us



PIN CONFIGURATION



SOP-8

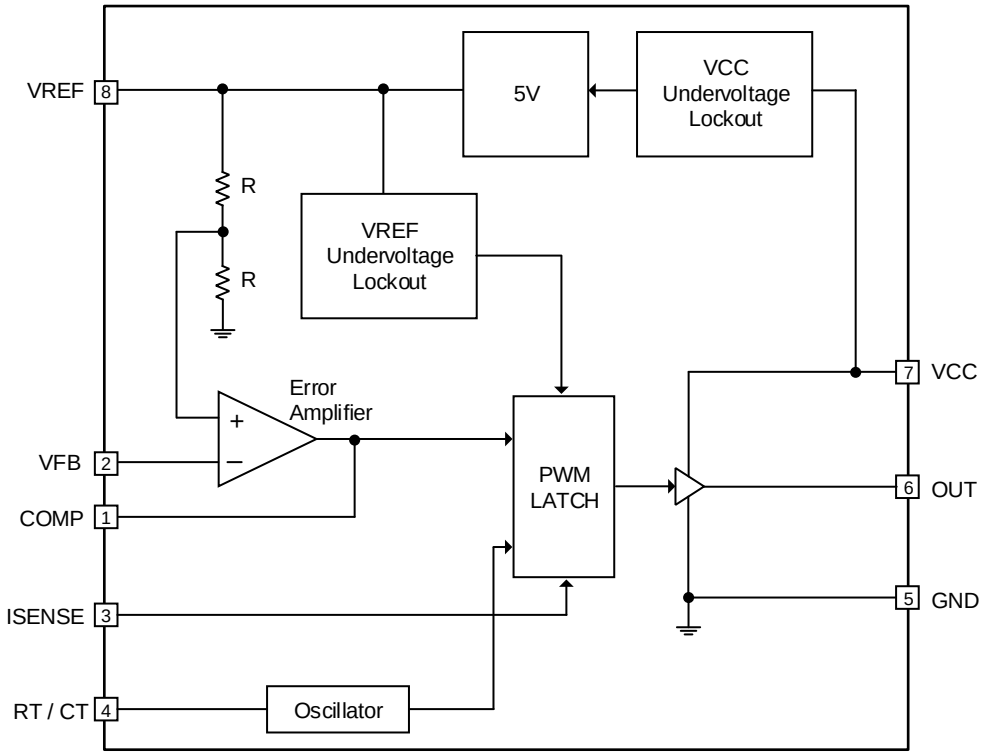


DIP-8

PIN DESCRIPTION

Pin No.	SOP-8 / DIP-8 PKG	
	Pin Name	Description
1	COMP (Compensation)	This pin is the Error Amplifier output and is made available for loop compensation.
2	VFB (Feedback Voltage)	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	ISENSE (Current Sense)	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to VREF and capacitor CT to ground.
5	GND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	VCC	This pin is the positive supply of the control IC.
8	VREF	This is the reference output. It provides charging current for capacitor CT through resistor RT.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V(NOTE 1), R_T = 10KΩ, C_T = 3.3nF, T_A = 0°C to 70°C ; unless otherwise specified)

Characteristics	Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	T_J=25°C, I_{OUT}=1mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	12V ≤ V_{CC} ≤ 25V		2.0	20	mV
Load Regulation	ΔV_{REF}	1mA ≤ I_{OUT} ≤ 20mA		3.0	25	
Short-Circuit Output Current	I_{SC}	T_A=25°C		-85	-180	mA
OSCILLATOR SECTION						
Oscillation Frequency	F_{OSC}	T_J = 25°C	47	52	57	KHz
Frequency Change with Voltage	Sv	12V ≤ V_{CC} ≤ 25V		0.2	1.0	%
Oscillator Amplitude	V_{OSC}			1.6		V_{p-p}
ERROR AMPLIFIER SECTION						
Input Bias Current	I_{BIAS}			-0.1	-2	µA
Feedback Input Voltage	V_{FB}	V_{PIN1}=2.5V	2.42	2.50	2.58	V
Open-Loop Voltage Gain	A_{VOL}	2V ≤ V_{OUT} ≤ 4V	65	90		dB
Power Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V	60	70		dB
Output Sink Current	I_{SINK}	V_{PIN2}=2.7V, V_{PIN1}=1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_{PIN2}=2.3V, V_{PIN1}=5.0V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{PIN2}=2.3V, R_L=15KΩ to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{PIN2}=2.7V, R_L=15KΩ to V_{REF}		0.8	1.1	
CURRENT SENSE SECTION						
Gain	G_V	(Note 2 & 3)	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{PIN1}=5V (Note 2)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V_{CC} ≤ 25V (Note 2)		70		dB
Input Bias Current	I_{BIAS}			-3.0	-10	µA
OUTPUT SECTION						
Low Output Voltage	V_{OL}	I_{SINK}=20mA		0.1	0.4	V
		I_{SINK}=200mA		1.5	2.2	
High Output Voltage	V_{OH}	I_{SINK}=20mA	13.0	13.5		
		I_{SINK}=200mA	12.0	13.0		
Rise Time	t_R	T_J=25°C, C_L=1nF		45	150	ns
Fall Time	t_F	T_J=25°C, C_L=1nF		35	150	ns

UNDERVOLTAGE LOCKOUT SECTION						
Start Threshold	V_{TH}	3842A/3844A	14.5	16.0	17.5	V
		3843A/3845A	7.8	8.4	9.0	
Minimum Operating Voltage (after turn-on)	$V_{CC(Min)}$	3842A/3844A	8.5	10	11.5	V
		3843A/3845A	7.0	7.6	8.2	
PWM SECTION						
Maximum Duty Cycle	$D_{(MAX)}$	3842A/3843A	94	96	100	%
		3844A/3845A	47	48	50	
TOTAL STANDBY CURRENT						
Start-up Current	I_{ST}	V_{CC}=14V for 3842A/3844A		0.17	0.3	mA
		V_{CC}=6.5V for 3843A/3845A		0.17	0.3	
Operating Supply Current	I_{CC}	V_{PIN3}=V_{PIN2}=0V		13	17	
Zener Voltage	V_Z	I_{CC}=25mA	30	38		V

Note 1 : Adjust V_{CC} above the start threshold before setting at 15V.

Note 2 : The parameter measured at a trip point of latch with V_{PIN2}=0

Note 3 : The gain is defined as A= $\Delta V_{PIN1}/\Delta V_{PIN3}$; $0 \le \Delta V_{PIN3} \le 0.8V$.

APPLICATION INFORMATION

Open Loop Test Circuit

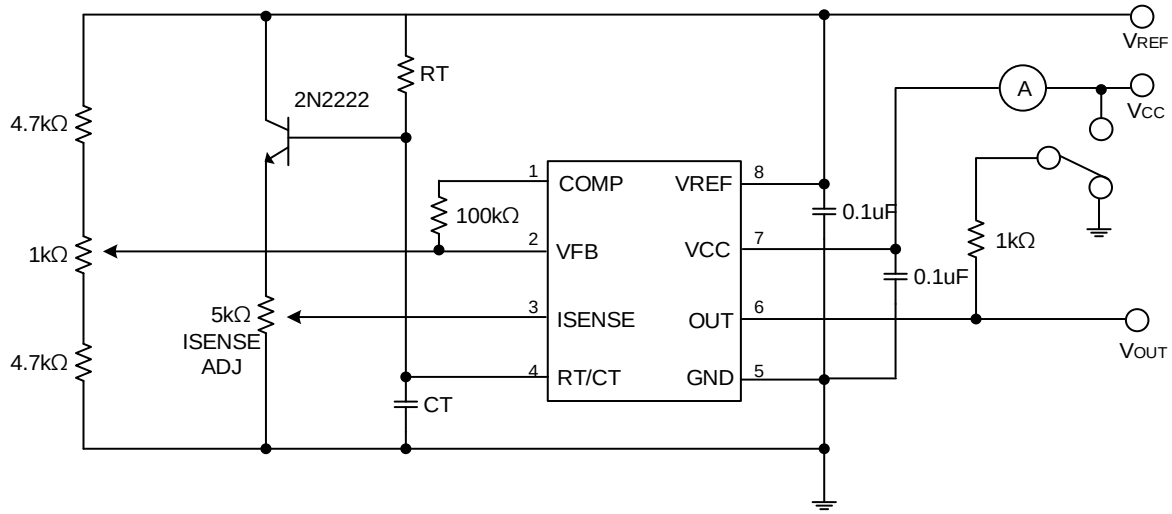
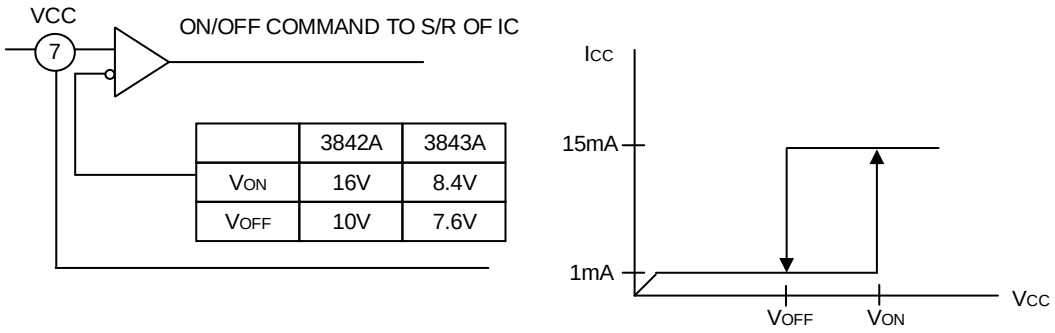


Fig 1. Application with open Loop Test Circuit

Under Voltage Lockout



	3842A	3843A
VON	16V	8.4V
VOFF	10V	7.6V

Fig 2. Application with Under Voltage Lockout

During under-voltage lock-out, the output driver is biased to a high impedance state.

Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

Under Voltage Lockout

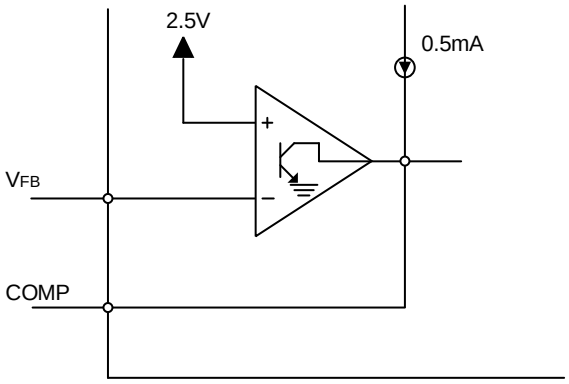


Fig 3. Application with Error Amp Configuration

Current Sense Circuit

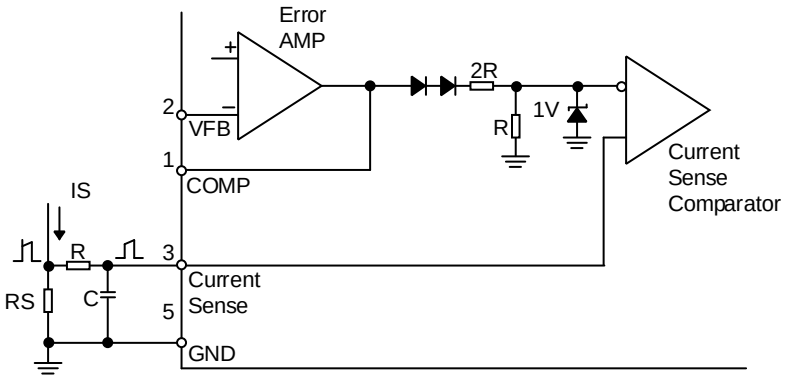


Fig 4. Application with Current Sense Circuit

Peak current (Is) is determined by the formula :

$$I_{S(MAX)} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Oscillator Waveforms and Maximum Duty Cycle

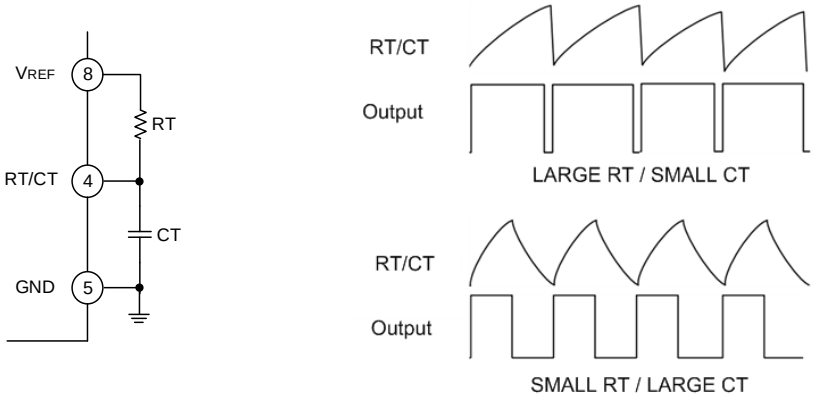


Fig 5. Application with Oscillator Waveforms and Maximum Duty Cycle

Duty cycle. Charge and discharge times are determined by the formula :

$t_c \sim 0.55\ R_T C_T$

$t_d \sim R_T C_T \int \left(\frac{0.0063R_T - 2.7}{0.0063R_T - 4}\right)$

Frequency, then, is:

$f = (t_c + t_d) - 1$

For RT>5kΩ:

$f \approx \frac{1.8}{R_T C_T}$

Shutdown Techniques

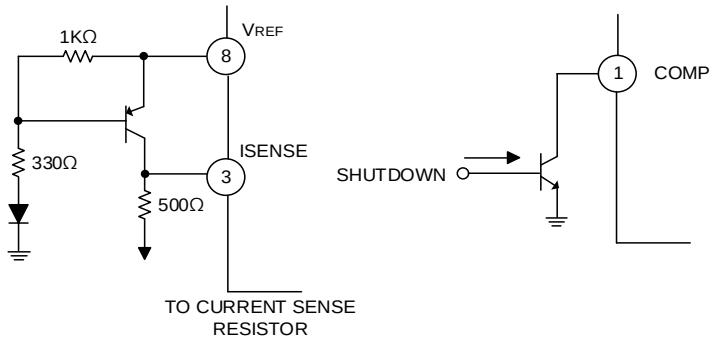


Fig 6. Application with Shutdown Techniques

Shutdown of the LM3842A can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling VCC below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Slope Compensation

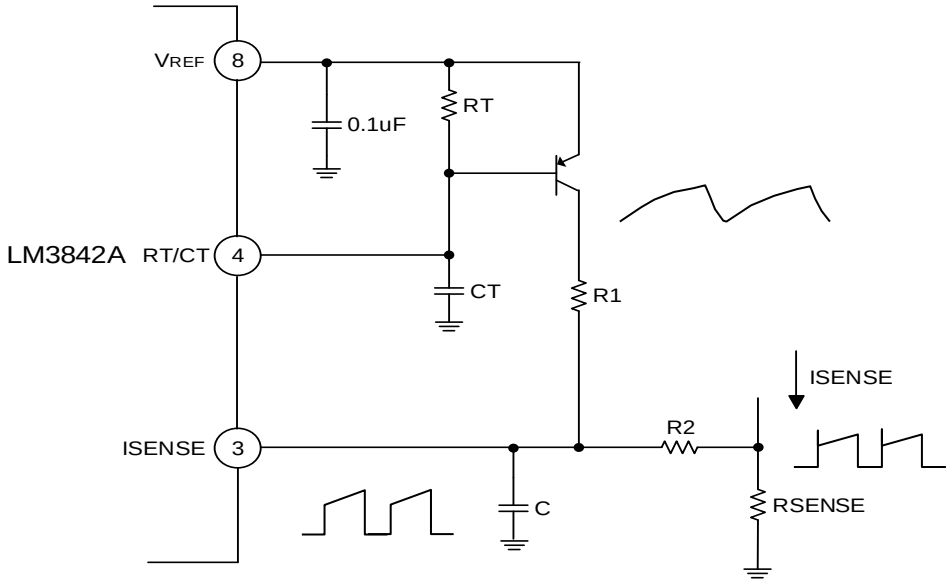


Fig 7. Application with Slope Compensation

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

TYPICAL OPERATING CHARACTERISTICS

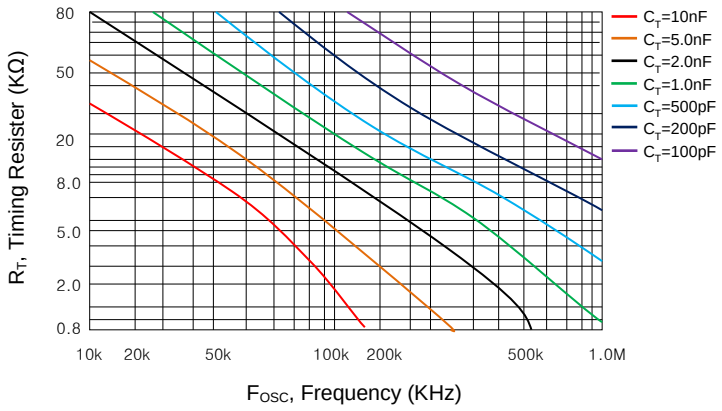


Fig 1. Output Dead Time

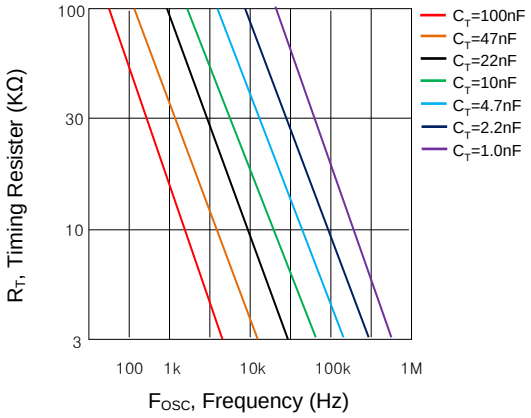


Fig 2. Timing Resistor vs. Frequency

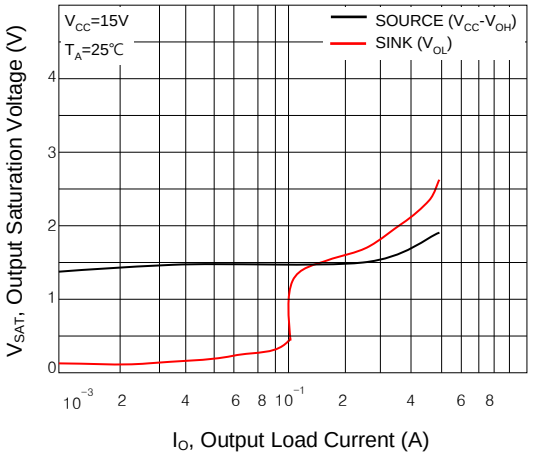


Fig 3. Output Saturation Characteristics

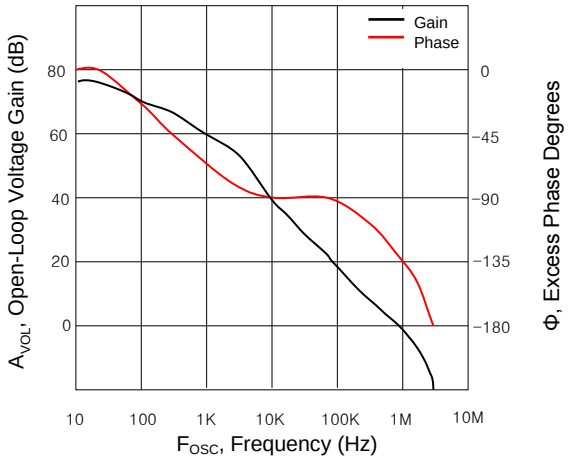


Fig 4. Error Amplifier Open Loop

REVISION NOTICE

The description in this datasheet can be revised without any notice to describe its electrical characteristics properly.