DATA SHEET

LM193A/293/A/393/A/2903

Low power dual voltage comparator

Product data
Supersedes data of 2002 Jan 22

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Philips
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Low power dual voltage comparator LM193A/293/A/393/A/2903

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- Wide single supply voltage range 2.0 V_{DC} to 32 V_{DC}, or dual supplies ±1.0 V_{DC}, to ±16 V_{DC}
- Very low supply current drain (0.8 mA) independent of supply voltage (2.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION

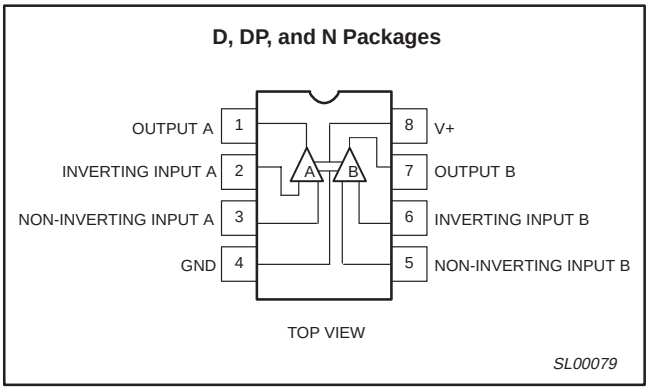


Figure 1. Pin configuration.

EQUIVALENT CIRCUIT

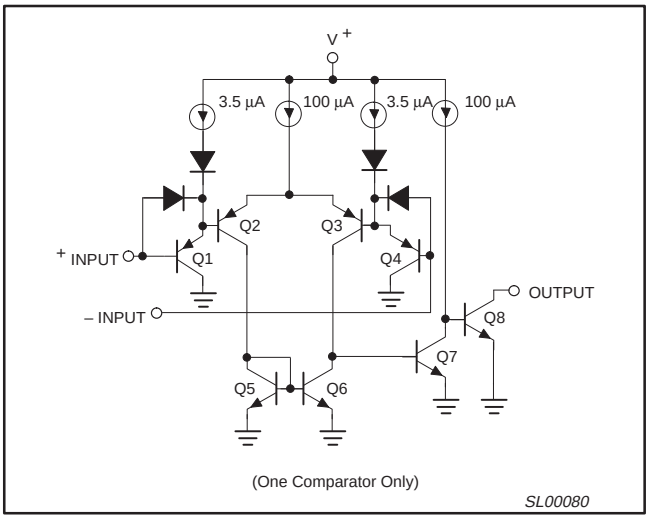


Figure 2. Equivalent circuit.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	LM193AN	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–25 °C to +85 °C	LM293D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–25 °C to +85 °C	LM293N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–25 °C to +85 °C	LM293AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–25 °C to +85 °C	LM293AN	SOT97-1
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	LM393D	SOT96-1
8-Pin Plastic Thin Shrink Small Outline Package (TSSOP)	0 °C to +70 °C	LM393DP	SOT505-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	LM393N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	LM393AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	LM393AN	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +125 °C	LM2903D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +125 °C	LM2903N	SOT97-1
8-Pin Plastic Thin Shrink Small Outline Package (TSSOP)	–40 °C to +125 °C	LM2903DP	SOT505-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_D	Maximum power dissipation, T_{amb} = 25 °C (still-air)[1]		
	N package	1160	mW
	D package	780	mW
	DP package	714	mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN} < –0.3 V_{DC})[3]	50	mA
T_{amb}	Operating temperature range		
	LM193A	–55 to +125	°C
	LM293/293A	–25 to +85	°C
	LM393/393A	0 to +70	°C
	LM2903	–40 to +125	°C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{sld}	Lead soldering temperature (10 sec max)	230	°C

NOTES:

1. Derate above 25 °C, at the following rates:
   N package at 9.3 mW/°C
   D package at 6.2 mW/°C
   DP package at 5.72 mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS

$V+ = 5\ V_{DC}$, LM193A: –55 °C $\leq T_{amb} \leq$ +125 °C, unless otherwise specified. LM293/293A: –25°C $\leq T_{amb} \leq$ +85 °C, unless otherwise specified. LM393/393A: 0 °C $\leq T_{amb} \leq$ +70 °C, unless otherwise specified. LM2903: –40 °C $\leq T_{amb} \leq$ +125 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_{amb} = 25 °C		±1.0	±2.0		±1.0	±2.0		±2.0	±7.0	mV
		Over temp.			±4.0			±4.0		±9	±15	mV
V_{CM}	Input common-mode voltage range[3, 6]	T_{amb} = 25 °C	0		V+–1.5	0		V+–1.5	0		V+–1.5	V
		Over temp.	0		V+–2.0	0		V+–2.0	0		V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all $V_{IN} \geq 0\ V_{DC}$ (or V– if needed)			V+			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range										
		T_{amb} = 25 °C		25	100		25	250		25	250	nA
		Over temp.			300			400		200	500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_{amb} = 25 °C		±3.0	±25		±5.0	±50		±5	±50	nA
		Over temp.			±100			±150		±50	±200	nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1\ V_{DC}$; $V_{IN(+)} = 0$; $V_O \leq 1.5\ V_{DC}$ T_{amb} = 25 °C	6.0	16		6.0	16		6.0	16		mA
	Output leakage current	$V_O = 5\ V_{DC}$; T_{amb} = 25 °C		0.1			0.1			0.1		nA
		$V_{IN(+)} \geq 1 V_{DC}$; $V_{IN(-)}$=0; $V_O = 30\ V_{DC}$; Over temp.			1.0			1.0			1.0	µA
I_{CC}	Supply current	$R_L = \infty$ on both comparators; T_{amb} = 25 °C		0.8	1		0.8	1		0.8	1	mA
		$R_L = \infty$ on both comparators; V+ = 30 V		1	2.5		1	2.5		1	2.5	mA
A_V	Voltage gain	$R_L \geq 15\ k\Omega$; $V+ = 15\ V_{DC}$; T_{amb} = 25 °C	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1\ V_{DC}$; $V_{IN(+)} = 0$; $I_{SINK} \leq 4$ mA T_{amb} = 25 °C		250	400		250	400		400	400	mV
		Over temp.			700			700			700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4\ V_{DC}$; $V_{RL} = 5\ V_{DC}$; $R_L = 5.1\ k\Omega$; T_{amb} = 25 °C		300			300			300		ns
t_R	Response time[5]	$V_{RL} = 5\ V_{DC}$; $R_L = 5.1\ k\Omega$; T_{amb} = 25 °C		1.3			1.3			1.3		µs

DC ELECTRICAL CHARACTERISTICS (Continued)

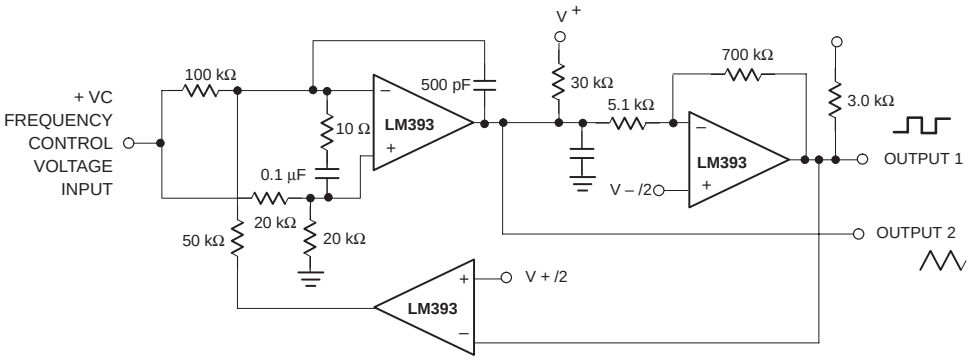
V+ = 5 V_{DC}, LM193A: –55 °C T_{amb} ≤ +125 °C, unless otherwise specified. LM293/293A: –25°C T_{amb} ≤ +85 °C, unless otherwise specified. LM393/393A: 0 °C T_{amb} ≤ +70 °C, unless otherwise specified. LM2903: –40 °C T_{amb} ≤ +125 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM293/393			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_{amb} = 25 °C Over temp.		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	T_{amb} = 25 °C Over temp.	0 0		V+–1.5 V+–2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all $V_{IN} \geq 0$ V_{DC} (or V– if needed)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(–)}$ with output in linear range T_{amb} = 25 °C Over temp.		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)} – I_{IN(–)}$ T_{amb} = 25 °C Over temp.		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(–)} \geq 1$ V_{DC}; $V_{IN(+)} = 0$; $V_O \leq 1.5$ V_{DC} T_{amb} = 25 °C	6.0	16		mA
	Output leakage current	$V_{IN(+)} \geq 1$ V_{DC}; $V_{IN(–)} = 0$, $V_O = 5$ V_{DC}; T_{amb} = 25 °C $V_O = 30$ V_{DC}; over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on both comparators, T_{amb} = 25 °C		0.8	1	mA
		$R_L = \infty$ on both comparators; V+ = 30 V			2.5	mA
A_V	Voltage gain	$R_L \geq 15$ kΩ; V+ = 15 V_{DC}	50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(–)} \geq 1$ V_{DC}; $V_{IN(+)} = 0$; $I_{SINK} \leq 4$ mA T_{amb} = 25 °C Over temp.		250	400 700	mV mV
t_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4$ V_{DC}; $V_{RL} = 5$ V_{DC}; $R_L = 5.1$ kΩ; T_{amb} = 25 °C		300		ns
t_R	Response time[5]	$V_{RL} = 5$ V_{DC}; $R_L = 5.1$ kΩ T_{amb} = 25 °C		1.3		µs

NOTES:

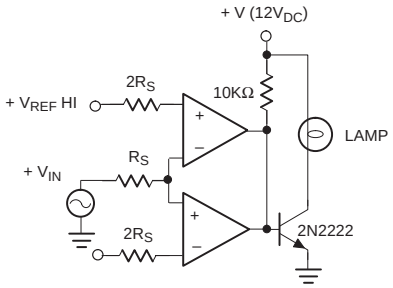
1. Positive excursions of input voltage may exceed the power supply level by 17 V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3 V_{DC} (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4$ V_{DC}, $R_S = 0$ Ω with V+ from 5 V_{DC} to 30 V_{DC} and over the full input common-mode range (0 V_{DC} to V+ –1.5 V_{DC}).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to 30 V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100 mV input step with a 5 mV overdrive.
6. For input signals that exceed V_{CC}, only the over-driven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

EQUIVALENT CIRCUIT

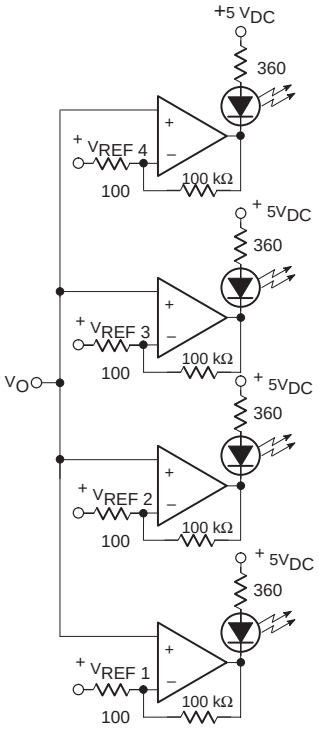


NOTES:
V+ = 30 V_{DC}
+ 250 $mV_{DC} \leq V_C = 50\ V_{DC}$
700H ≤ f_O = 100 kHz

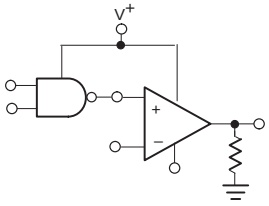
Two–Decade High–Frequency VCO



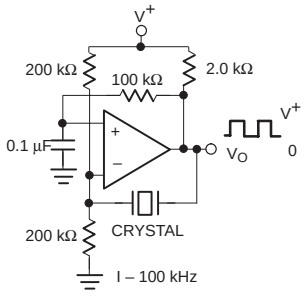
Limit Comparator



Visible Voltage Indicator



TTL-to-MOS Logic Converter



Crystal–Controlled Oscillator

NOTE:
Input of unused comparators should be grounded.

SL00081

Figure 3. Equivalent circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

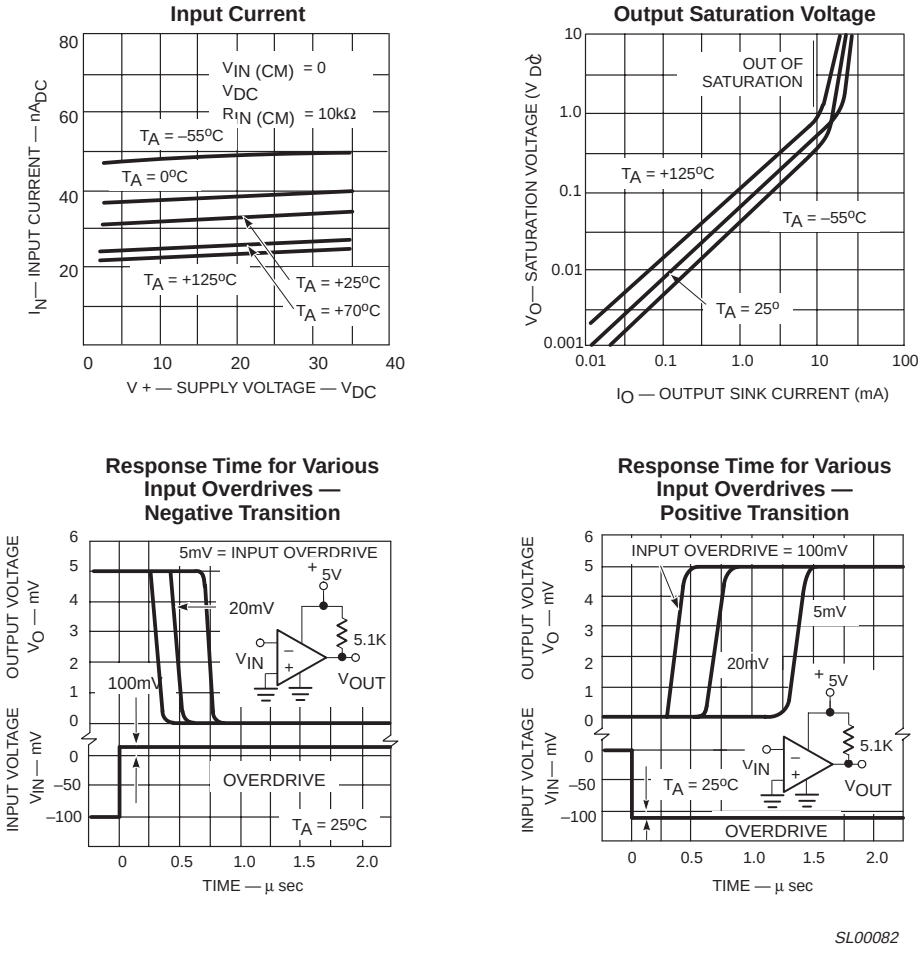
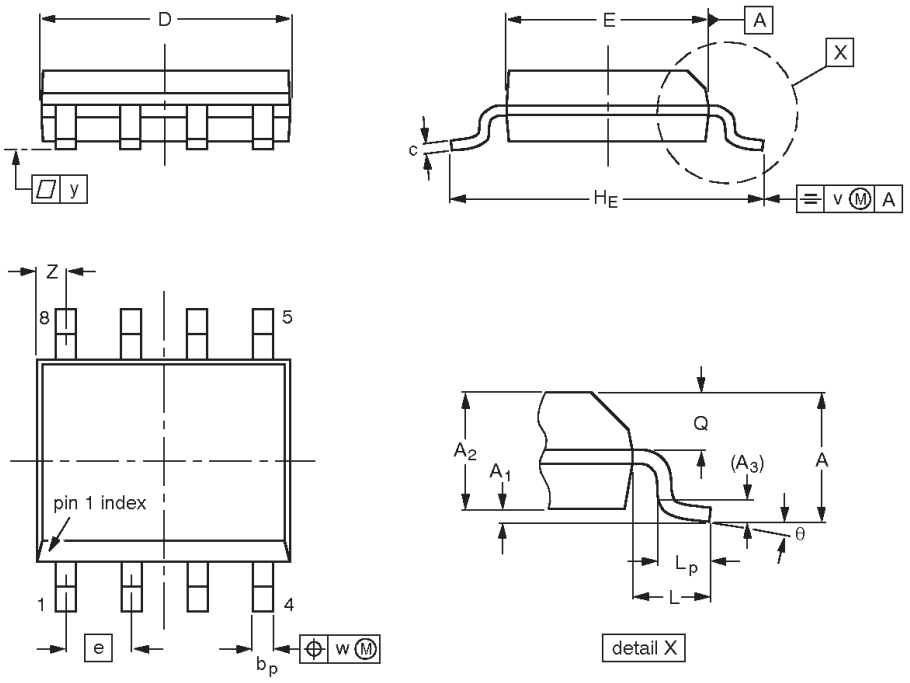
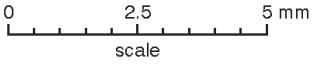


Figure 4. Typical performance characteristics.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

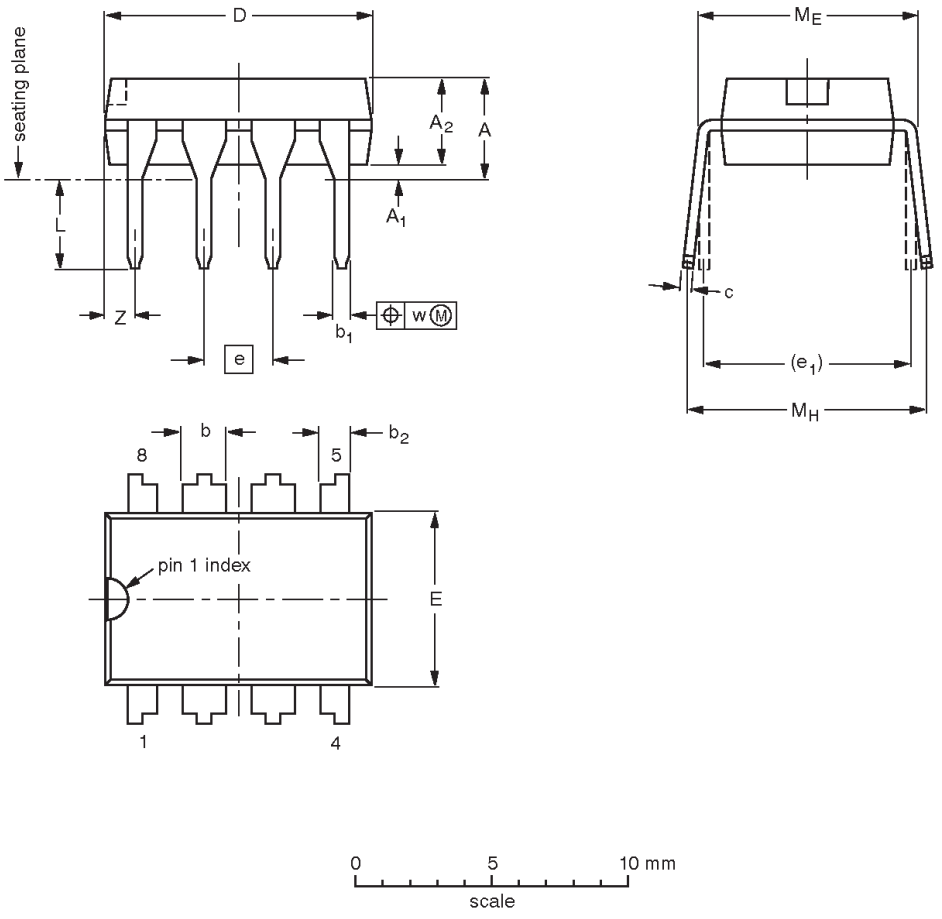
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

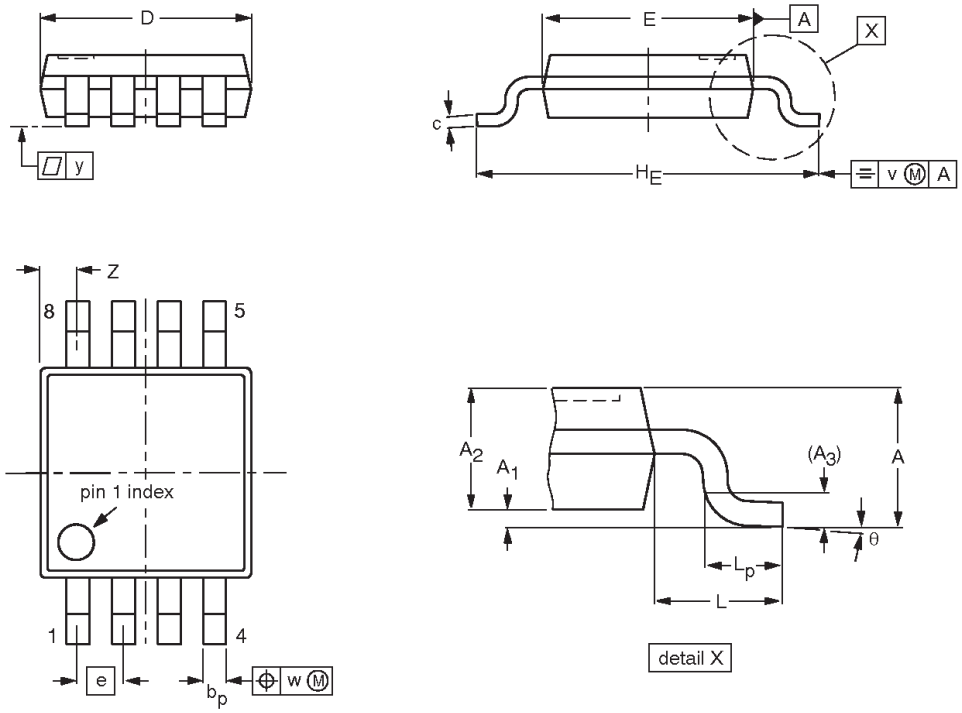
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

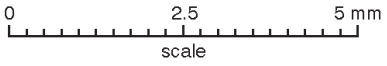
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

NOTES

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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