LM432 Dual Op Amp with On-Chip Fixed 2.5V Reference

Check for Samples: LM432

FEATURES

- **Dual Op Amp Circuitry**
- **(Typical for V_S= 5V)**
- **Input offset voltage 0.6mV**
- **Input offset current 1nA**
- **Input bias current 3nA**
- **Common-mode input voltage range 0V to V_S−1V**
- **Power supply current 150µA**
- **Reference Circuitry**
- **Reference voltage 2.5V**
- **Reference voltage deviation (−40°C to 85°C) 4mV**
- **Sink Current Capability 0.2mA to 10mA**

APPLICATIONS

- **Low cost charging circuitry**
- **Power supplies and adapters**

DESCRIPTION

The LM432 integrates two operational amplifiers and one 2.5V reference. The reference is based on the LMV431 adjustable shunt regulator with the output voltage adjusted to a fixed 2.5V. The Op Amps are similar to the LM358 with a common-mode input range that includes ground. Integrating the reference and Op Amps creates a solution for low cost charging applications.

Connection Diagram

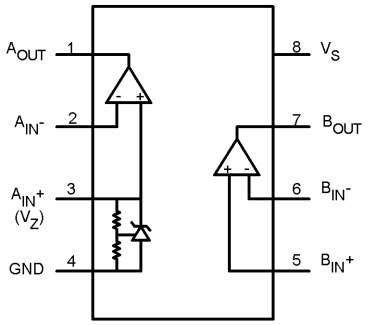

Figure 1. 8-Pin SOIC (Top View)

Application Circuit

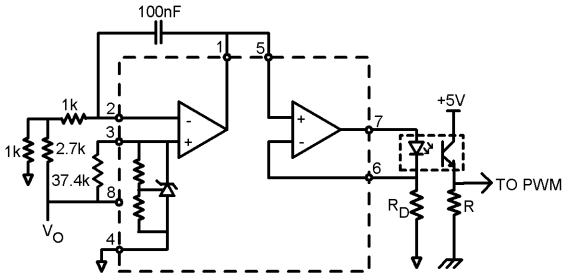

Figure 2. Optocoupler Driver Circuit for Power Supply Isolation

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Suppy Voltage (V_S)	20V
Storage Temperature	−65°C to 150°C
Junction Temperature (T_J)	150°C
ESD Human Body Model	2kV
Input Voltage Range	−0.3V to 20V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to GND = $0V_{DC}$, unless otherwise specified.

Operating Ratings (1), (2)

Temperature Range	−40°C to 85°C
Supply Voltage (3)	2.5V to 16V
Thermal Resistance(θ_{JA})	162°C/W

(1) Operating Rating indicate conditions for which the device is functional. These rating do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = $0V_{DC}$, unless otherwise specified.
(3) Minimum value of operating voltage is for Amplifier B only.

Electrical Characteristics

The following specifications apply for both amplifiers at V_S = 5V, V_{CM} = 2.5V, V_O = 2.5V, R_L = ∞, and T_J = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
OP Amp Circuitry						
V_{OS}	Input Offset Voltage	Amplifier B only	−4	0.6	4	mV
I_{OS}	Input Offset Current	Amplifier B only		1	50	nA
I_B	Input Bias Current	Amplifier B only		3	150	nA
V_{CM}	Common-Mode Input Voltage Range	Amplifier B only, CMRR > 50dB	0		V_S-1	V
I_S	Power Supply Current	Total for both amplifiers		150	500	µA
A_V	Voltage Gain	V_S = 16V, 1V < V_O < 11V, R_L = 10kΩ connected to V_S/2	65	100		dB
V_{OL}	Output Voltage Low			2	50	mV
V_{OH}	Output Voltage High		V_S – 1.5	V_S – 1.3		V
I_{SOURCE}	Output Current Source		20	30		mA
I_{SINK}	Output Current Sink		5	11		mA
Reference Circuitry For Op Amp A The following specifications apply for I_Z = 200µA and T_J = 25°C, unless otherwise noted.						
V_Z	Reference Voltage at IN^+ Terminal		2.450	2.5	2.550	V
V_{ZDEV}	Reference Voltage Deviation at IN^+ Terminal Over Temperature (3) (4)	−40°C ≤ T_J ≤ 85°C		4	65	mV
$I_{Z\ (MIN)}$	Minimum Cathode Current for Regulation at IN^+ (V_Z) Terminal			150	200	µA
r_z	Dynamic Output Impedance (5)	200µA < I_Z < 1mA, Freq = 0Hz		0.2		Ω

(1) Guaranteed to National's Average Outgoing Quality Level (AOQL).
(2) Typicals represent the most likely parametic norm.
(3) Reference voltage deviation, V_{ZDEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.
(4) Typical Temperature drift ΔV/ΔT = 12.8ppm/°C
(5) The Dynamic Output Impendance, r_z, is defined as $r_z = \Delta V_Z/\Delta I_Z$.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM432MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LM432MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM432MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LM432MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

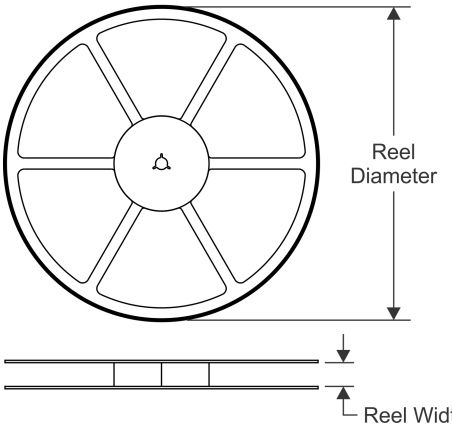
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

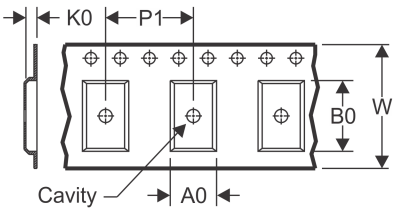
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

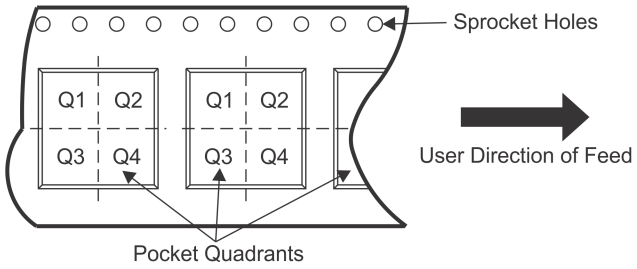


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

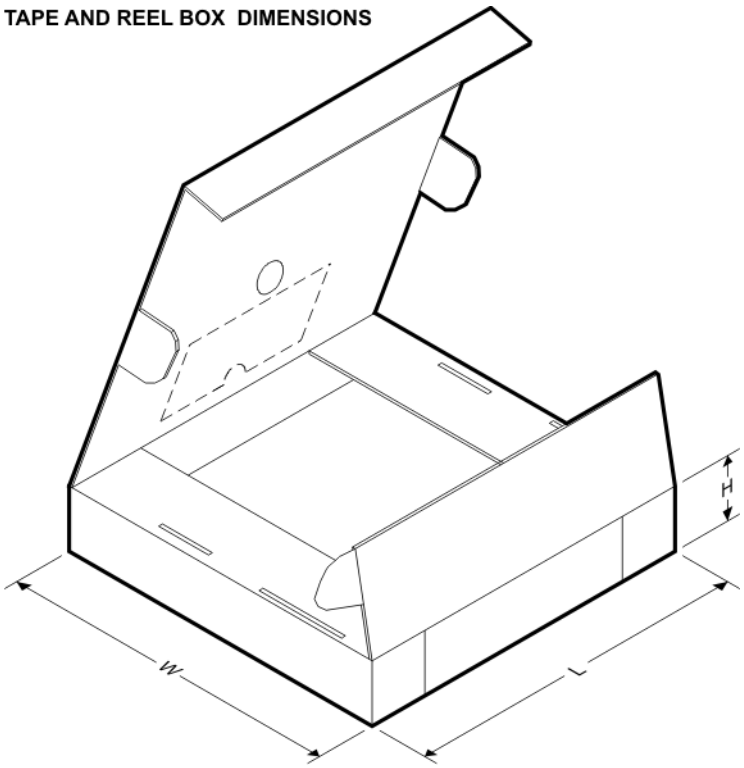
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM432MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM432MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

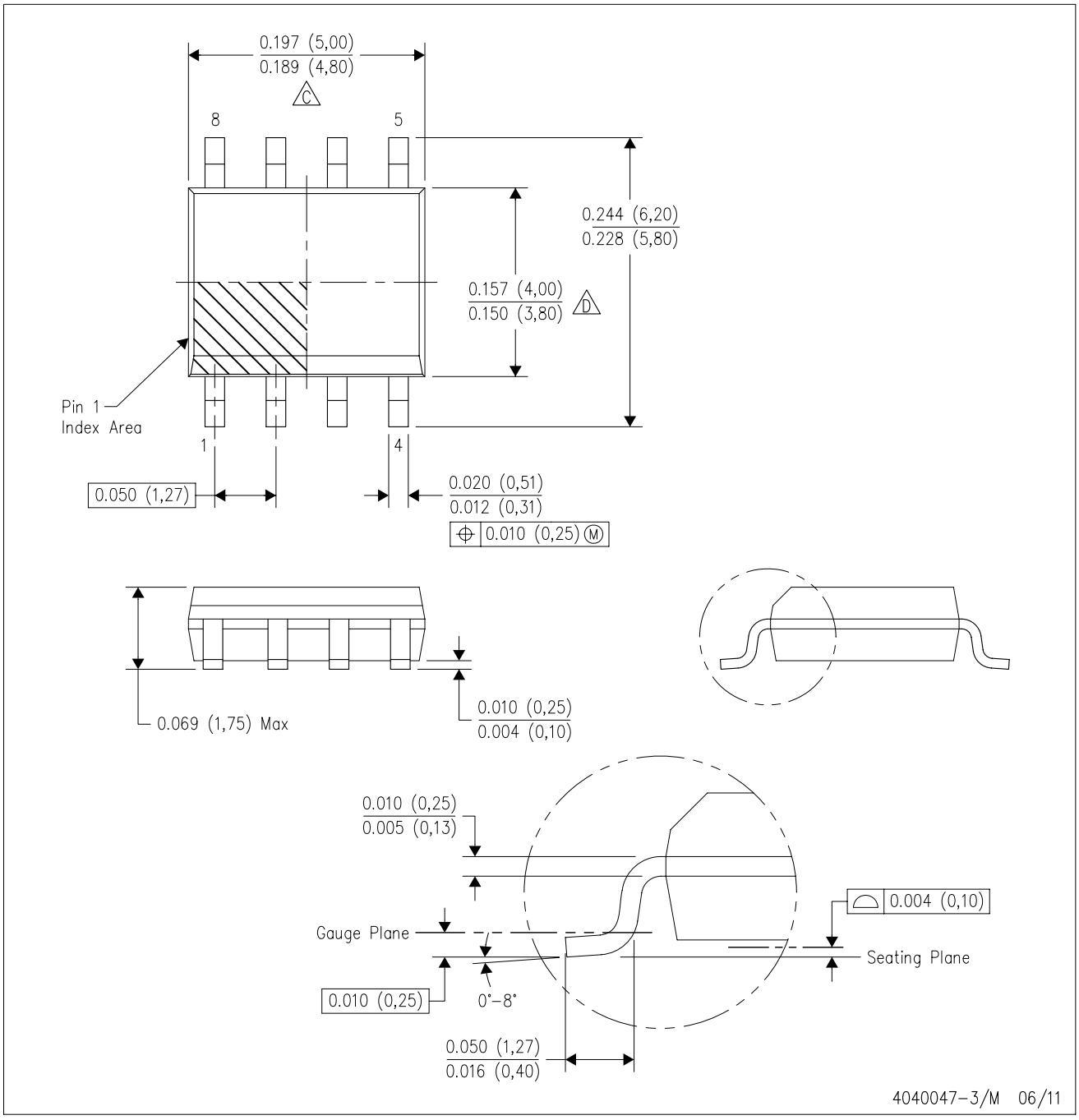
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM432MAX	SOIC	D	8	2500	349.0	337.0	45.0
LM432MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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