LM5041B Cascaded PWM Controller

Check for Samples: LM5041B

FEATURES

- **Internal Start-up Bias Regulator**
- **Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis**
- **Current Mode Control**
- **Internal Error Amplifier with Reference**
- **Cycle-by-cycle Over-Current Protection**
- **Leading Edge Blanking**
- **Programmable Push-Pull Overlap or Dead Time**
- **Internal 1.5A Push-Pull Gate Drivers**
- **Programmable Soft-Start**
- **Programmable Oscillator with Sync Capability**
- **Precision Reference**
- **Thermal Shutdown**

APPLICATIONS

- **Telecommunication Power Converters**
- **Industrial Power Converters**
- **Multi-Output Power Converters**

PACKAGES

- **TSSOP-16**
- **WSON-16 (5x5 mm) Thermally Enhanced**

DESCRIPTION

The LM5041B PWM controller contains all of the features necessary to implement either current-fed or voltage-fed push-pull or bridge power converters. These “Cascaded” topologies are well suited for multiple output and higher power applications. The LM5041B includes these four control outputs: the buck stage controls (HD and LD) and the push-pull control outputs (PUSH and PULL). Push-pull outputs are driven at 50% nominal duty cycle at one half of the switching frequency of the buck stage and can be configured for either a specified overlap time (for current-fed applications) or a specified non-overlap time (for voltage-fed applications). Push-pull stage MOSFETs can be driven directly from the internal gate drivers while the buck stage requires an external driver such as the LM5102. The LM5041B includes a high-voltage start-up regulator that operates over a wide input range of 15V to 100V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 1 MHz and total propagation delays of less than 100 ns. Additional features include line Under-Voltage Lock-Out (UVLO), Soft-Start, an error amplifier, precision voltage reference, and thermal shutdown.

The differences between LM5041, LM5041A and LM5041B are as follows: In the LM5041A and the LM5041B version, the hiccup mode over-current protection is not employed and the VCC bias regulator is not disabled by a low state at the SS pin. In the LM5041B version, both the high and low side buck stage gate drivers are forced to a low state when the controller is disabled. In the LM5041 and the LM5041B version, the buck stage controller is disabled by either a low state at the UVLO pin or a low state at the SS pin. Also in the LM5041B version, the REF pin 5V regulator is not disabled by a UVLO pin low state.

Typical Application Circuit

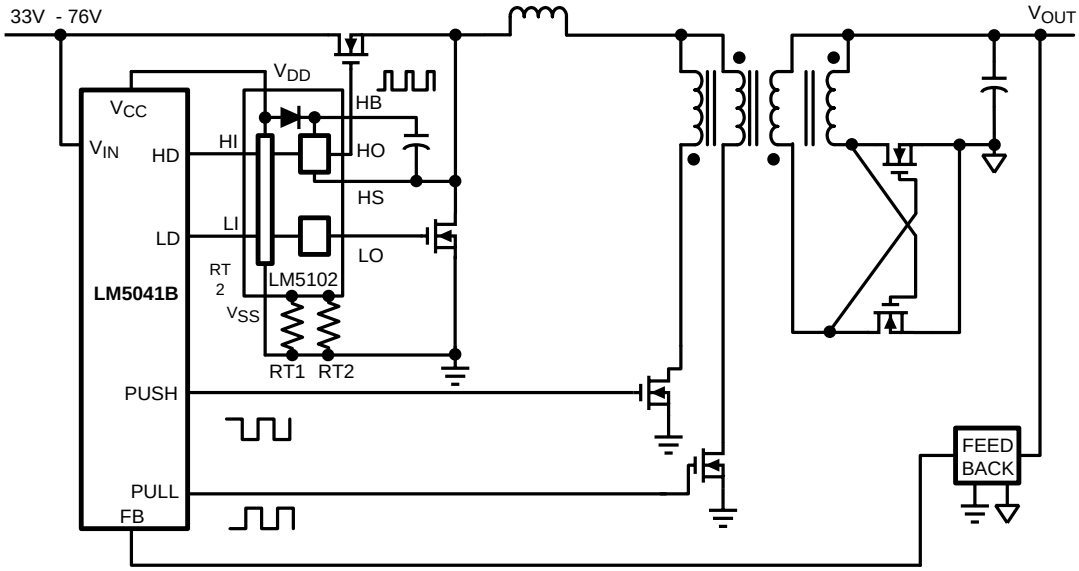


Figure 1. Simplified Cascaded Push-Pull Power Converter

Connection Diagram

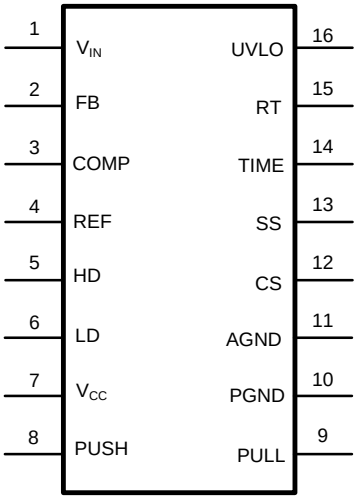


Figure 2. 16-Lead TSSOP, WSON

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Description	Pin Application Information
1	V_{IN}	Source Input Voltage	Input to start-up regulator. Input range 15V to 100V.
2	FB	Feedback Signal	Inverting input for the internal error amplifier. The non-inverting input is connected to a 0.75V reference.
3	COMP	Output of the Internal Error Amplifier	There is an internal 5 kΩ resistor pull-up on this pin. The error amplifier provides an active sink.
4	REF	Precision 5 volt reference output	Maximum output current: 10 mA. Locally decouple with a 0.1 µF capacitor. Reference stays low until the V_{CC} UV are satisfied.
5	HD	Main Buck PWM control output	Buck switch PWM control output. The maximum duty cycle clamp for this output corresponds to an off time of typically 240 ns per cycle. The LM5101 or LM5102 Buck stage gate driver can be used to level shift and drive the Buck switch MOSFET.
6	LD	Buck Sync Switch control output	Sync Switch control output. Inversion of HD output during normal operation. The LM5101 or LM5102 lower drive can be used to drive the synchronous rectifier switch.
7	V_{CC}	Output of the internal high voltage start-up regulator. Regulated to 9 volts.	If an auxiliary winding raises the voltage on this pin above the regulation set-point, the internal start-up regulator will shutdown, reducing the IC power dissipation.
8	PUSH	Output of the push-pull drivers	Output of the push-pull gate driver. Output capability of 1.5A peak .
9	PULL	Output of the push-pull drivers	Output of the push-pull gate driver. Output capability of 1.5A peak.
10	PGND	Power ground	Connect directly to analog ground.
11	AGND	Analog ground	Connect directly to power ground.
12	CS	Current sense input	Current sense input to the PWM comparator (current mode control). There is a 50 ns leading edge blanking on this pin. If CS exceeds 0.5V, the PWM controller will go into cycle by cycle current limit.
13	SS	Soft-Start control	An external capacitor and an internal 10 µA current source, set the soft-start ramp. Both HD and LD will be forced to a low state if the SS pin is below the shutdown threshold of 0.45V.
14	TIME	Push-Pull overlap and dead time control	An external resistor (R_{SET}) sets the overlap time or dead time for the push-pull outputs. A resistor connected between TIME and GND produces overlap. A resistor connected between TIME and REF produces dead time.
15	RT / SYNC	Oscillator timing resistor pin and sync	An external resistor sets the oscillator frequency. This pin will also accept an external oscillator.
16	UVLO	Line Under-Voltage Shutdown	An external divider from the power source sets the shutdown levels. Threshold of operation equals 2.5V. Hysteresis is set by a switched internal current source (20 µA).
WSON DAP	SUB	Die substrate	The exposed die attach pad of the WSON package should be connected to a PCB thermal pad at ground potential. For additional information on using TI's No Pull Back WSON package, please refer to Application Note AN-1187 (literature number SNOA401).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

V_{IN} to GND	100V
V_{CC} to GND	16V
All Other Inputs to GND	-0.3 to 7V
Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
ESD Rating(3)	±2 kV
Lead temperature (4)	
Wave	4 seconds at 260°C
Infrared	10 seconds at 240°C
Vapor Phase	75 seconds at 219°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test Method is per JESD-22-A114.
(4) For detailed information on soldering plastic TSSOP and WSON packages, please refer to Application Note *AN-1520: A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (literature number SNVA183), Application Note AN-1187 (literature number SNOA401), or go to www.ti.com/packaging for more information.

OPERATING RATINGS(1)

V_{IN}	15 to 90V
Junction Temperature	-40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated the following conditions apply: V_{IN} = 48V, V_{CC} = 10V, RT = 26.7 kΩ, R_{SET} = 20 kΩ. (1). Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the Operating Junction Temperature (T_J) range of **-40°C to +125°C**. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator						
V_{CC} Reg	V_{CC} Regulation	Open circuit	**8.7**	9	**9.3**	V
	V_{CC} Current Limit	(1)	**15**	25	-	mA
I-V_{IN}	Startup Regulator Leakage (external Vcc Supply)	V_{IN} = 100V	-	145	**500**	µA
	Shutdown Current (Iin)	UVLO = 0V, V_{CC} = open	-	350	**450**	µA
V_{CC} Supply						
	V_{CC} Under-Voltage Lock-Out Threshold	V_{CC} rising	**V_{CC} Reg - 400 mV**	V_{CC} Reg - 275 mV	-	V
	V_{CC} Under-Voltage Lock-Out Hysteresis		**1.7**	2.1	**2.6**	V
	Supply Current (I_{CC})	C_L = 0	-	3	**4**	mA

(1) Device thermal limitations may limit usable range.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated the following conditions apply: V_{IN} = 48V, V_{CC} = 10V, RT = 26.7 kΩ, R_{SET} = 20 kΩ. (1). Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the Operating Junction Temperature (T_J) range of **-40°C to +125°C**. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Error Amplifier						
GBW	Gain Bandwidth		-	3	-	MHz
	DC Gain		-	80	-	dB
	Input Voltage	V_{FB} = COMP	**0.735**	0.75	**0.765**	V
	COMP Sink Capability	V_{FB} = 1.5V, COMP= 1V	**4**	8	-	mA
Reference Supply						
V_{REF}	Ref Voltage	I_{REF} = 0 mA	**4.85**	5	**5.15**	V
	Ref Voltage Regulation	I_{REF} = 0 to 10 mA	-	25	**50**	mV
	Ref Current Limit		**15**	20	-	mA
Current Limit						
	ILIM Delay to Output	CS Step from 0 to 0.6V Time to Onset of OUT Transition (90%) C_L = 0	-	40	-	ns
	Cycle by Cycle Threshold Voltage		**0.45**	0.5	**0.55**	V
	Leading Edge Blanking Time		-	50	-	ns
	CS Sink Current (clocked)	CS = 0.3V	**2**	5	-	mA
Soft-Start						
	Soft-Start Current Source		**7**	10	**13**	µA
	Soft-Start to COMP Offset		**0.35**	0.55	**0.75**	V
	Shutdown Threshold		**0.25**	0.5	**0.75**	V
Oscillator						
	Frequency1	RT = 26.7 kΩ	180 **175**	200	220 **225**	kHz
	Frequency2	RT = 7.87 kΩ	**515**	600	**685**	kHz
	Sync threshold		-	3	**3.5**	V
PWM Comparator						
	Delay to Output	COMP = 2V, CS stepped 0 to 0.4V Time to onset of OUT transition low	-	25	-	ns
	Max Duty Cycle	TS = Oscillator Period	-	(Ts-240ns) / Ts	-	%
	Min Duty Cycle	COMP = 0V	-	-	0	%
	COMP to PWM Comparator Gain		-	0.32	-	
	COMP Open Circuit Voltage	FB = 0V	**4.1**	4.8	**5.5**	V
	COMP Short Circuit Current	FB = 0V, COMP = 0V	**0.6**	1	**1.4**	mA
Slope Compensation						
	Slope Comp Amplitude	Delta increase at PWM Comparator to CS	-	110	-	mV
UVLO Shutdown						
	Under-Voltage Shutdown		**2.44**	2.5	**2.56**	V
	Under-voltage Shutdown Hysteresis Current Source		**16**	20	**24**	µA

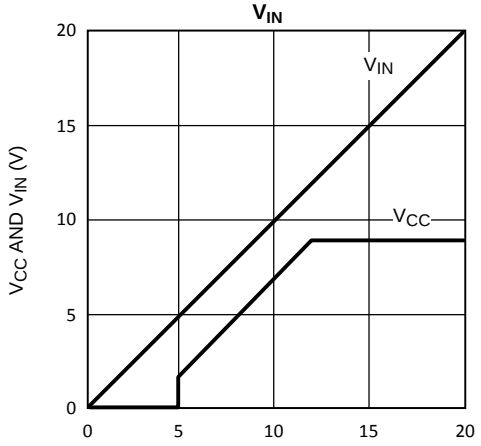
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated the following conditions apply: V_{IN} = 48V, V_{CC} = 10V, RT = 26.7 kΩ, R_{SET} = 20 kΩ. (1). Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the Operating Junction Temperature (T_J) range of **-40°C to +125°C**. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

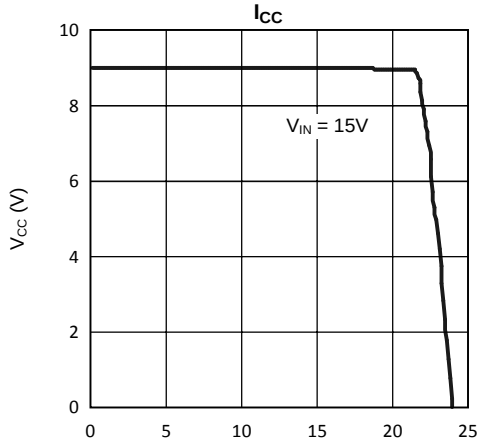
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Buck Stage Outputs						
	Output High level		-	5 (V_{REF})	-	V
	Output High Saturation	I_{OUT} = 10 mA, REF = V_{OUT}	-	0.5	**1**	V
	Output Low Saturation	I_{OUT} = −10 mA	-	0.5	**1**	V
	Rise Time	C_L = 100 pF	-	10	-	ns
	Fall Time	C_L = 100 pF	-	10	-	ns
Push-Pull Outputs						
	Overlap Time	R_{SET} = 20 kΩ Connected to GND, 50% to 50% Transitions	**60**	90	**120**	ns
	Dead Time	R_{SET} = 20kΩ Connected to REF, 50% to 50% Transitions	**65**	95	**125**	ns
	Output High Saturation	I_{OUT} = 50 mA V_{CC} - V_{OUT}	-	0.25	**0.5**	V
	Output Low Saturation	I_{OUT} = 100 mA	-	0.5	**1**	V
	Rise Time	C_L = 1 nF	-	20		ns
	Fall Time	C_L = 1 nF	-	20	-	ns
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temp.		-	165	-	°C
	Thermal Shutdown Hysteresis		-	25	-	°C
Thermal Resistance						
θ_{JA}	Thermal Resistance Junction to Ambient	TSSOP Package	-	125	-	°C/W
		WSON Package	-	32	-	°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

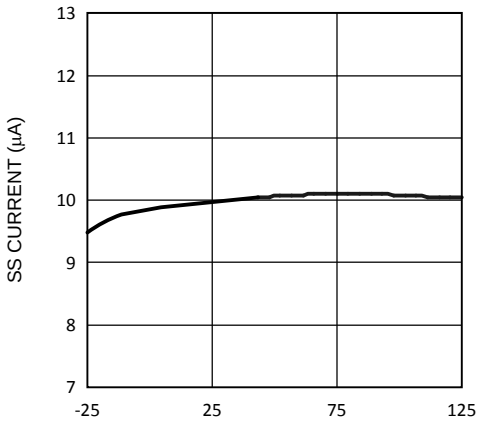
V_{CC} and V_{IN} vs V_{IN}



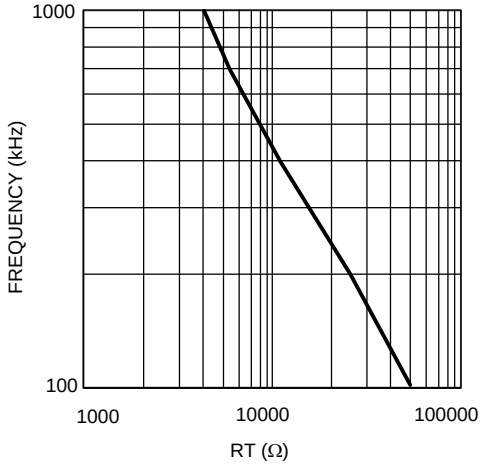
V_{CC} vs I_{CC}



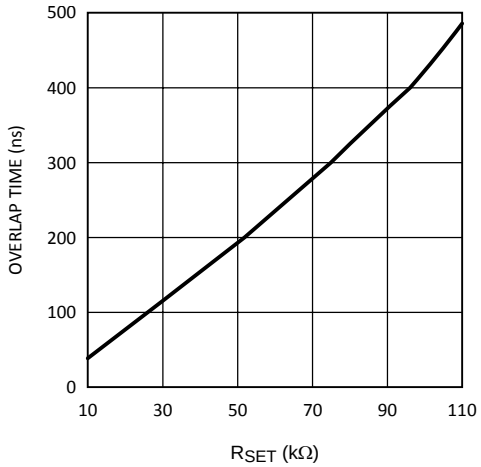
SS Pin Current vs Temp



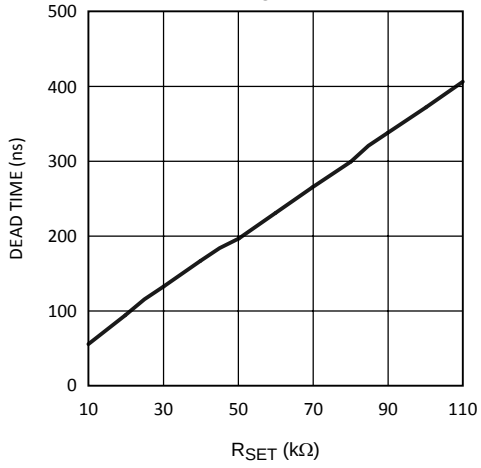
Frequency vs RT



Overlap Time vs R_{SET}

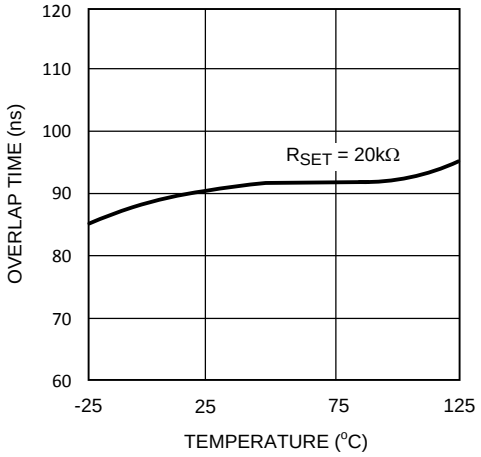


Dead Time vs R_{SET}

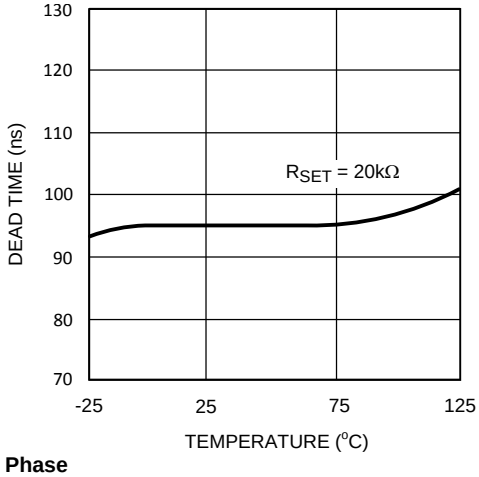


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

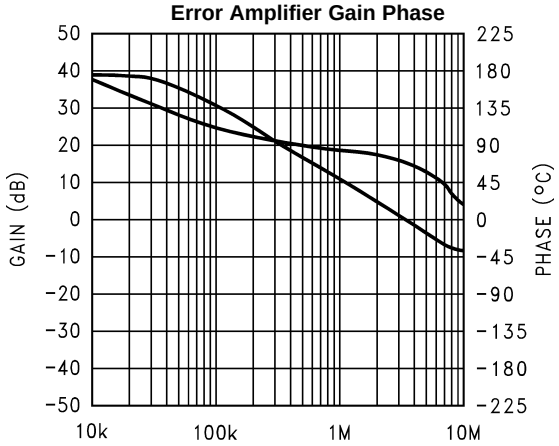
Overlap Time vs Temp



Dead Time vs Temp



Error Amplifier Gain Phase



BLOCK DIAGRAM

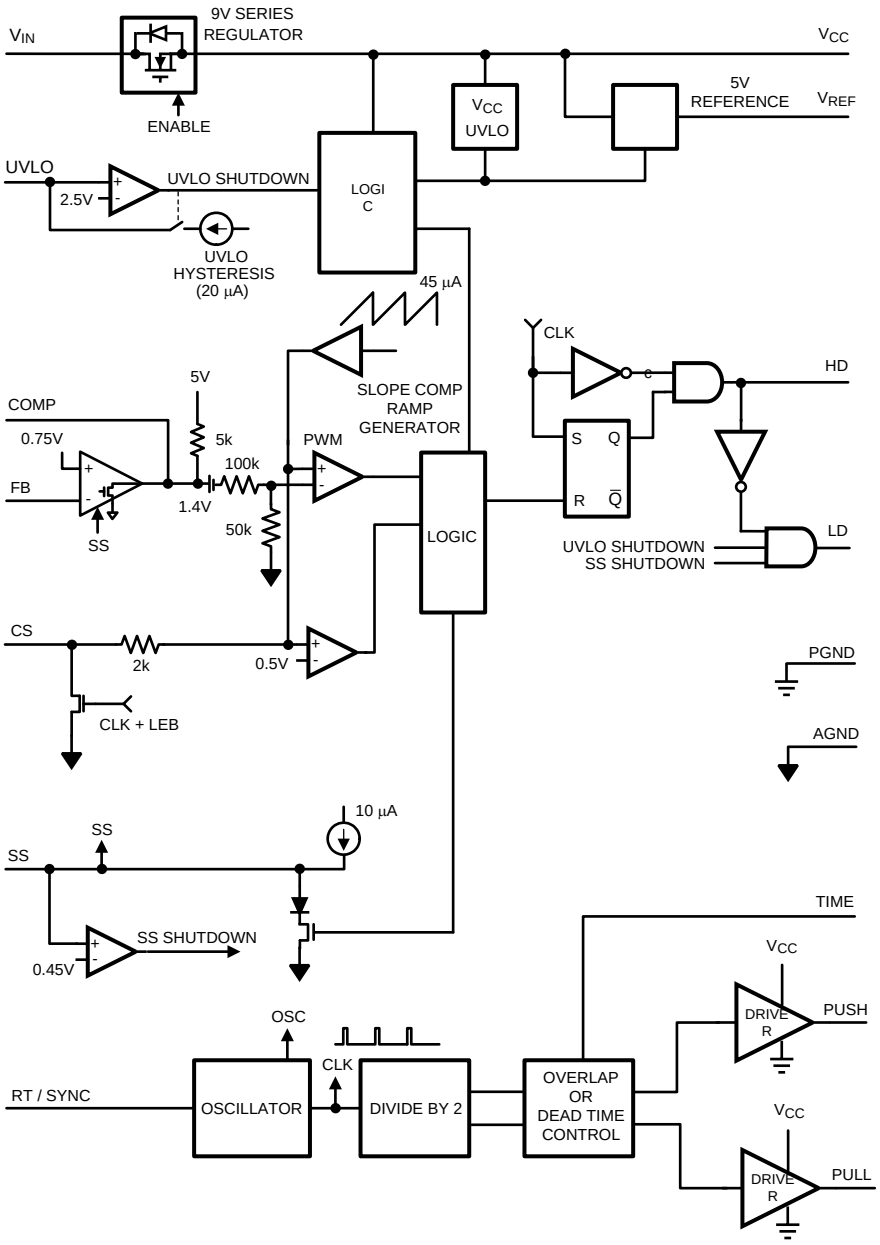


Figure 3. Simplified Block Diagram

DETAILED OPERATING DESCRIPTION

The LM5041B PWM controller contains all of the features necessary to implement either current-fed or voltage-fed push-pull or bridge power converters. These “Cascaded” topologies are well suited for multiple output and higher power applications. The LM5041B includes these four control outputs: the buck stage controls (HD and LD) and the push-pull control outputs (PUSH and PULL). Push-pull outputs are driven at 50% nominal duty cycle at one half of the switching frequency of the buck stage and can be configured for either a specified overlap time (for current-fed applications) or a specified non-overlap time (for voltage-fed applications). Push-pull stage MOSFETs can be driven directly from the internal gate drivers while the buck stage requires an external driver such as the LM5102. The LM5041B includes a high-voltage start-up regulator that operates over a wide input range of 15V to 100V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 1 MHz and total propagation delays of less than 100 ns. Additional features include line Under-Voltage Lock-Out (UVLO), Soft-Start, an error amplifier, precision voltage reference, and thermal shutdown.

High Voltage Start-Up Regulator

The LM5041B contains an internal high-voltage start-up regulator, thus the input pin (Vin) can be connected directly to the line voltage. The regulator output is internally current limited to 15 mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the Vcc pin. The recommended capacitance range for the Vcc regulator is 0.1µF to 100 µF. When the voltage on the Vcc pin reaches the regulation point of 9V, the internal voltage reference (REF) reaches its regulation point of 5V, and the soft-start capacitor is charged above its shutdown threshold, the controller outputs are enabled. The Buck stage outputs will remain enabled until Vcc falls below 7V, the REF pin voltage falls below approximately 3V, the SS pin is forced below the 0.45V shutdown threshold or the line Under-Voltage Lock-Out detector indicates that Vin is out of range. The push-pull outputs continue switching until the REF pin voltage falls below approximately 3V. In typical applications, an auxiliary transformer winding is connected through a diode to the Vcc pin. This winding must raise the Vcc voltage above 9.3V to shut off the internal start-up regulator. Powering V_{CC} from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The recommended capacitance range for the Vref regulator output is 0.1µF to 10 µF.

The external V_{CC} capacitor must be sized such that the capacitor maintains a V_{CC} voltage greater than 7V during the initial start-up. During a fault mode when the converter auxiliary winding is inactive, external current draw on the V_{CC} line should be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage into the two pins.

Line Under-Voltage Detector

The LM5041B contains a line Under-Voltage Lock-Out (UVLO) circuit. An external set-point resistor divider from V_{IN} to ground sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 2.5V when V_{IN} is in the desired operating range. If the Under-Voltage threshold is not met, both HD and LD will be forced to low state and VCC regulator will be disabled while the push-pull outputs continue switching until the REF pin voltage falls below approximately 3V. ULVO hysteresis is accomplished with an internal 20 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin falls below the 2.5V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. By shorting the UVLO pin to ground, the converter can be disabled.

Buck Stage Control Outputs

The LM5041B Buck switch maximum duty cycle clamp ensures that there will be sufficient off time each cycle to recharge the bootstrap capacitor used in the high side gate driver. The Buck switch is specified to be off, and the sync switch on, for at least 250 ns per switching cycle. The Buck stage control outputs (LD and HD) are CMOS buffers with logic levels of 0 to 5V.

During any fault state or Under-Voltage off state, both HD and LD state will be forced to low by the buck stage control.

Push-Pull Outputs

The push pull outputs operate continuously at a nominal 50% duty cycle. A distinguishing feature of the LM5041B is the ability to accurately configure either dead time (both-off) or overlap time (both-on) on the complementary push-pull outputs. The overlap/dead time magnitude is controlled by a resistor connected to the TIME pin on the controller. The TIME pin holds one end of the resistor at 2.5V and the other end of the resistor should be connected to either REF for dead time control setting or to GND for overlap control. The polarity of the current in the TIME is detected by the LM5041B The magnitude of the overlap/dead time can be calculated as follows:

Overlap Time (ns) = (3.66 x R_{SET}) + 7

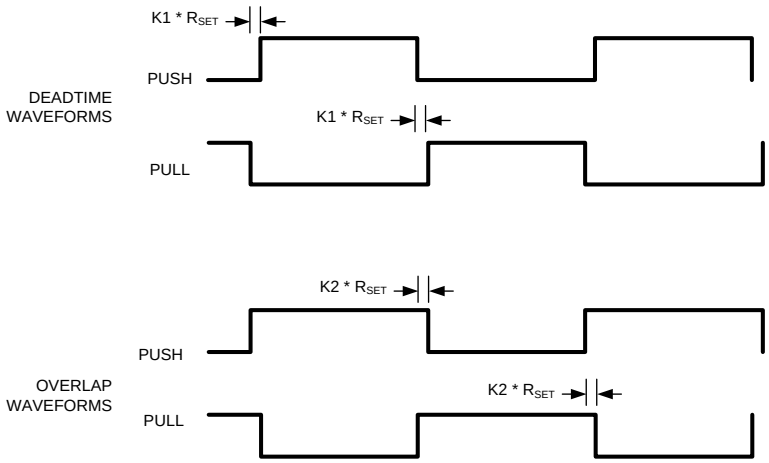
Overlap Time in ns, R_{SET} connected to GND, R_{SET} in kΩ

Dead Time (ns) = (3.69 x R_{SET}) + 21

Dead Time in ns, R_{SET} connected to REF, R_{SET} in kΩ

Recommended R_{SET} programming range: 10 kΩ to 100 kΩ

Current-fed designs require a period of overlap to insure there is a continuous path for the buck inductor current. Voltage-fed designs require a period of dead time to insure there is no time when the push-pull transformer acts as a shorted turn to the low impedance sourcing node. The push-pull outputs alternate continuously under all conditions provided REF the voltage is greater than 3V.



PWM Comparator

The PWM comparator compares the slope compensated current ramp signal to the loop error voltage from the internal error amplifier (COMP pin). This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The comparator polarity is such that 0V on the COMP pin will produce zero duty cycle in the buck stage.

Error Amplifier

An internal high gain wide-bandwidth error amplifier is provided within the LM5041B. The amplifier's non-inverting input is tied to a 0.75V reference. The inverting input is connected to the FB pin. In non-isolated applications the power converter output is connected to the FB pin via the voltage setting resistors. Loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amp is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ground. An internal 5 kΩ pull-up resistor between the 5V reference and the COMP pin can be used as the pull-up for an opto-coupler in isolated applications.

Current Limit/Current Sense

The LM5041B provides cycle-by-cycle over-current protection. If the voltage at the CS comparator (CS pin voltage plus slope comp voltage) exceeds 0.5V the present buck stage duty cycle is terminated (cycle by cycle current limit). A small RC filter located near the controller is recommended to filter current sense signals at the CS pin. An internal MOSFET discharges the external CS pin for an additional 50 ns at the beginning of each cycle to reduce the leading edge spike that occurs when the buck stage MOSFET is turned on.

The LM5041B current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed close to the device and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. A resistor may be used for current sensing instead of a transformer, located in the push-pull transistor sources, but a low inductance type of resistor is required. When designing with a sense resistor, all of the noise sensitive low power grounds should be connected together around the IC and a single connection should be made to the high current power ground (sense resistor ground point).

Oscillator and Sync Capability

The LM5041B oscillator is set by a single external resistor connected between the RT pin and GND. To set a desired oscillator frequency (F), the necessary RT resistor can be calculated from:

$$RT = \frac{(1/F) - 235 \times 10^{-9}}{182 \times 10^{-12}}\ \Omega \tag{1}$$

The buck stage will switch at the oscillator frequency and each push-pull output will switch at half the oscillator frequency in a push-pull configuration. The LM5041B can also be synchronized to an external clock. The external clock must have a higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100 pF capacitor. A peak voltage level greater than 3V is required for detection of the sync pulse. The sync pulse width should be set in the 15 ns to 150 ns range by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to 2V. The RT resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND).

Slope Compensation

The PWM comparator compares the current sense signal to the voltage at the COMP pin. The output stage of the internal error amplifier generally drives the COMP pin. At duty cycles greater than 50%, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed ramp signal (slope compensation) to the current sense ramp, oscillations can be avoided. The LM5041B integrates this slope compensation by buffering the internal oscillator ramp and summing a current ramp generated by the oscillator internally with the current sense signal. Additional slope compensation may be provided by increasing the source impedance of the current sense signal.

Soft-Start and Shutdown

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses and surges. At power on, a 10 µA current is sourced out of the soft-start pin (SS) to charge an external capacitor. The capacitor voltage will ramp up slowly and will limit the maximum duty cycle of the buck stage. In the event of a fault as indicated by V_{CC} Under-voltage, line Under-voltage the output drivers are disabled and the soft-start capacitor is discharged to 0.7V. When the fault condition is no longer present, a soft-start sequence will begin again and buck stage duty cycle will gradually increase as the soft-start capacitor is charged.

The SS pin also serves as an enable input of HD and LD. Both HD and LD will be forced to a low state if the SS pin is below the shutdown threshold of 0.45V.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low-power standby state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

Differences Between LM5041, LM5041A and LM5041B

There are five differences between LM5041, LM5041A and LM5041B. In the LM5041A and the LM5041B versions, the hiccup mode over-current protection is not employed and the VCC bias regulator is not disabled by SS pin shutdown state. In the LM5041B version, both HD and LD will be low state when the PWM controller disabled. In the LM5041 and the LM5041B version, PWM controller is disabled by either a UVLO pin low state or SS pin shutdown state. Also in the LM5041B version, the REF pin output is not disabled by a UVLO pin low state. However, if VCC does not receive power from an external source, the UVLO pin low state will disable the internal VCC regulator and a VCC under-voltage condition will eventually disable REF as the VCC voltage falls.

Differences Between LM5041, LM5041A and LM5041B

ITEM	LM5041	LM5041A	LM5041B
Hiccup mode over-current protection	Available	N/A	N/A
VCC disabled by SS shutdown	Yes	No	No
REF disabled by UVLO pin low state	Yes	Yes	No
BUCK controller disabled by SS shutdown	Yes	No	Yes
BUCK driver states when the controller disabled	HD : LOW LD :HIGH	HD : LOW LD : HIGH	HD : LOW LD : LOW

Logic Table

MODE	CONTROLS		DEVICE	PIN STATES				
	UVLO	SS		VCC	REF	HD	LD	PUSH&PULL
Normal Operation	HIGH	-	**LM5041**	9V	5V	PWM	$\overline{\text{PWM}}$	50% Duty Cycle
			LM5041A					
			LM5041B					
UVLO Shutdown	LOW	-	**LM5041**	GND	GND	LOW	HIGH	LOW
			LM5041A					
			LM5041B				LOW	
SS Shutdown	HIGH	LOW	**LM5041**	GND	GND	LOW	HIGH	LOW
			LM5041A	9V	5V			50% Duty Cycle
			LM5041B				LOW	

Typical Application

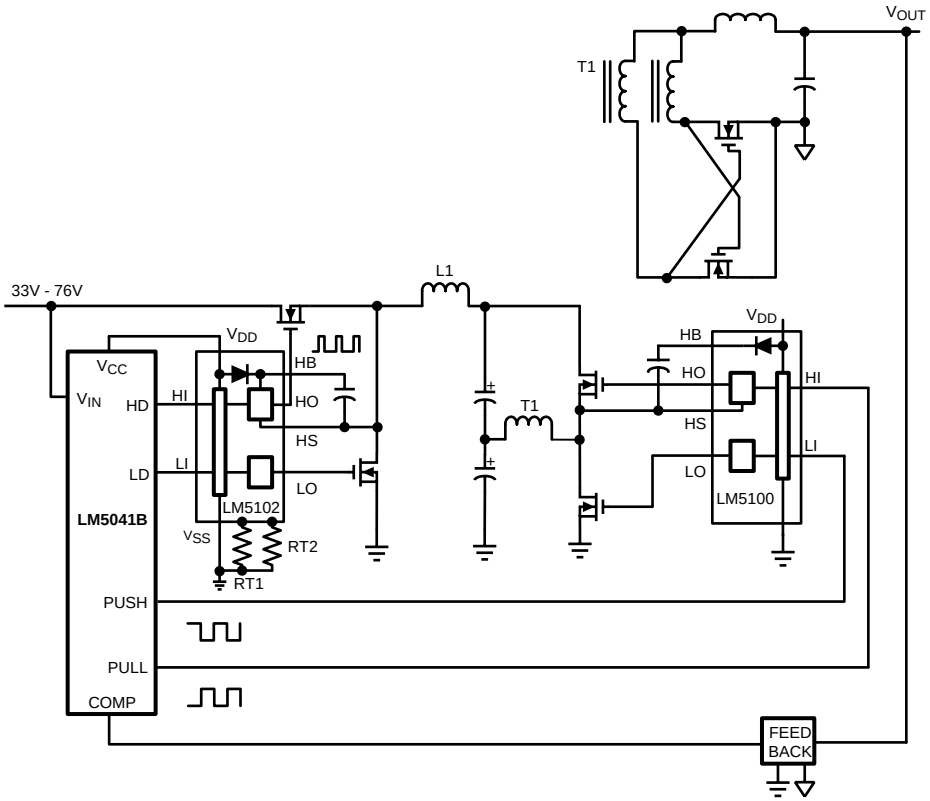
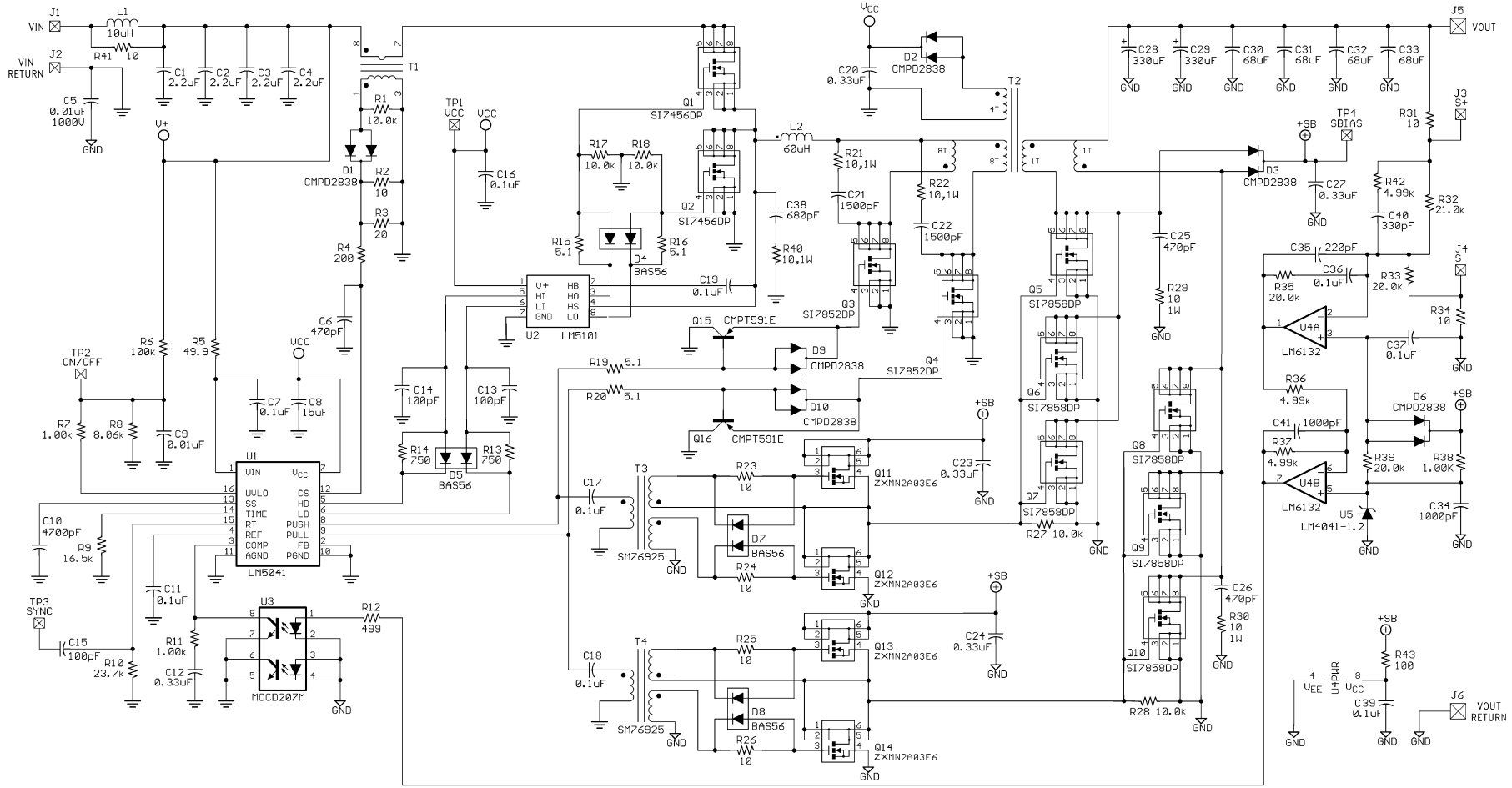


Figure 4. Simplified Cascaded Half-Bridge

Application Circuit: Input 35V to 80V, Output 2.5V, 50A



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5041BMTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5041B MTC	Samples
LM5041BMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5041B MTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

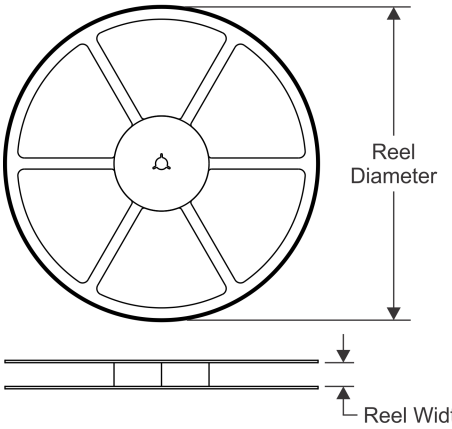
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

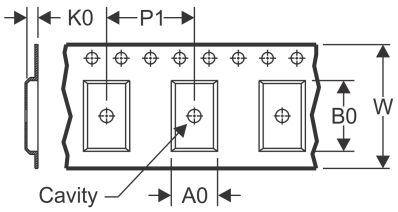
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

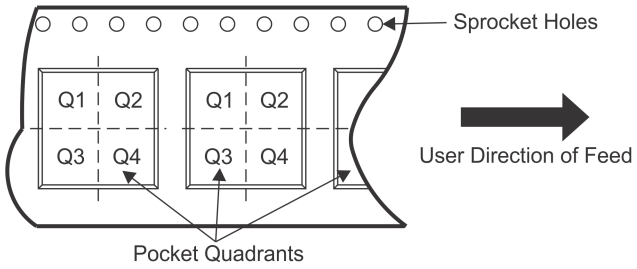


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

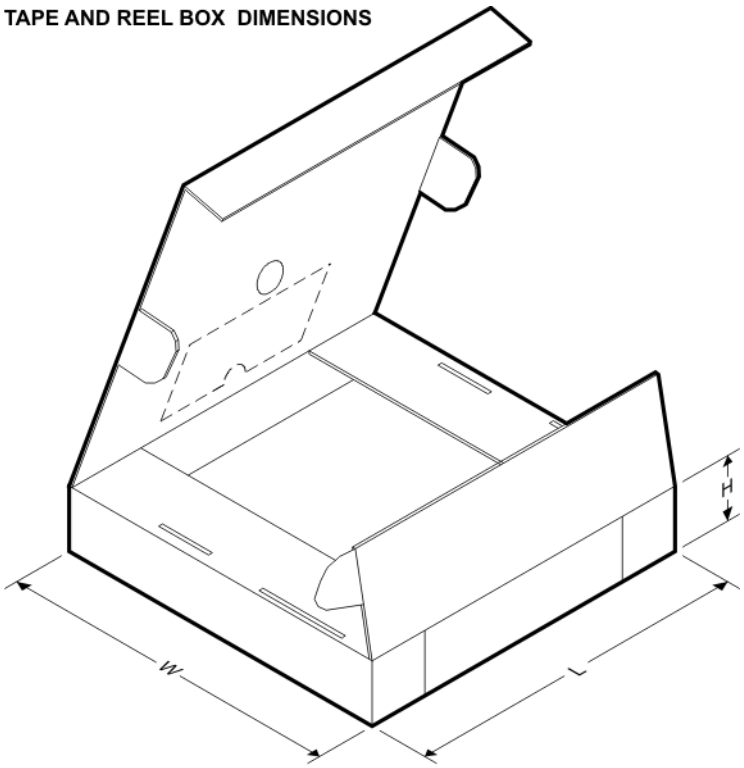
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5041BMTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

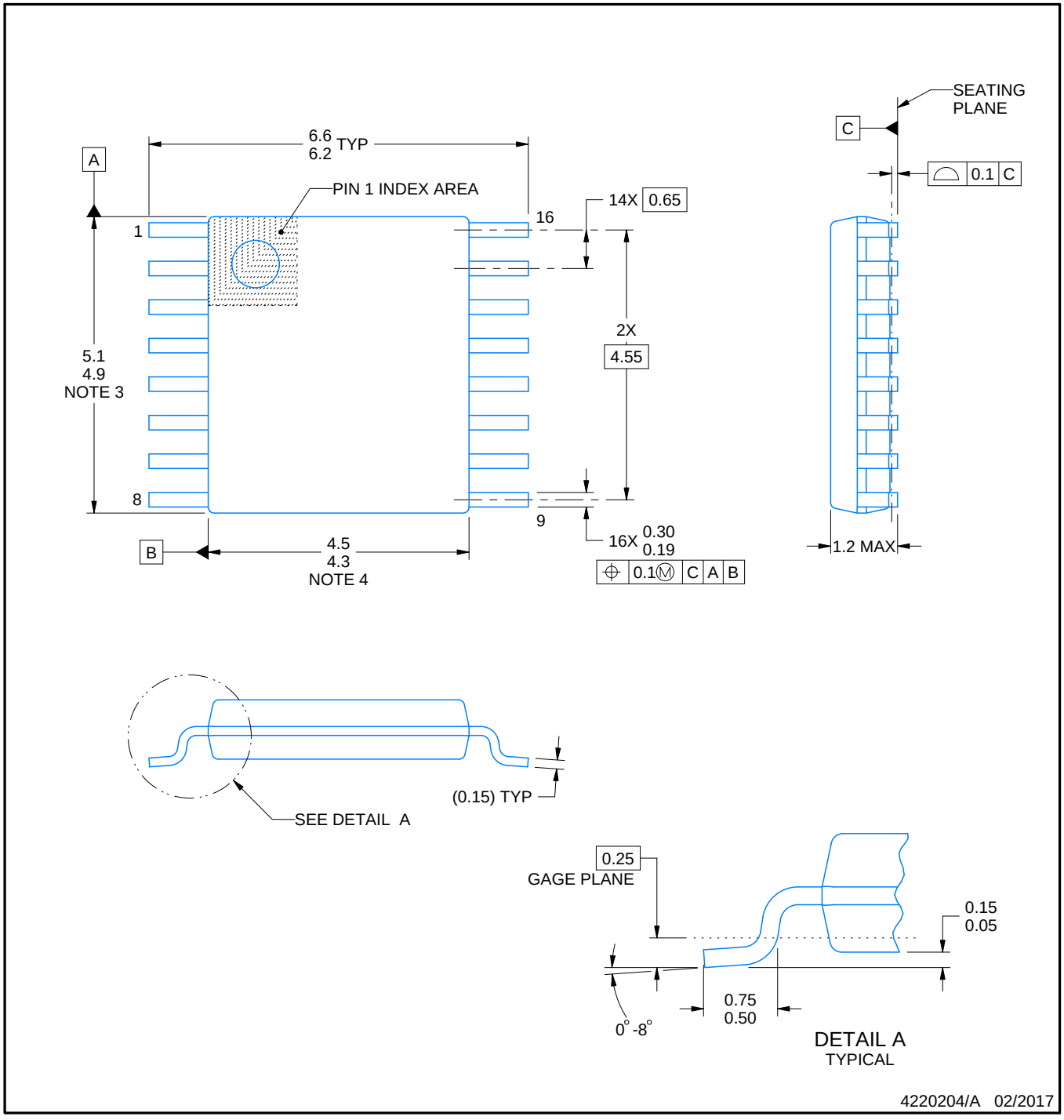
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5041BMTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

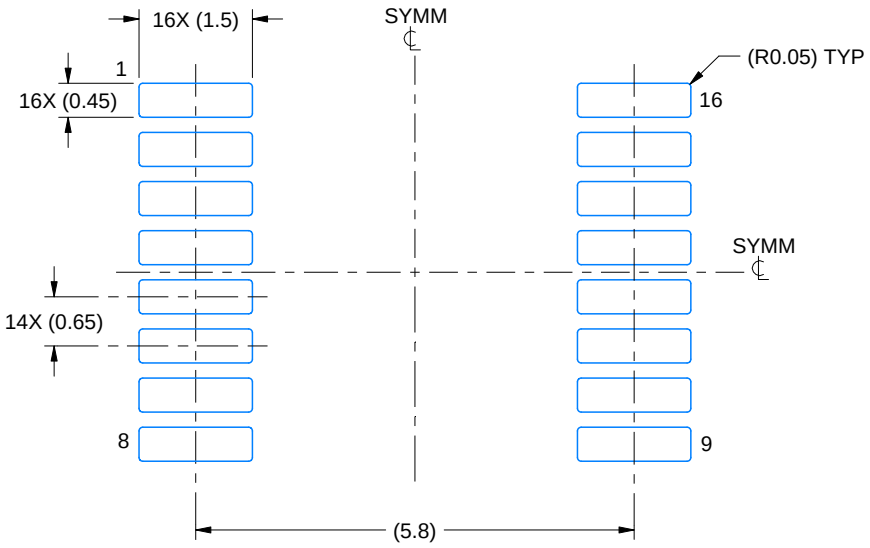
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

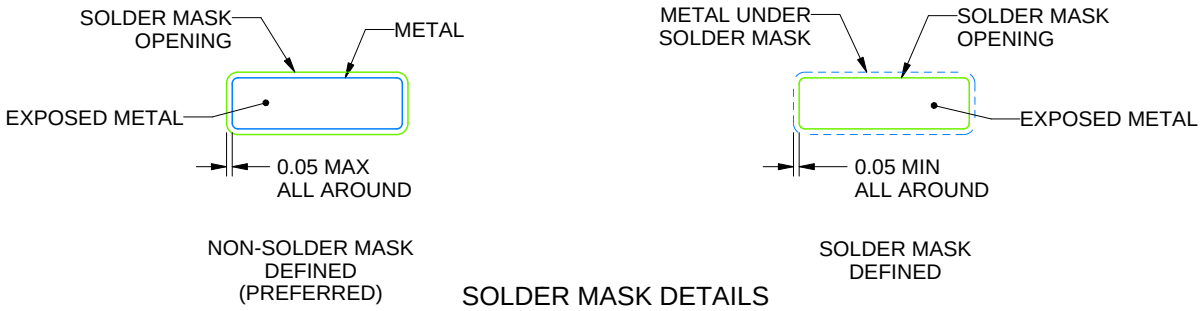


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

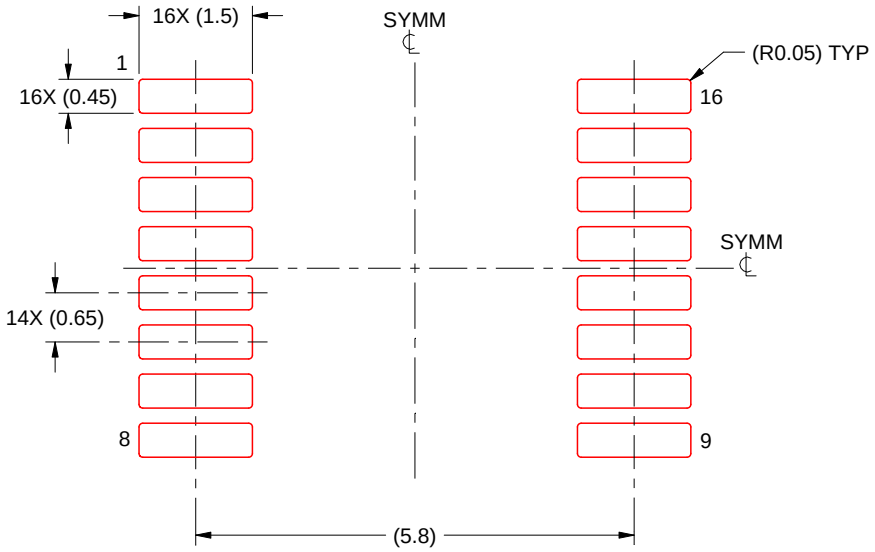


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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