LM5080 Modular Current Sharing Controller

Check for Samples: LM5080

FEATURES

- **Average Program Current Share Method**
- **Single-wire Star Link Current Share Bus**
- **No Precision External Resistors Necessary**
- **3V to 15V Bias Voltage Range**
- **Adaptable for High or Low Side Current Sensing**
- **Flexible Architecture Allows 4 Modes of Operation:**
  - **Negative Remote Sense Adjustment**
  - **Positive Remote Sense Adjustment**
  - **Trim or Reference Adjustment**
  - **Feedback Divider Adjustment**

PACKAGES

- **VSSOP-8**
- **RoHS compliant Pb free available**

DESCRIPTION

The LM5080 is a simple and cost effective load share controller that provides all functions required to balance the currents delivered from multiple power converters operated in parallel. The LM5080 implements an average program (AP) method of active load share control which adjusts the output voltage of individual power stages either up or down to deliver nearly equal currents to a common load. The average program method improves stability and reduces the output voltage tolerance when compared to other common load sharing methods. The LM5080 supports two common applications for load share controllers: external control in which the load share circuit balances currents between separate power modules (bricks), and internal control where the load share circuit is integrated into the voltage regulation loop of each power converter module or circuit.

LM5080 Typical Application

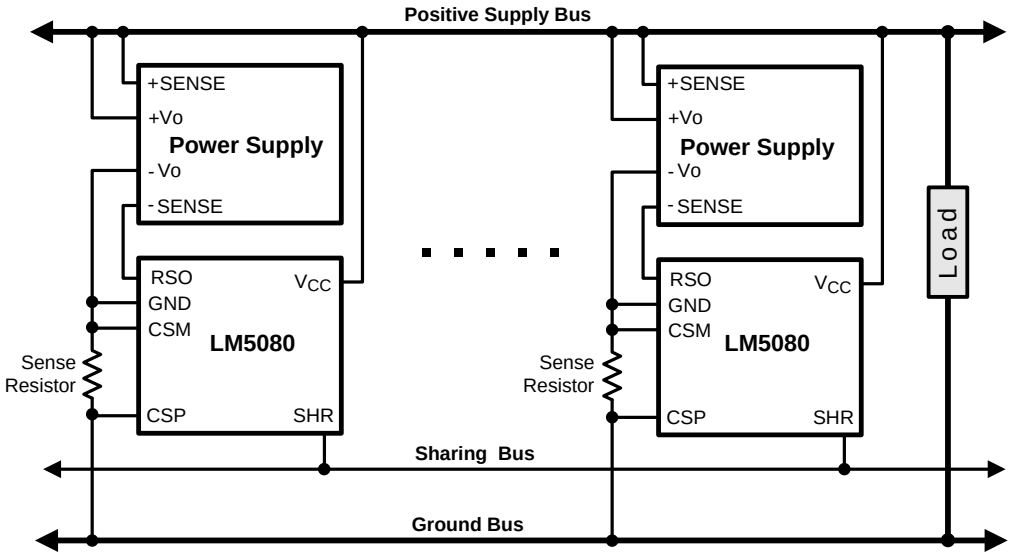


Figure 1. Remote Sense Adjust Mode

Connection Diagram

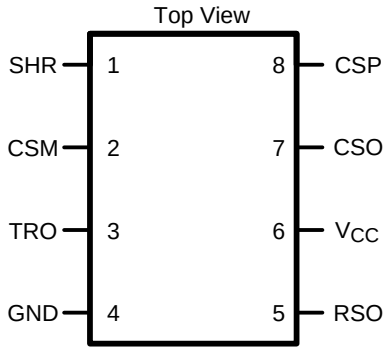


Figure 2. 8-Lead VSSOP
See Package Number DGK0008A

PIN DESCRIPTIONS

Pin	Name	Description
1	SHR	Current Share Bus. The SHR pins of each LM5080 device are connected together.
2	CSM	Current Sense Amplifier Minus Input.
3	TRO	Transconductance Output. One of two outputs of the current sense transconductance amplifier.
4	GND	Ground. Connect to negative terminal of the LM5080 bias supply.
5	RSO	Remote Sense Output. Capable of driving the low impedance remote sense pin of a power converter.
6	VCC	Bias Supply. VCC can be connected to the output of the power converter that the LM5080 controls if greater than 3V, or it can be connected to another bias source for lower voltage systems.
7	CSO	Current Sense Output. One of two outputs of the current sense transconductance amplifier.
8	CSP	Current Sense Amplifier Positive Input.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

V_{CC} to GND	-0.3V to 15V
RSO to GND (3)	-0.3V to 5V
All other pins to GND	-0.3V to 5V
ESD Rating (4) Human Body Model	2kV
Storage Temperature	-55°C to +150°C
Junction Temperature	150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Maximum recommended operating voltage not to exceed VCC - 2V or 5V, whichever is lower.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

OPERATING RATINGS(1)

VCC to GND	3V to 14 V
Operating Junction Temperature	-40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of –40°C to +125°C and are provided for reference only. Unless otherwise specified, the following conditions apply: CSM = 0, VCC = 5V, RSO unloaded.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ICC	VCC Quiescent Current	RSO shorted to CSO CSP = 50 mV CTRO = 10nF		3.7	**5.5**	mA
	CSP Input open circuit voltage ratio	Specified as a percentage of VCC	**19**	20	**21**	%
	CSP mode threshold ratio- Rising	Specified as a percentage of VCC	**8.5**	10.5	**12.5**	%
	CSP mode threshold ratio - Falling	Specified as a percentage of VCC	**7.0**	9.5	**11**	%
Current Share Amplifier						
VIO	Input Offset Voltage (RSO-CSP)	RSO shorted to CSO CSP = 50 mV CTRO = 10nF	-2.5 **-3.5**	0	2.5 **3.5**	mV
		RSO shorted to CSO CSP = 600 mV CTRO = 10nF, VCC = 3V	-1 **-2**	0	1 **2**	mV
CSM_{MAX}	Input Common Mode Voltage Range	CSP - CSM = 50 mV RSO shorted to CSO CSO-CSP < 1 mV CTRO = 10 nF		VCC-2V		V
CSM_{MIN}				0		V
GM_{TRO}	Current Share Amplifier Transconductance	GM_{TRO} = ΔITRO / ΔVSHR CTRO = 10 nF		8.7		mA/V
I_{TRO_SRC}	TRO sourcing current limit	TRO = 500 mV CSO open, CSP = 1.1V	**9**	11	**14**	µA
I_{TRO_SINK}	TRO sinking current limit	TRO = 500 mV CSO open, CSP=0.9V	**8.2**	11	**13.5**	µA
I_{TRO_OS}	TRO offset current	TRO = 750 mV CSP, CSO Open Circuit	**–1**	0	**1**	µA

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of –40°C to +125°C and are provided for reference only. Unless otherwise specified, the following conditions apply: CSM = 0, VCC = 5V, RSO unloaded.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TRO_MIN}	TRO Output Range	CSP, CSO, SHA open circuit ITRO_OS < 500 nA		450		mV
V_{TRO_MAX}				2.75		V
RSO Buffer						
VIO_{RSO}	RSO Buffer Input offset Voltage	Offset = TRO-RSO, TR0 = 750 mV CSO, CSP open circuit	**-4**	0	**4**	mV
I_{LIMSRC}	RSO source current limit		**18**	26	**35**	mA
I_{LIMSNK}	RSO sink current limit		**18**	26	**35**	mA
VOL_{RSO}	RSO output low voltage	CSP = 0V, Sinking 10 mA		12	**28**	mV
Thermal Resistance						
θ_{JA}	Junction to Ambient	VSSOP-8 Package		190		°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

I_{CC} vs V_{CC}

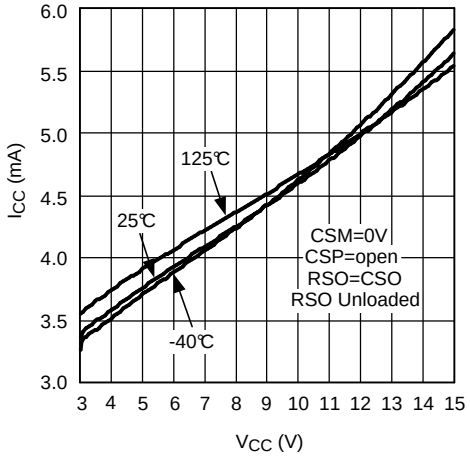


Figure 3.

Current Share Amplifier Transconductance vs VCC

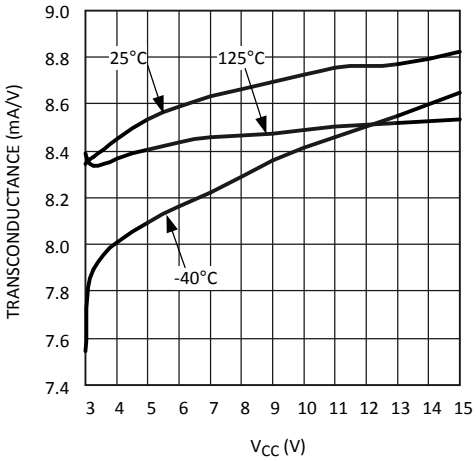


Figure 4.

RSO Sink Current Limit vs VCC

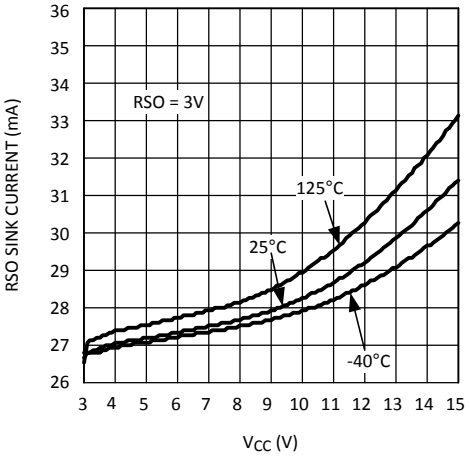


Figure 5.

RSO Source Current Limit vs VCC

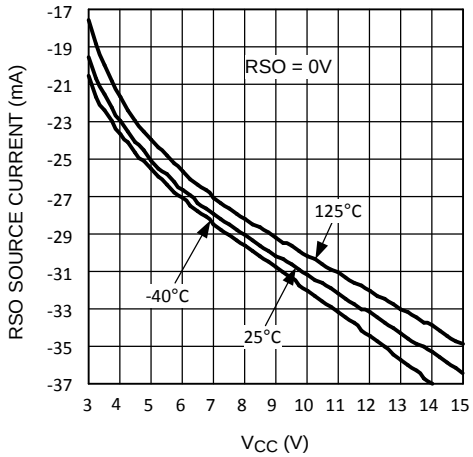


Figure 6.

RSO Buffer Input Offset Voltage vs VCC

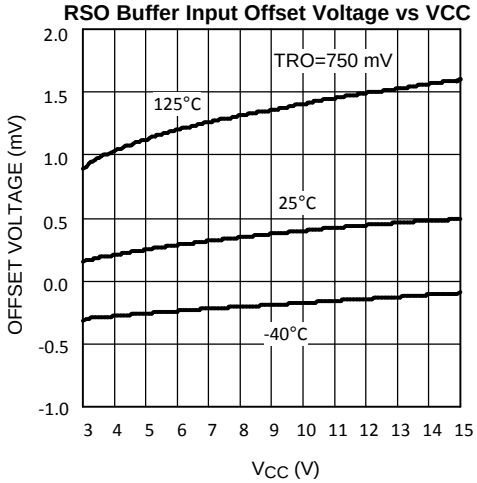


Figure 7.

RSO VOL vs VCC

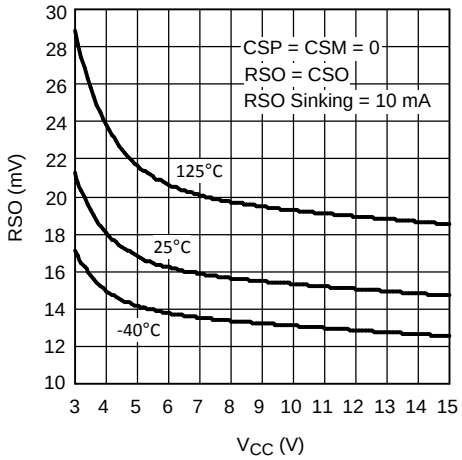


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TRO Current Limit vs VCC

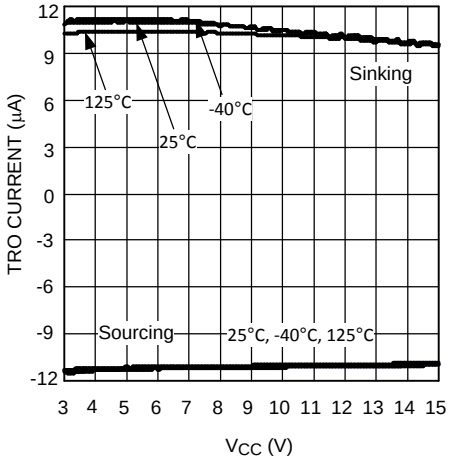


Figure 9.

TRO Offset Current vs TRO Voltage

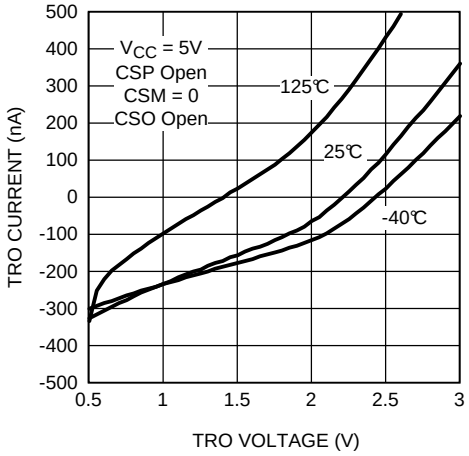


Figure 10.

CSP Input Open Circuit Voltage vs VCC

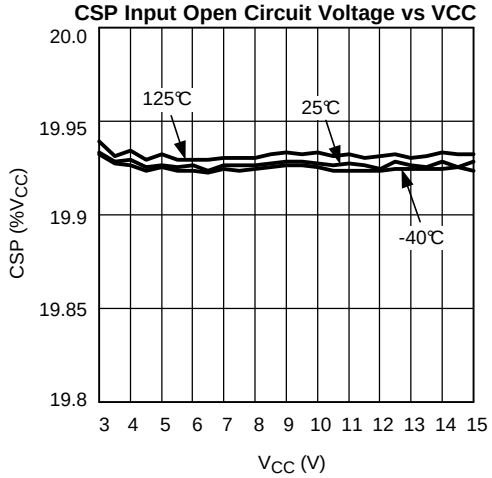


Figure 11.

CSP Mode Thresholds vs VCC

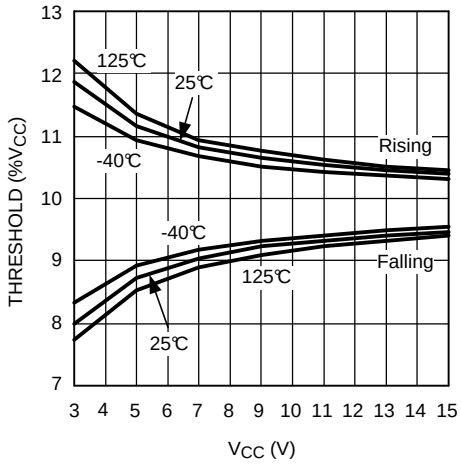
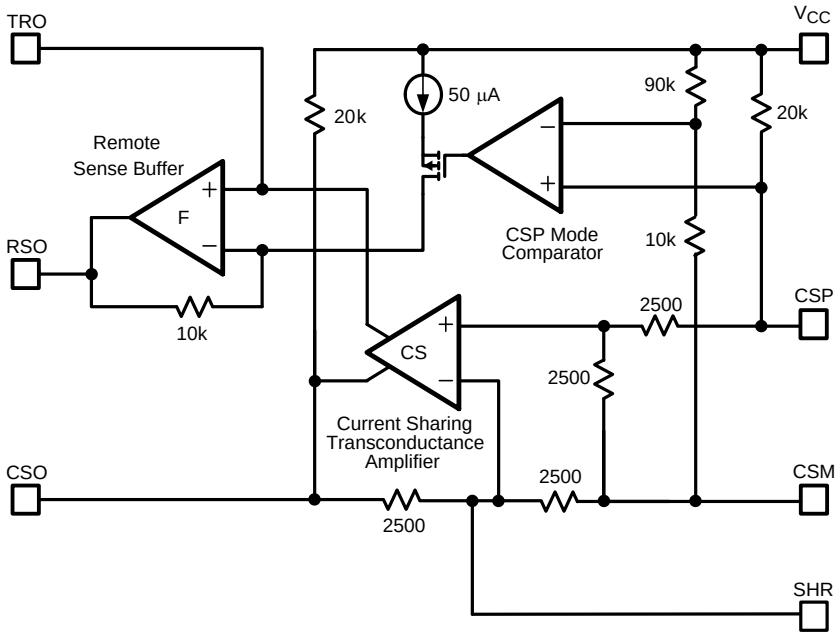


Figure 12.

BLOCK DIAGRAM



OPERATING DESCRIPTION

Identical regulators connected in parallel will theoretically share the total load current equally. However, slight mismatches in the reference voltage or feedback dividers of each regulator can cause significant imbalances in the load current sharing. The LM5080 senses the load current of each regulator with an external sense resistor and makes adjustments to the regulator's output voltage to achieve nearly equal current sharing. There are four possible implementations for the LM5080:

Reference Adjust Mode achieves current sharing by adjusting the regulator reference voltage by applying an error current from the TRO transconductance amplifier to the trim or adjust pin of the regulator.

Remote Sense Positive Mode achieves current sharing by adjusting the positive remote sense pin of the power converter with current supplied by the RSO buffer amplifier output.

Remote Sense Negative Mode achieves current sharing by adjusting the negative remote sense pin of the power converter with current supplied by the RSO buffer amplifier output.

Feedback Adjust Mode achieves current sharing by adjusting the regulator feedback voltage by applying an error current from the TRO transconductance amplifier to the feedback resistor divider.

In each mode, the LM5080 combines the regulator's load current information with the total load information on the share (SHR) bus to create an error current on the TRO output which is proportional to the load current mismatch. In the reference adjust or feedback adjust modes of operation, the output of the current share amplifier (CSA) is fed directly into the regulator reference or feedback divider. The RSO buffer can optionally be used to boost the transconductance of the CSA if needed. In the remote sense adjust modes, the RSO and CSO pins are tied together which reconfigures the CSA as a voltage error amplifier where the RSO buffer drives the remote sense pins of the regulator directly.

CURRENT SHARE AMPLIFIER

The current share amplifier is a low input offset transconductance amplifier with inputs CSP and CSM and dual outputs, TRO and CSO. The two outputs are identical except TRO is current limited to approximately ±10 µA in order to limit the maximum correction of the regulator reference in the trim adjust and feedback adjust modes. The outputs can operate down to 450 mV without saturating which allows the TRO output to adjust reference voltages as low as 500 mV. A capacitor from TRO to ground (CTRO) is used for frequency compensation of the current share loop.

In the two remote sense adjust modes, the current share amplifier is configured as a unity gain differential voltage amplifier by tying RSO to CSO. A capacitor from TRO to ground (CTRO) is used for frequency compensation of the amplifier and the current share loop.

RSO BUFFER

The RSO buffer is a low-offset unity-gain operational amplifier that has different uses, depending on the mode of operation. In the remote sense adjust modes, the RSO pin is externally tied to the CSO pin to create a differential voltage amplifier that can drive the 10Ω input impedance of the remote sense pin of typical power converter modules. The RSO buffer can source or sink 10mA at an output voltage as low as 20mV above ground. With RSO load resistors of 10Ω, the buffer can drive up to 10nF without causing amplifier instability. For RSO loads > 1 kΩ, max load capacitance on this node is 500pF for stable operation. In the trim adjust and feedback adjust modes, the RSO buffer can be configured with external resistors to boost the CSA transconductance which increases the current share loop gain.

CSP MODE COMPARATOR

The LM5080 monitors CSP & CSM with the CSP mode comparator and applies a 500 mV input offset on the RSO buffer amplifier if CSP-CSM is less than 10% of VCC (which indicates a remote sense application mode). This offset allows the RSO output to swing within 10 mV of ground without saturating the TRO output which drives the RSO buffer. In the trim adjust and feedback adjust modes, the CSP pin is left open. In this configuration CSP is internally biased such that CSP - CSM = 0.2 x VCC resulting in the removal of the 500mV RSO buffer offset.

REFERENCE ADJUSTMENT OPERATION MODE

The reference adjust or trim adjust mode configuration is shown in Figure 13. Typically only the current share amplifier is used, however the RSO buffer can be optionally configured for boosting the transconductance to increase the current share loop gain (Figure 14). CSP is left open and CSM is connected to a low side current sense resistor. The TRO output is connected to the TRIM pin of the power converter to inject a correction that adjusts the voltage regulator.

To understand the control loop, assume for a moment the SHR pin is disconnected from the share bus. Since both inputs to the current share amplifier are equal, the TRO output current (IT) is zero and independent of the sense resistor voltage (VRS). Hence the voltage regulation loop of each converter is unaffected by the LM5080 when the SHR bus is open. When the SHR pins are connected in a 2 supply system, the transfer function between the sense resistor voltages (VRS1 & VRS2) and the current injected into each power converter TRIM pin (IT1 & IT2) are as follows:

$$IT1 = 0.9 \times gm \times (VRS1 - VRS2)$$

$$IT2 = 0.9 \times gm \times (VRS2 - VRS1)$$

where

- gm = current share amplifier transconductance (8.7mA/V)

As long as the current sharing is equal (VRS1=VRS2), the correction to the references (IT1 & IT2) will remain unchanged. However, any difference between VRS1 and VRS2 will drive the TRIM pin currents in opposite polarities. As a result the power converter output voltages will be adjusted to force VRS1=VRS2. For 3 or more channels, the same averaging concept is true; the injected currents (IT) will drive the references such that the sense voltages are nearly identical.

A capacitor from TRO to ground (CTRO) sets the dominant pole of the current share loop. The pole location is determined by gm, CTRO and the impedance of the regulator trim pin. The current share loop frequency response does not need to be fast and in fact should be less than or equal to 1/10th the regulator bandwidth. Since similar regulators will have similar transient responses to a load step, the LM5080 only needs to correct the differences in each regulator's voltage reference and feedback divider which do not require a fast response. In some systems a small resistor (RTRO) in series with CTRO can improve stability by introducing a zero at high frequencies to increase the phase margin of the current share loop.

It is essential that the VCC pins of all LM5080's be tied to the same point in this mode. Any mismatch in the VCC voltages between LM5080's will significantly contribute to current share errors. The current sense resistors should be located as close to the load as possible to minimize trace resistance in series with the sense resistors which can also contribute to sharing errors. In this mode, the best accuracy will be achieved with lower VCC values since any mismatch in the gain resistors internal to the LM5080 will affect the current share accuracy.

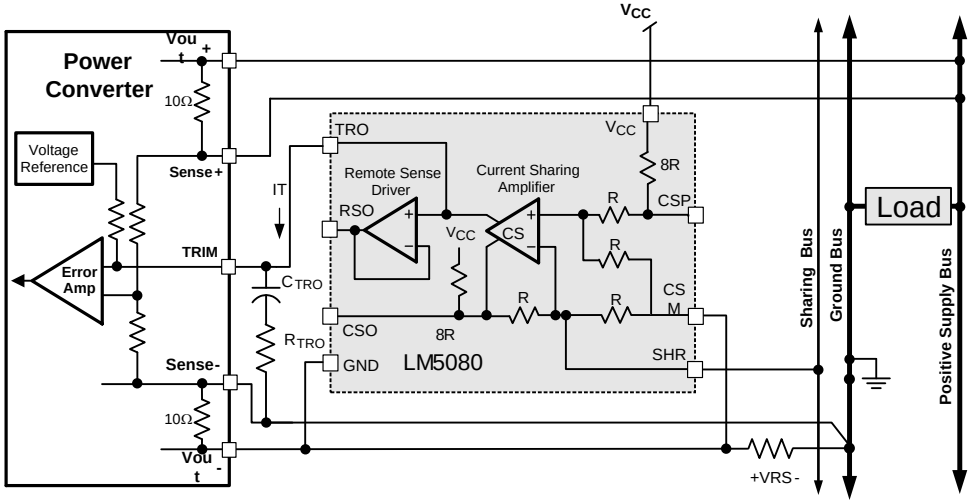


Figure 13. Reference Adjust Mode Implementation

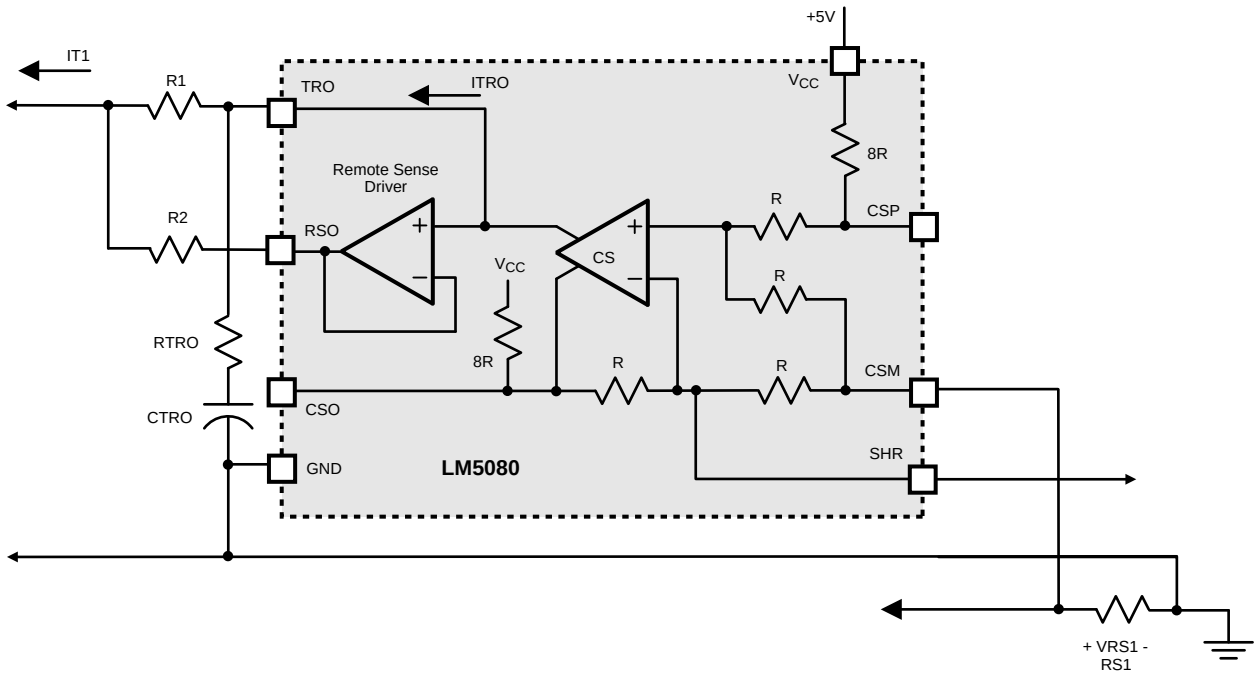


Figure 14. LM5080 Showing the RSO Buffer Configured to Boost Transconductance

The effective output current from the TRO pin can be multiplied to increase the current share loop gain if necessary. R1 should be at least 10kΩ.

$$IT1 = ITRO \times \left(1 + \frac{R1}{R2}\right)$$

REMOTE SENSE ADJUST MODES

The two remote sense adjust modes (positive and negative) achieve current sharing by controlling either remote sense input of the power converter. These configurations for the LM5080 are shown in Figure 15 and Figure 16. To understand the sharing mechanism, assume for a moment the SHR pin is disconnected from the share bus. Connecting RSO and CSO configures the current sharing amplifier as a differential amplifier with a gain of one. The CSP and RSO voltage will be identical and independent of the voltage across the sense resistor. Hence the voltage regulation loop of each power converter is unaffected by the LM5080 when the SHR bus is open.

When the SHR pins are connected, the small signal transfer functions between the sense resistor voltages (VRS) and the power supplies negative remote sense voltages (VSNS) are:

$$VSNS1 = A/4 \times (VRS1 - VRS2)$$

$$VSNS2 = A/4 \times (VRS2 - VRS1)$$

where

- $A = \dfrac{Gm \times Ro}{(j\omega \times Ro \times C_{TRO} + 1)}$
- gm = current share amplifier transconductance (8.7mA/V)
- Ro = output impedance of TRO pin (typically 6 MΩ)

Provided the current sharing is equal (VRS1=VRS2), the VSNS voltages will remain unchanged. However, any difference between VRS1 and VRS2 will drive the VSNS1 and VSNS2 voltages in opposite polarities. As a result the power converter output voltages will be adjusted to force VRS1=VRS2.

A capacitor from TRO to ground will compensate the differential amplifier as well as set the dominant pole of the current share loop. CTRO should be at least 2 nF to insure stability of the differential amplifier. In some systems a small resistor (RTRO) in series with CTRO will improve stability of the current share loop by introducing a zero at high frequencies.

In the remote sense modes, it is essential the CSP pins of all LM5080's be tied to the exact same location on the PC board. Any mismatch in the CSP voltages between LM5080's will contribute to current share errors. As in the reference adjust mode, the current sense resistors should be located as close to the load as possible to minimize trace resistance in series with the sense resistors. In the remote sense positive mode, VCC must be biased at least 2V higher than the output regulation voltage to maintain CSP and CSM in the proper common mode range.

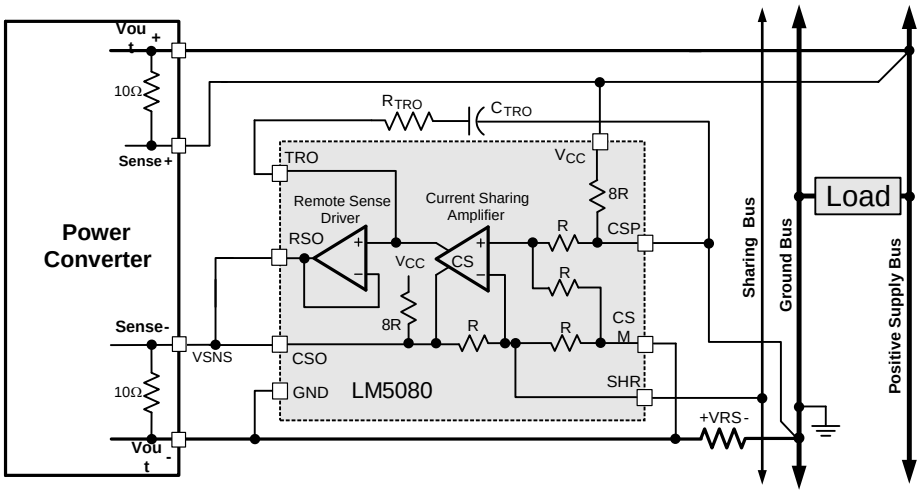


Figure 15. Remote Sense Negative Mode Implementation

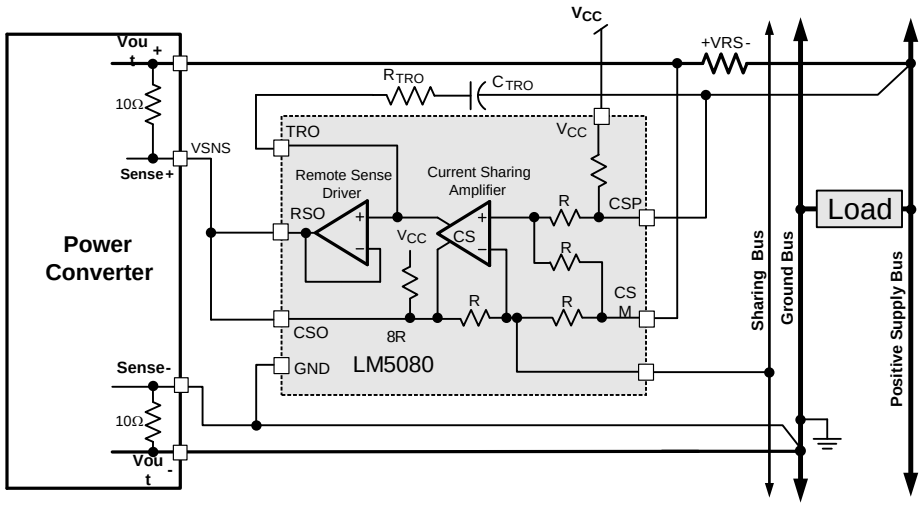


Figure 16. Remote Sense Positive Mode Implementation

FEEDBACK ADJUSTMENT MODE

The feedback adjust mode configuration is shown in Figure 17. It is very similar to the reference adjust mode except the current sensing is done on the high side of the load and the correction is applied to the feedback resistor divider in the voltage regulation loop.

Similar to the reference adjust mode, the transfer functions between the sense resistor voltages (VRS) and the currents injected into the power converter TRIM pin (IT) are:

IT1 = 0.9 x gm x (VRS1 - VRS2)

IT2 = 0.9 x gm x (VRS2 - VRS1)

where

- gm = current share amplifier transconductance (8.7mA/V)

As previously described, provided the current sharing is equal (VRS1=VRS2), the correction current to the reference (IT) will be zero. However, any difference between VRS1 and VRS2 will drive the TRIM pin currents in opposite polarities. As a result the power converter output voltages will be adjusted to force VRS1=VRS2.

In this mode, VCC must be biased at least 2V higher than the output regulation voltage to maintain CSP and CSM in the proper common mode range. It is essential the VCC pins of all LM5080's be tied to the same point in this mode. Any mismatch in the VCC voltages between LM5080's will contribute to current share errors. For the same reasons as discussed in the above two operating modes, the current sense resistors should be located as close to the load as possible. In this mode, the best accuracy will be achieved with lower VCC values since any mismatch in the gain resistors internal to the LM5080 will affect the current share accuracy.

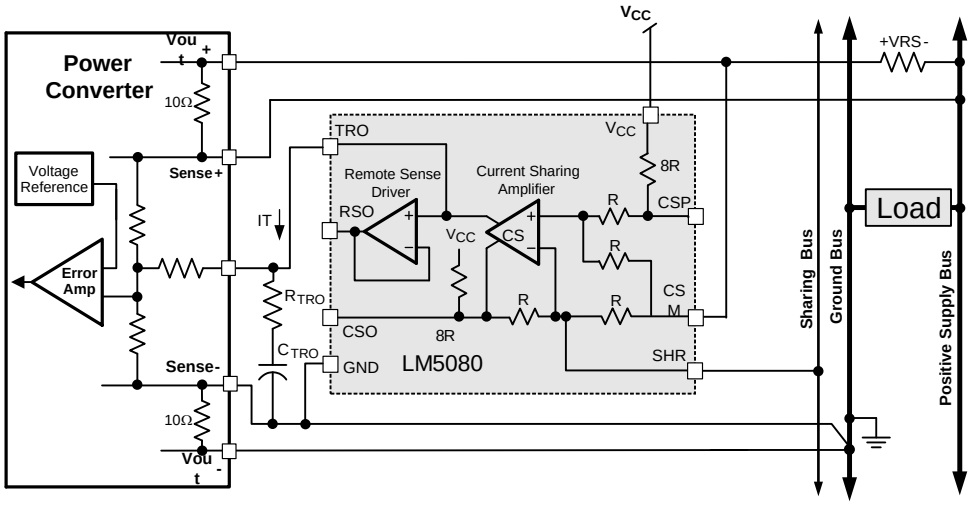


Figure 17. Feedback Adjust Mode Implementation

VOLTAGE MARGINING

Shifting the output regulation voltage up or down by a small amount is referred to as voltage margining. In the remote sense adjust modes and the feedback adjust modes, this can be done by connecting all of the power converter TRIM pins together and injecting a positive or negative current. However, in the reference adjust mode, the TRIM pin is used for current sharing. An alternative margining method is to inject a current into the SHR share bus. This will simultaneously shift the regulation voltages of all power converter's while maintaining equal current sharing. The injected current is split equally between the LM5080's SHR inputs and added to the TRIM pin currents creating an equal offset voltage for all of the power converter references. The trim pin current injected into each power converter's reference (IT) is dependent on the magnitude of the total injected current into the SHR bus (ISHR), the number of LM5080's on the SHR bus (N) and any transconductance boost supplied (R1 & R2):

$$IT1 = I_{SHR} \times \left(\frac{22.5}{21 \times N} \right) \times \left(1 + \frac{R1}{R2} \right)$$

An alternate method to shift the regulation voltage is to tie all the CSP pins together and inject a current into that node. The trim pin current injected into each power converter's reference (IT) attributed to the current injected into the CSP node (ICSP) is derived to be:

$$IT1 = I_{CSP} \times \left(\frac{20}{21 \times N} \right) \times \left(1 + \frac{R1}{R2} \right)$$

Figure 18 shows a margining up and down application implemented using pull up resistors to VCC. Since the SHR and CSP voltages are approximately 0.1 x VCC and 0.2 x VCC respectively, the injected current can be independently controlled with RM1 and RM2.

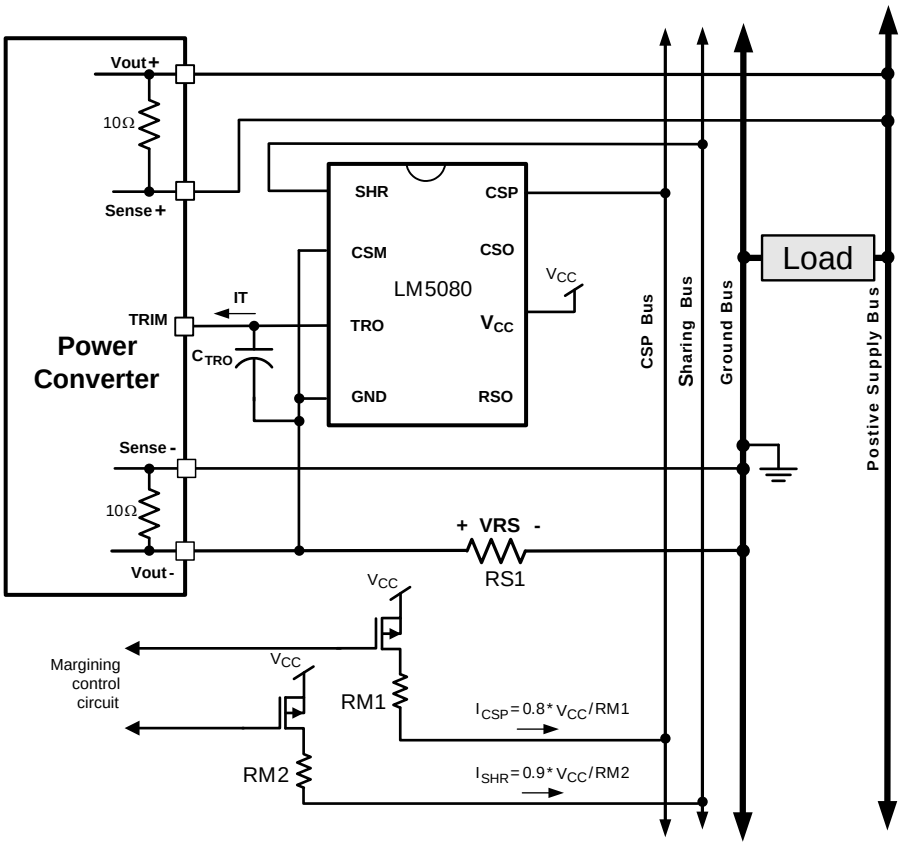


Figure 18. One Method of Implementing Voltage Margining

GENERAL DESIGN PROCEDURE

1. Select an appropriate sense resistor value. More sense voltage will result in better load sharing but more efficiency loss. Sense voltages of 50mV or more are recommended. In addition, the sense voltage at full load should be less than 5% of VCC in applications that control the remote sense terminals of the power supply.
2. For the reference adjust and feedback adjust modes, determine if transconductance (gm) boosting is required. Boosting the transconductance also boosts the TRO pin current limit. The TRO pin current limit (approximately 10µA typical) multiplied by the reference impedance determines the maximum correction the LM5080 can make to the reference. The LM5080 must have enough TRO current to adjust the converter output voltage by at least the accuracy of the reference. For example, if the reference accuracy is ±2%, the LM5080 must have the ability to adjust the reference by at least 2% (in the event one converter is 2% high and the other 2% low).
3. Compensate the current share loop by selecting an appropriate capacitance for CTRO. The compensation of the current share loop is dependent on the frequency response of the output voltage to the controlling node of the converter (TRIM pin, feedback divider or remote sense pins). Given the wide variety of converter designs and the many operating modes of the LM5080, selection of CTRO is best accomplished using a simple iterative procedure. Start with a large capacitance in TRO (100µF or more). While monitoring the load current in each converter with a current probe, determine the minimum CTRO required for stability by decreasing CTRO until the current sharing becomes unstable under step loads. The step loads should be more than 50% of the load range and applied at a frequency well below the cross over frequency of the converter. The TRO capacitance can be further reduced by introducing some resistance (RTRO) in series with CTRO to cancel the 2nd order poles within the converter.
4. If RTRO > 100 Ω in either remote sense mode, a second CTRO capacitor (~ 2nF) should be added between TRO and CSP to keep the error amplifier stable.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5080MM/NOPB	LIFEBUY	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SHUB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

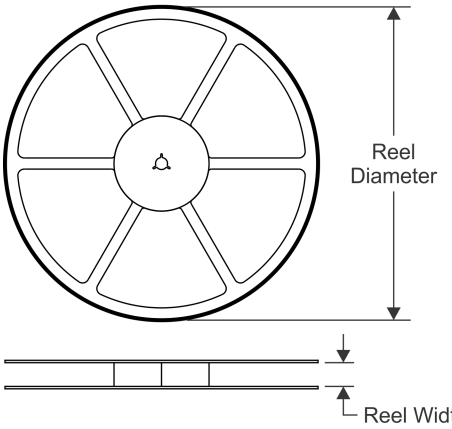
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

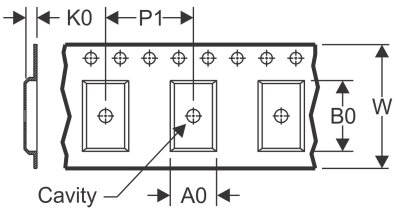
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

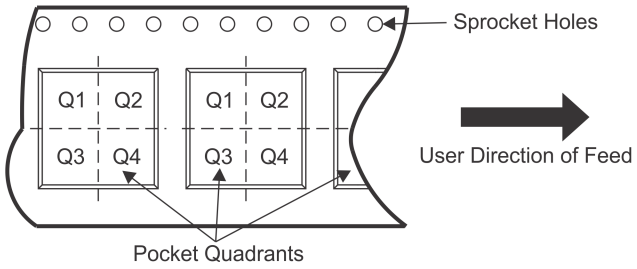


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

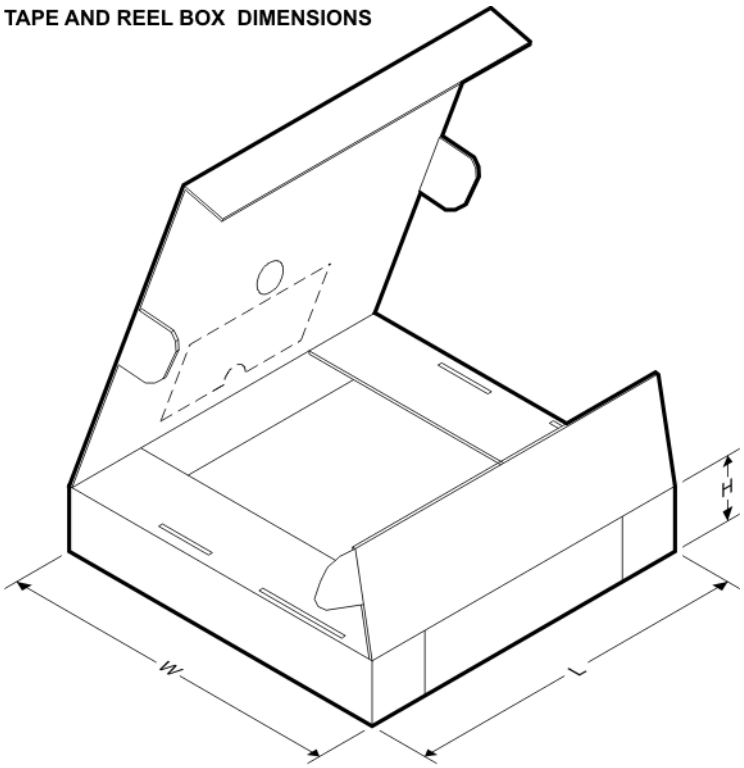
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5080MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

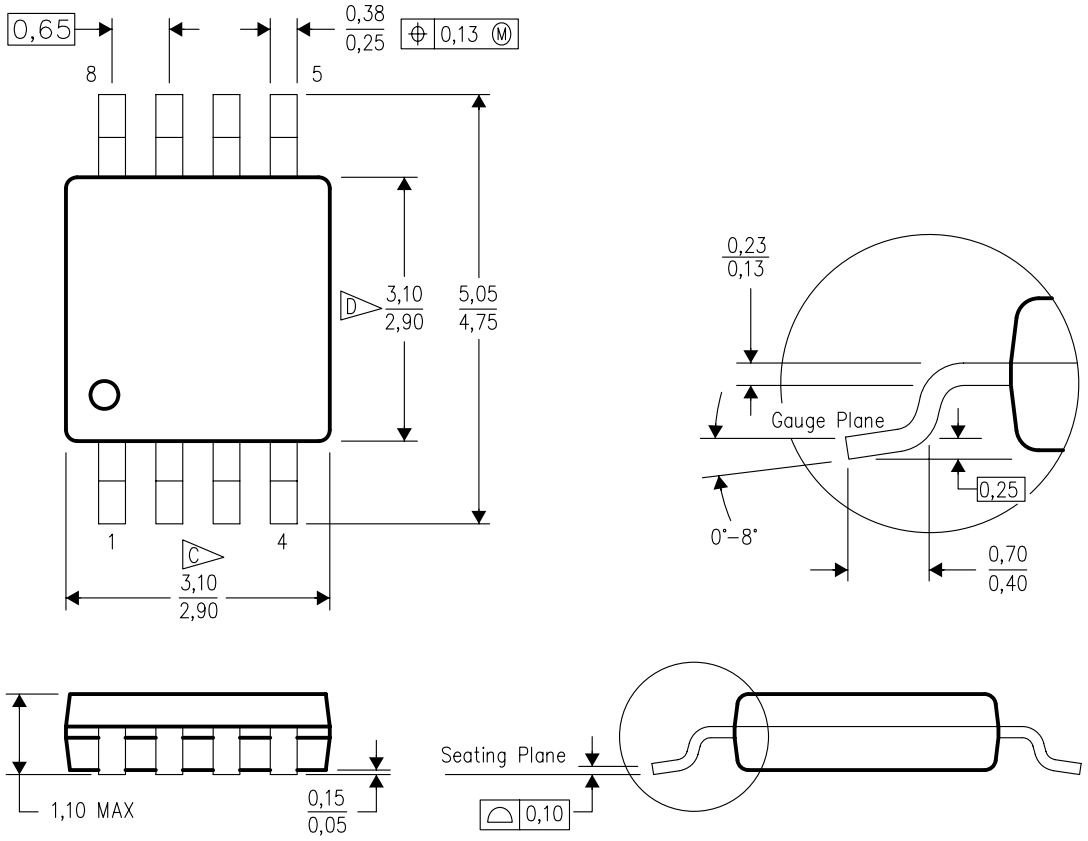
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5080MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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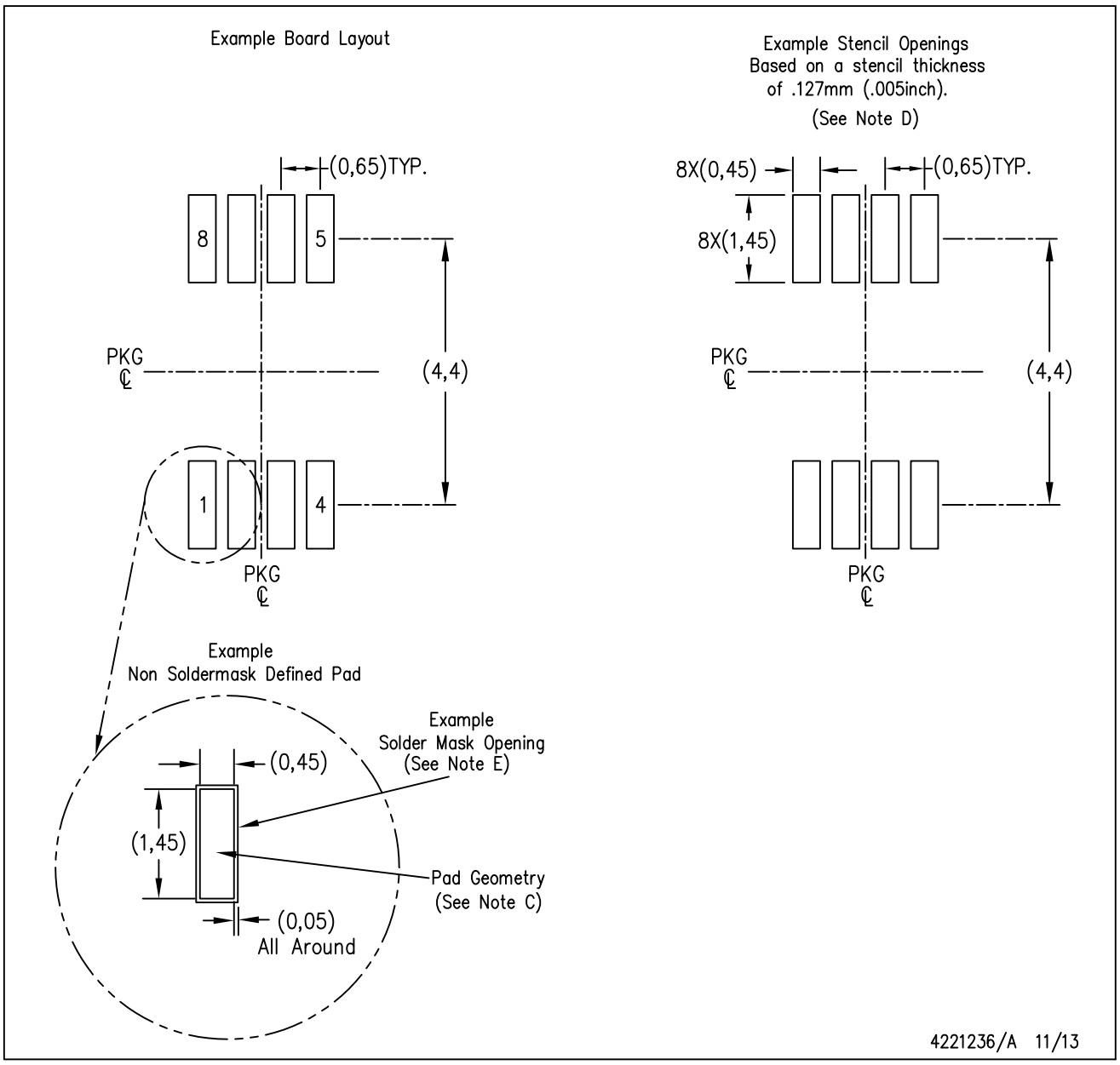
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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