Line Drivers/Receivers

LM55109/LM75109, LM55110/LM75110 dual line drivers

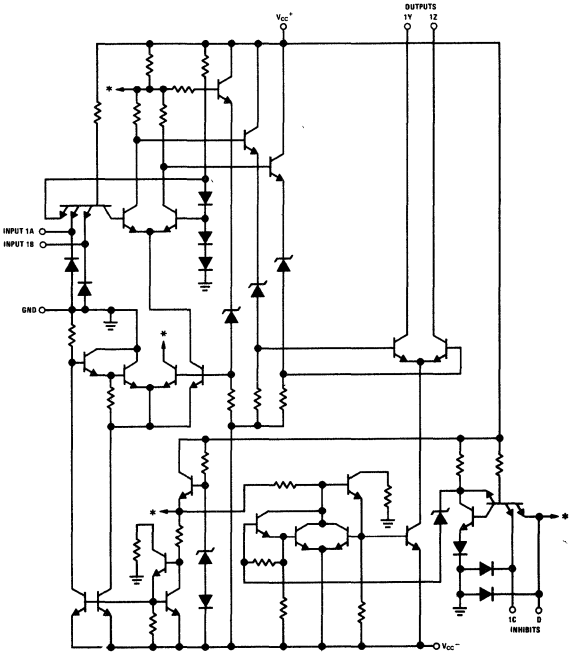
general description

These products are TTL compatible high speed differential line drivers intended for use in terminated twisted-pair party-line data transmission systems. They may also be used for level shifting since output common-mode range is −3V to +10V. An internal current sink is switched to either output dependent on input logic conditions. The current sink may be turned off by appropriate inhibit input conditions.

features

- Tightly controlled output currents over temperature, V_{CC}, and common-mode variations
- High speed 15 ns max
- Wide output common-mode range
- High output impedance
- Inhibits for party-line applications
- Current sink outputs 6 or 12 mA
- Dual circuits
- Standard supply voltages ±5V
- Input clamp diodes
- 14 pin cavity or molded DIP

schematic diagram

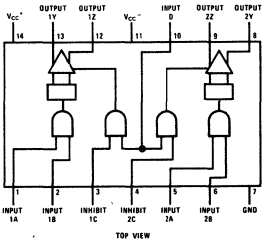


Note 1. 1/2 of the dual circuit shown

Note 2: *Indicates connections common to second half of circuit.

connection diagram

Dual-In-Line Package

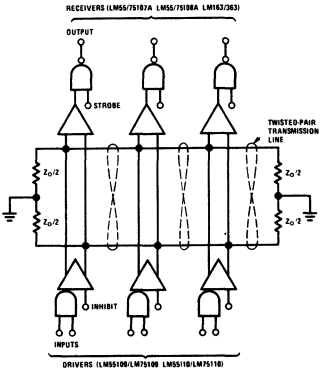


Order Number LM55109J, LM55110J, LM75109J, or LM75110J
See Package 16

Order Number LM75109N or LM75110N
See Package 22

typical application

Party-Line Data Transmission System



absolute maximum ratings

Supply Voltage, V_{CC}^+	7V
Supply Voltage, V_{CC}^-	−7V
Logic and Inhibitor Input Voltages	5 5V
Common-mode Output Voltage	−5V to 12V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
LM55109, LM55110	4.5	5.5	V
LM75109, LM75110	4.75	5.25	V
Temperature (T_A)			
LM55109, LM55110	−55	+125	°C
LM75109, LM75110	0	+70	°C

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55109/LM75109			LM55110/LM75110			
		MIN	TYP	MAX	MIN	TYP	MAX	
Positive Common Mode Output Voltage		0		10	0		10	V
Negative Common Mode Output Voltage		0		−3	0		−3	V
High Level Input Current Into 1A, 1B, 2A or 2B ($I_{IH(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(L)}$ = 2 4V			40			40	µA
High Level Input Current Into 1A, 1B, 2A or 2B ($I_{IH(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(L)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1A, 1B, 2A or 2B ($I_{IL(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(L)}$ = 0 4V			−3			−3	mA
High Level Input Current Into 1C or 2C ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = 2 4V			40			40	µA
High Level Input Current Into 1C or 2C ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1C or 2C ($I_{IL(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(I)}$ = 0 4V			−3			−3	mA
High Level Input Current Into D ($I_{IH(I)}$)	V_{CC}^+ = Max V_{CC}^- = Max, $V_{IH(I)}$ = 2 4V			80			80	µA
High Level Input Current Into D ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into D ($I_{IL(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(I)}$ = 0 4V			−6			−6	mA
On State Output Current ($I_{O(ON)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{CC}^+ = Min, V_{CC}^- = Max	3 5		7	6 5		15	mA mA
Off State Output Current ($I_{O(OFF)}$)	V_{CC}^+ = Min, V_{CC}^- = Min			100			100	µA
Supply Current From V_{CC}^+ With Driver Enabled ($I_{CC^+(ON)}$)	$V_{IL(L)}$ = 0 4V, $V_{IH(I)}$ = 2V		18	30		23	35	mA
Supply Current From V_{CC}^- With Driver Enabled ($I_{CC^-(ON)}$)	$V_{IL(L)}$ = 0.4V, $V_{IH(I)}$ = 2V		−18	−30		−34	−50	mA
Supply Current From V_{CC}^+ With Driver Inhibited ($I_{CC^+(OFF)}$)	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0 4V		18			21		mA
Supply Current From V_{CC}^- With Driver Inhibited ($I_{CC^-(OFF)}$)	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0 4V		−10			−17		mA
Input Clamp Voltage on Inputs or Inhibits (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5		−1	−1 5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = 5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55109/LM75109			LM55110/LM75110			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Logic Input A or B to Output Y or Z ($t_{PLH(L)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		9	15		9	15	ns
Propagation Delay Time, High to Low Level, From Logic Input A or B to Output Y or Z ($t_{PHL(L)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		9	15		9	15	ns
Propagation Delay Time, Low to High Level, From Inhibitor Input C or D to Output Y or Z ($t_{PLH(I)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		16	25		16	25	ns
Propagation Delay Time, High to Low Level, From Inhibitor Input C or D to Output Y or Z ($t_{PHL(I)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		13	25		13	25	ns