Memory/Clock Drivers

LM55325/LM75325 memory drivers general description

The LM55325 and LM75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs These circuits are designed for use with magnetic memories

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2} This protects the outputs from voltage surges associated with switching inductive loads

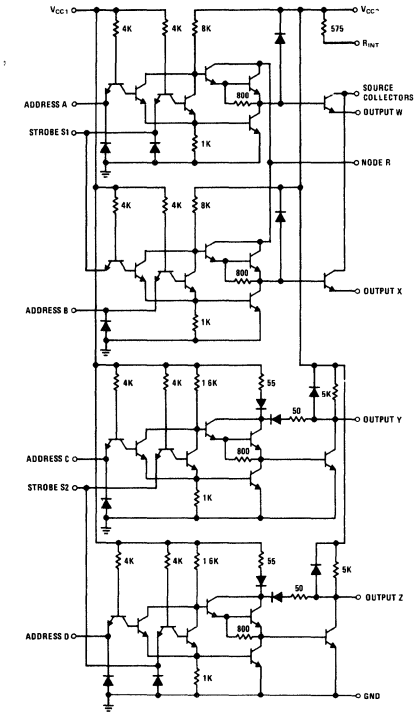
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V

The LM55325 operates over the full military temperature range of -55°C to +125°C, while the LM75325 operates from 0°C to +70°C

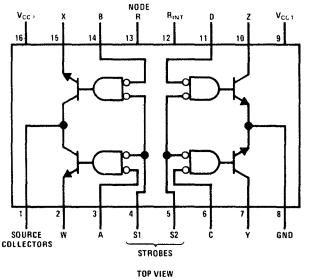
features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package



Order Number LM55325J or LM75325J
See Package 17

Order Number LM75325N
See Package 23

truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE Not more than one output is to be on at any one time

absolute maximum ratings

Supply Voltage V_{CC1} (Note 1)		7V
Supply Voltage V_{CC2} (Note 1)		25V
Input Voltage (Any Address or Strobe Input)		5.5V
Continuous Total Dissipation at (or Below) +70°C Free-Air Temperature (Note 2)		800 mW
Operating Temperature Range	LM55325	−55°C to +125°C
	LM75325	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55325			LM75325			
		MIN	TYP*	MAX	MIN	TYP*	MAX	
High Level Input Voltage (V_{IH})	Figure 1 and 2	2			2			V
Low Level Input Voltage (V_{IL})	Figure 3 and 4			0.8			0.8	V
Input Clamp Voltage (V_I)	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C, Figure 5		−1.3	−1.7		−1.3	−1.7	V
Source Collectors Terminal Off State Current (I_{OFF})	V_{CC1} = 4.5V, V_{CC2} = 24V, Full Range, Figure 1			500			200	μA
Source Collectors Terminal Off State Current (I_{OFF})	V_{CC1} = 4.5V, V_{CC2} = 24V, T_A = 25°C, Figure 1		3	150		3	200	μA
High Level Sink Output Voltage (V_{OH})	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0V, Figure 2	19	23		19	23		V
Saturation Voltage Source Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, Full Range, (Note 3) Figure 3			0.9			0.9	V
Saturation Voltage Source Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, T_A = 25°C, (Note 3) Figure 3		0.43	0.7		0.43	0.75	V
Saturation Voltage Sink Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, Full Range, (Note 3) Figure 4			0.9			0.9	V
Saturation Voltage Sink Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, T_A = 25°C, (Note 3) Figure 4		0.43	0.7		0.43	0.75	V
Input Current at Maximum Input Voltage Address Inputs (I_I)	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, Figure 5			1			1	mA
Input Current at Maximum Input Voltage Strobe Inputs (I_I)	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, Figure 5			2			2	mA
High Level Input Current Address Inputs (I_{IH})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, Figure 5		3	40		3	40	μA
High Level Input Current Strobe Inputs (I_{IH})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, Figure 5		6	80		6	80	μA
Low Level Input Current Address Inputs (I_{IL})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, Figure 5		−1	−1.6		−1	−1.6	mA
Low Level Input Current Strobe Inputs (I_{IL})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, Figure 5		−2	−3.2		−2	−3.2	mA
Supply Current, All Sources and Sinks Off From V_{CC1} ($I_{CC\,OFF}$)	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, Figure 6		14	22		14	22	mA
Supply Current, All Sources and Sinks Off From V_{CC2} ($I_{CC\,OFF}$)	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, Figure 6		7.5	20		7.5	20	mA
Supply Current From V_{CC1}, Either Sink On (I_{CC1})	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C, Figure 7		55	70		55	70	mA
Supply Current From V_{CC2}, Either Source On (I_{CC2})	V_{CC1} = 5.5V, V_{CC} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C, Figure 8		32	50		32	50	mA

Note 1: Voltage values are with respect to network ground terminal.

Note 2: For operation of LM55325 above +70°C free-air temperature, refer to Dissipation Derating Curve (Figure 12).

Note 3: These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

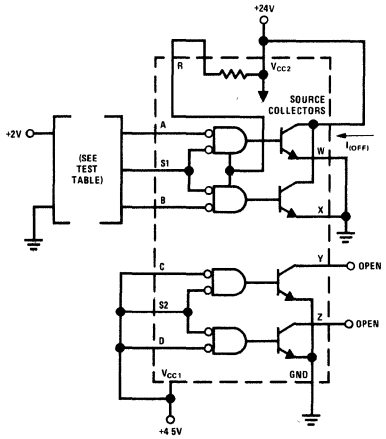
*All typical values are at T_A = 25°C.

**Not more than one output is to be on at any one time.

ac switching characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Propagation Delay Time, Low to High Level Output to Source Collectors (t_{PLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		25	50	ns
Propagation Delay Time, High to Low Level Output to Source Collectors (t_{PHL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		25	50	ns
Transition Time, Low to High Level Output to Source Outputs (t_{TLH})	V_{CC2} = 20V, R_L = 1 kΩ, C_L = 25 pF, Figure 10		55		ns
Transition Time, High to Low Level Output to Source Outputs (t_{THL})	V_{CC2} = 20V, R_L = 1 kΩ, C_L = 25 pF, Figure 10		7		ns
Propagation Delay Time, Low to High Level Output to Sink Outputs (t_{PLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		20	45	ns
Propagation Delay Time, High to Low Level Output to Sink Outputs (t_{PHL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		20	45	ns
Transition Time, Low to High Level Output to Sink Outputs (t_{TLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		7	15	ns
Transition Time, High to Low Level Output to Sink Outputs (t_{THL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		9	20	ns
Storage Time, Sink Outputs (t_S)	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		15	30	ns

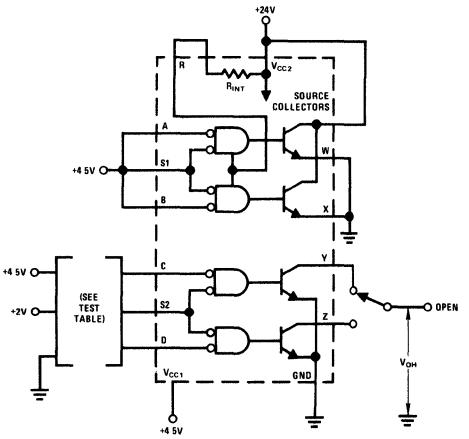
dc test circuits



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

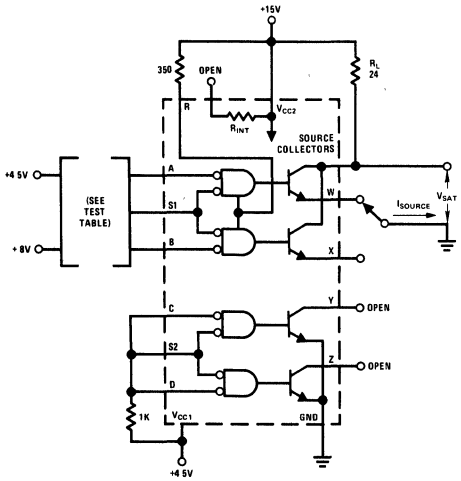


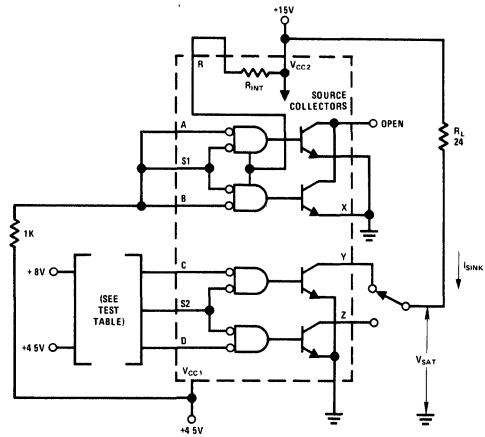
TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

FIGURE 2. V_{IH} and V_{OH}

dc test circuits(con't)





Note 1. Figures 3 and 4 parameters must be measured using pulse techniques $t_W = 200\mu s$, duty cycle $\leq 2\%$

TEST TABLE

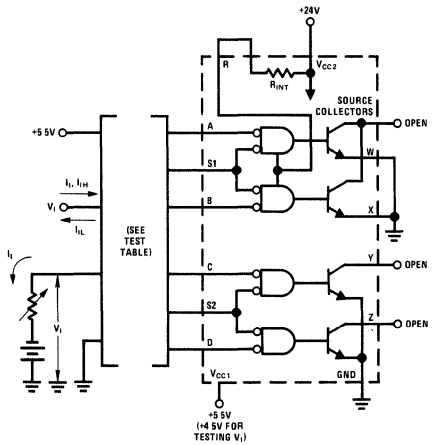
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

FIGURE 3. V_{IL} and Source V_{SAT}

TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V MEASURE I_I / APPLY V_I = 2.4V MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = −10 mA, MEASURE V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH}, and I_{IL}

dc test circuits(con't)

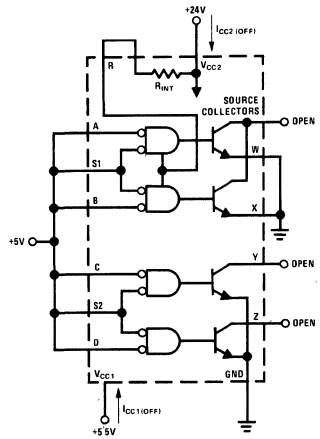
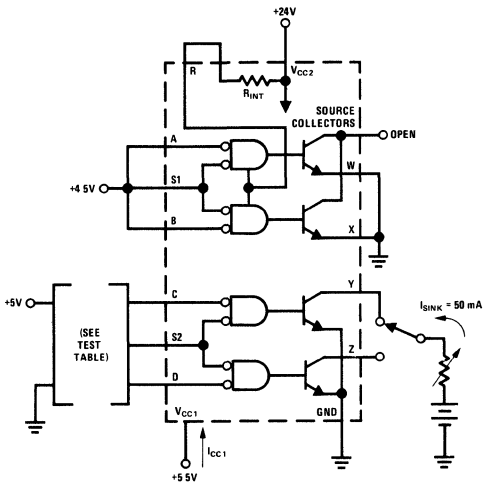


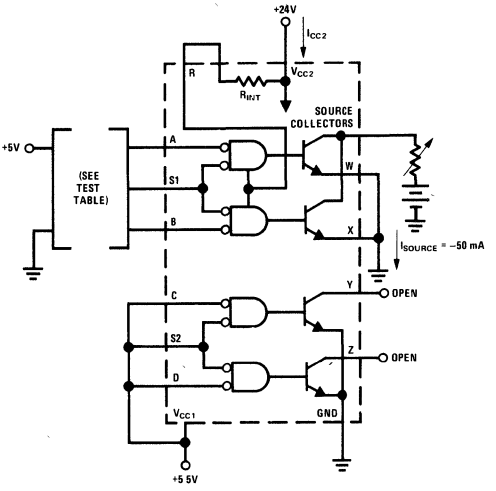
FIGURE 6. $I_{CC1(OFF)}$ and $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(SINK)}$	OPEN
5V	GND	GND	OPEN	$I_{(SINK)}$

FIGURE 7. I_{CC1}, Either Sink On

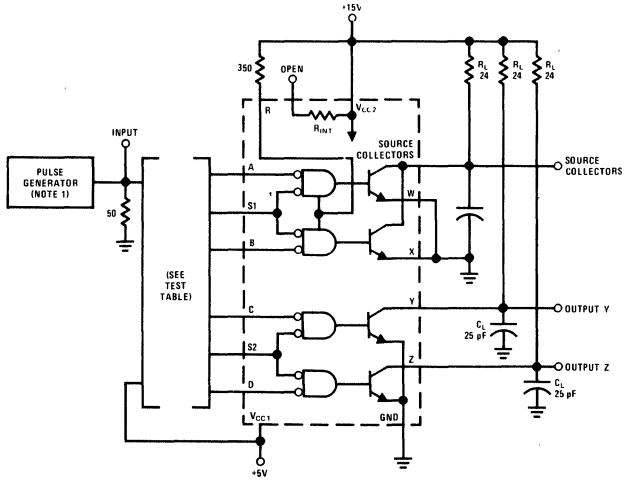


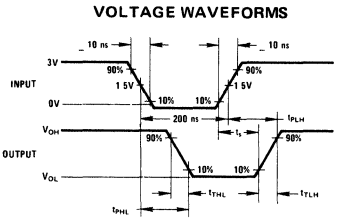
TEST TABLE

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

dc test circuits(con't)





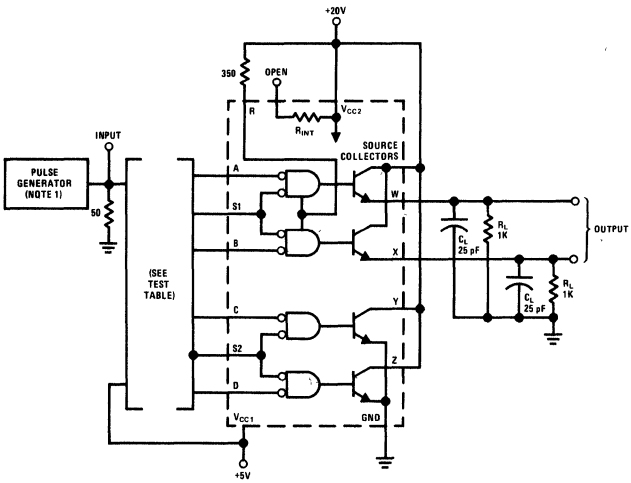
Note 1 The pulse generator has the followng characteristics $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$.

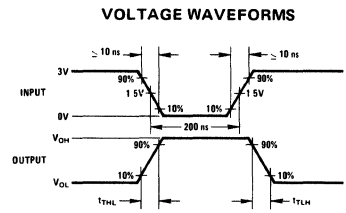
Note 2 C_L includes probe and jig capacitance

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times





Note 1 The pulse generator has the followng characteristics $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$

Note 2 C_L includes probe and jig capacitance

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

FIGURE 10. Transition Times of Source Outputs

applications

External Resistor Calculation

A typical magnetic-memory word drive requirement is shown in Figure 11. A source-output transistor of one LM75325 delivers load current (I_L). The sink-output transistor of another LM75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\ I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20V and V_L = 3V while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

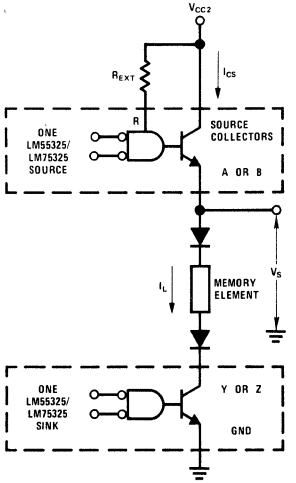
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1 For clarity, partial logic diagrams of two LM55325's are shown
Note 2 Source and sink shown are in different packages

FIGURE 11. Typical Application Data

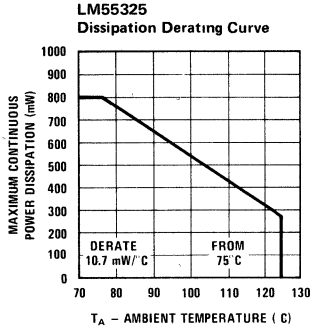


FIGURE 12. Thermal Information