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《新规 New · 变更》 Revision

产 品 规 格 书
Product Specification

产品名 Product: TFT-LCD Module

机种名 Model: LM645DU1A

【接收印栏】

※ 本基准书由封面、附件等全 26 页构成。
如果对该规格书有异议，请在下订单前提出。
※ This Product Specification have26 pages including the coversheet and Appendices. Please negotiate the objection point before purchase order.

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REVISION HISTORY

MODEL NO: LM645DU1A

DATE	NO.	REVISED No.	PAGE	SUMMARY	NOTE
2012/07/25	PN-PT-001	Ver.1.0	26	First Edition	Tentative
2012/8/21	PN-PT-002	Ver.1.1	26	Replace the connector of Converter Update module drawing	
2012/12/21	PN-PT-003	Ver.1.2	26	Update Optical Characteristics Update module drawing	

1. GENERAL DESCRIPTION

1.1 OVERVIEW

This module is color active matrix LCD module incorporating amorphous silicon TFT(Thin Film Transistor) LCD panel. It is composed of a color TFT-LCD panel, driver ICs, LED Backlight unit… etc. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with about 1,073,741,824 colors(R/G/B 10bit in each color) by using LVDS(Low Voltage Differential Signaling) to interface, +12V of DC supply voltage.

1.2 CHARACTERISTICS

Parameter	Technical literatures	Unit
Display size	163.9 (Diagonal)	cm
	64.5 (Diagonal)	inch
Active area	1428.48(H) x 803.52(V)	mm
Pixel Format	1920(H) x 1080(V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.744(H) x 0.744 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Unit Outline Dimensions	1463.08(H) × 848.9(H) × 1.776(D)	mm
Surface treatment	Anti glare Hard coating: (2H)	

1.3 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Remark
Module Size	Horizontal (H)	1455.48	1457.28	1459.08	mm	[Note 1]
	Vertical (V)	833.72	835.22	856.72	mm	[Note 1]
	Depth (D)	15.3	16.3	17.3	mm	[Note 1]
Weight			30		kg	

[Note 1] Please refer to the attached drawings for more information of front and back outline dimensions and the dimension of bosses are not included.

2. ABSOLUTE MAXIMUM RATINGS

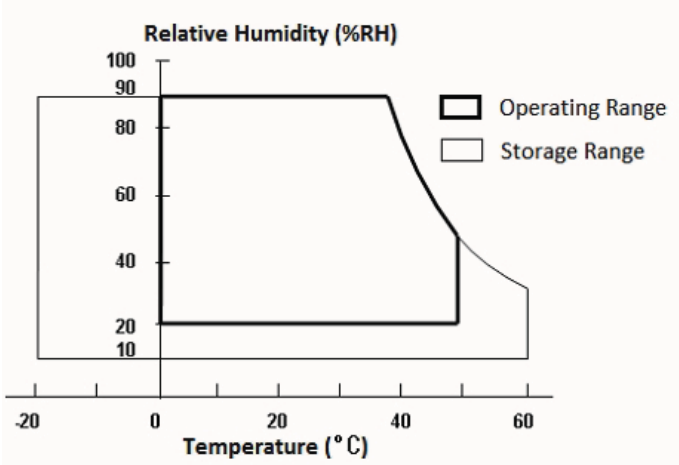
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Parameter	Symbol	Condition	Ratings		Unit	Remark
			Min.	Max.		
12V supply voltage	V_{CC}	Ta=25°C	0	+14.0	V	
Input voltage	Vin	Ta=25°C	-0.3	+3.6	V	[Note 1]
LVDS signal voltage	V_{LVDS}	Ta=25°C	0	+2.4	V	
Operation temperature	TOPR	-	0	+50	°C	[Note 2]
Storage temperature	TSTG	-	-20	+60	°C	

(*) "*Absolute Maximum Ratings*" is regulations that do not exceed it even momentarily.

(*) Stress beyond those listed under "*Absolute Maximum Ratings*" may cause permanent damage to the device.

[Note 1] Applies to the input signal expect supply voltage and LVDS signal.
[Note 2] Humidity: 90%RH Max.(Ta≦40°C), Maximum wet-bulb temperature at 39°C or less Ta≧40°C, No condensation.



3. Input Terminals

3.1 TFT panel driving

CN1 (Interface signals and +12V DC power supply)

Using connector : 91213-0510Y (ACES)

Mating connector : 91214-05130 (ACES), FI-RE51HL/FI-RE51CL (JAE)

Mating LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	I2C_SDA	I2C_Data (for Vcom adjust)[Note1]	Pull up:(3.3V)
3	I2C_SCL	I2C_Clock (for Vcom adjust)[Note1]	Pull up:(3.3V)
4	Reserved	It is required to set non-connection(OPEN)	
5	Frame	Frame frequency setting 0:100Hz 1:120Hz [Note2]	Pull down:(GND)
6	Reserved	It is required to set non-connection(OPEN)	
7	LVDS SEL	Select LVDS data order [Note3][Note4]	Pull up: (3.3V)
8	Reserved	It is required to set non-connection(OPEN)	
9	Reserved	It is required to set non-connection(OPEN)	
10	Reserved	It is required to set non-connection(OPEN)	
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN2 (Interface signals)

Using connector : 91213-0410Y(ACES)

Mating connector : 91214-04130(ACES) , FI-RE41HL/ FI-RE41CL (JAE)

Pin No.	Symbol	Function	Remark
1	Reserved (VCC)	(+12V Power Supply) (OPEN)	
2	Reserved (VCC)	(+12V Power Supply) (OPEN)	
3	Reserved (VCC)	(+12V Power Supply) (OPEN)	
4	Reserved	Non-Conection(OPEN)	
5	Reserved	Non-Conection(OPEN)	
6	Reserved	Non-Conection(OPEN)	
7	Reserved	Non-Conection(OPEN)	
8	Reserved	Non-Conection(OPEN)	
9	GND		
10	CIN0-	Cport (-)LVDS CH0 differential data input	
11	CIN0+	Cport (+)LVDS CH0 differential data input	
12	CIN1-	Cport (-)LVDS CH1 differential data input	
13	CIN1+	Cport (+)LVDS CH1 differential data input	
14	CIN2-	Cport (-)LVDS CH2 differential data input	
15	CIN2+	Cport (+)LVDS CH2 differential data input	
16	GND		
17	CCK-	Cport LVDS Clock signal(-)	
18	CCK+	Cport LVDS Clock signal(+)	
19	GND		
20	CIN3-	Cport (-)LVDS CH3 differential data input	
21	CIN3+	Cport (+)LVDS CH3 differential data input	
22	CIN4-	Cport (-)LVDS CH4 differential data input	
23	CIN4+	Cport (+)LVDS CH4 differential data input	
24	GND		
25	GND		
26	DIN0-	Dport (-)LVDS CH0 differential data input	
27	DIN0+	Dport (+)LVDS CH0 differential data input	
28	DIN1-	Dport (-)LVDS CH1 differential data input	
29	DIN1+	Dport (+)LVDS CH1 differential data input	
30	DIN2-	Dport (-)LVDS CH2 differential data input	
31	DIN2+	Dport (+)LVDS CH2 differential data input	
32	GND		
33	DCK-	Dport LVDS Clock signal(-)	
34	DCK+	Dport LVDS Clock signal(+)	
35	GND		
36	DIN3-	Dport (-)LVDS CH3 differential data input	
37	DIN3+	Dport (+)LVDS CH3 differential data input	
38	DIN4-	Dport (-)LVDS CH4 differential data input	
39	DIN4+	Dport (+)LVDS CH4 differential data input	
40	GND		
41	GND		

The equivalent circuit figure of the terminal.

[Note 1]

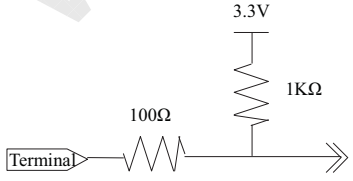


Fig.3-1-1 equivalent circuit (Pin No2,3)

[Note 2]

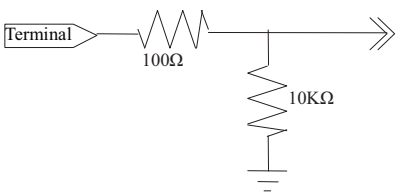


Fig.3-1-2 equivalent circuit (Pin No5)

[Note 3]

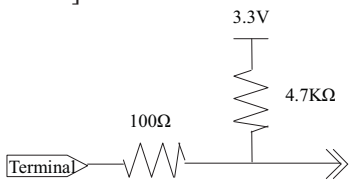


Fig.3-1-3 equivalent circuit (Pin No7)

[Note 4] LVDS Data order

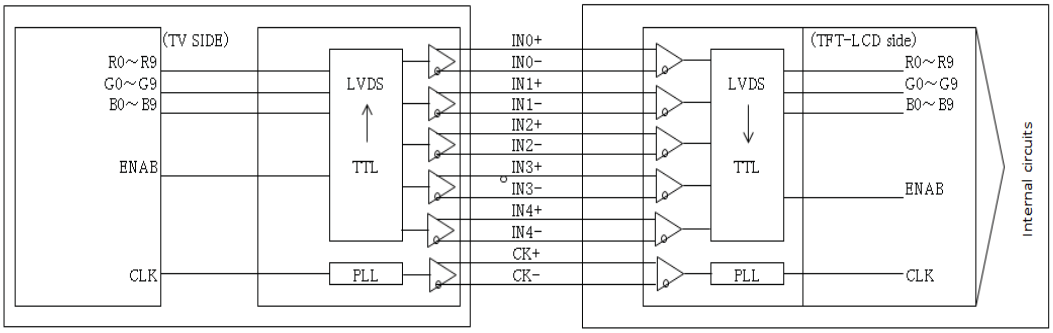
SELLVDS		
Data	H(3.3V) or OPEN [VESA]	L(GND) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

NA: Not Available

(*)Since the display position is prescribed by the rise of DE(Display Enable) signal, please do not fix DE signal during operation at ”High”.

3.2 Interface block diagram

Corresponding LVDS Transmitter: THC63LVD1023 or equivalent device.



※INx mean AINx,BINx,CINx,DINx (x=0~4) and
CK mean ACK,BCK,CCK,DCK

Fig.3-2 Interface block diagram

3.3 Block diagram

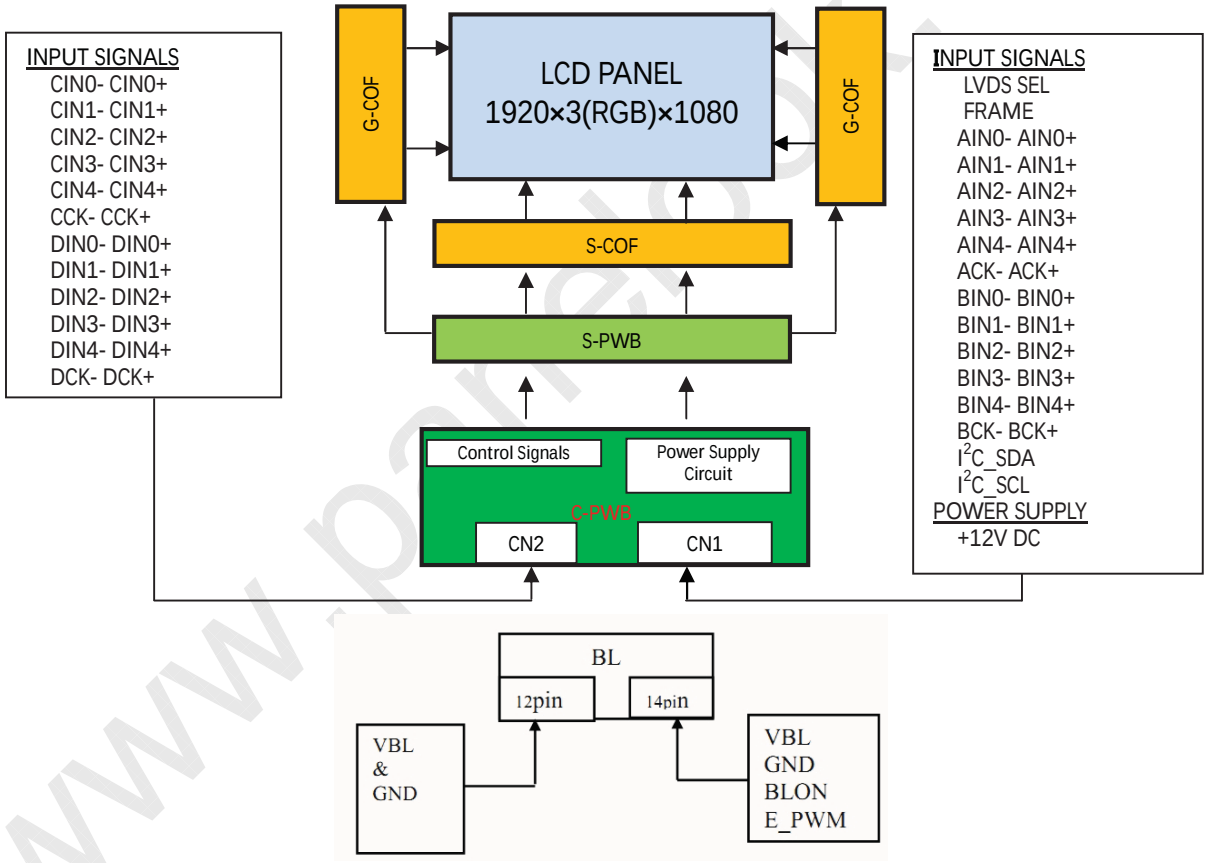


Fig.3-3 Block diagram

4. ELECTRICAL CHARACTERISTICS

4.1 DC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage		Vcc	11.4	12.0	12.6	V	[Note 1]
Current dissipation		Icc	-	0.74	1.2	A	[Note 2]
Inrush current		I_{RUSH}	-	-	5.5	A	[Note 3]
Permissible input ripple voltage		V_{RP}	-	-	100	mVp-p	Vcc=+12.0V
Input Low voltage		V_{IL}	0	-	0.7	V	[Note 4]
Input High voltage		V_{IH}	2.1	-	3.3	V	
Input leak current (Low)		I_{IL}	-	-	40	μA	V_I=0V [Note 4]
Input leak current (High)		I_{IH}	-	-	400	μA	V_I=3.3V [Note 4]
Terminal resistor		R_T	-	100	-	Ω	Differential input
Differential input threshold voltage	High	V_{TH}	-	-	100	mV	V_{CM} = +1.2V [Note 5]
	Low	V_{TL}	-100	-	-	mV	
Input Differential voltage		|VID|	200	400	600	mV	[Note 5]
Differential input common mode voltage		V_{CM}	|VID|/2	1.2	2.4-|VID|/2	V	[Note 5]

[Note 1]
Input voltage sequences
50us ≦ t1 ≦ 20ms
20ms < t2-1
20ms < t2-2
0 < t3-1 ≦ 1s
0 < t3-2 ≦ 1s
1s ≦ t4
300ms ≦ t5-1
300ms ≦ t5-2
0 < t6-1
0 < t6-2

Dip conditions for supply voltage
a) 9.1V ≦ V_{CC} < 10.8V
td ≦ 10ms
b) V_{CC} < 9.1V
Dip conditions for supply voltage is based on input voltage sequence.

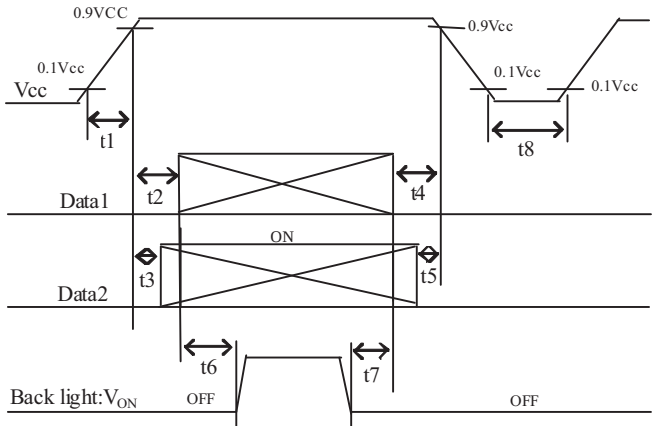


Fig. 4-1 Input voltage sequence

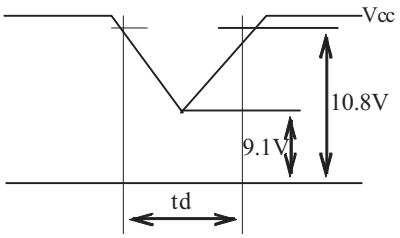


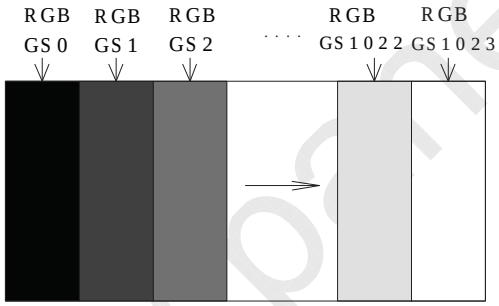
Fig. 4-2 Dip conditions for supply voltage

※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±,DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

※ Data2: LVDS SEL, FRAME

[Note1]About the sequence of data input and back light lighting, please base on the above-mentioned sequence. When back light is switched on before a panel operation or off after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

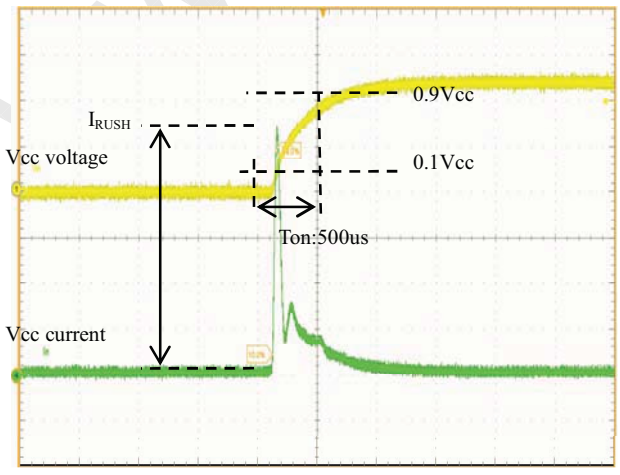
[Note 2]
Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)
The explanation of RGB gray scale is seen in section 8.



Vcc＝+12.0V
CK＝74.25MHz
Th＝7.41μs

Fig. 4-3 typical current situation

[Note 3]
Rush current is corrugated at the time of power on.



Ton: Vcc(+12V) Rising Time from 10% to 90%.
I: Current of Vcc(+12V)
I_{RUSH}: The max current after rising.

[HOW TO]
When you turn the C-PWB power on, measure the Vcc(12V) voltage and current at the same time.

Fig. 4-4 Waveform of rush current

[Note 4] I^2C_SCL, I^2C_SDA, Frame, LVDS SEL
[Note 5] Applies to the LVDS signal

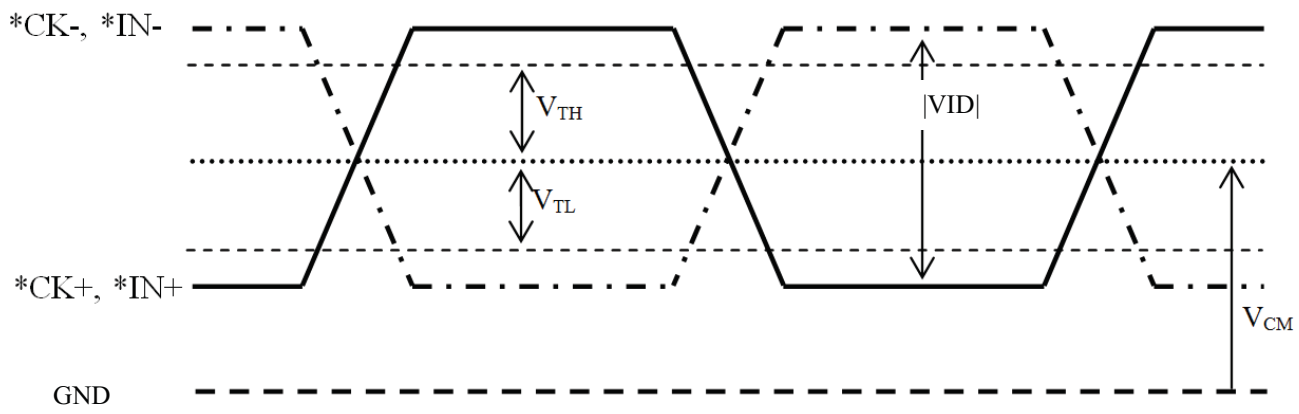


Fig. 4-5 LVDS input characteristics

5. TIMING CHARACTERISTICS OF INPUT SIGNALS

5.1 Timing Characteristics of LVDS Signal

Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock	Frequency	$1/T_C$	67	74.25	80	MHz
Horizontal period	Total period	TH	515	550	825	clock
			6.94	7.41	11.1	μs
	Display period (High)	THd	480	480	480	clock
Vertical period	Total period	TV	1120	1125	1400	line
			73.052	120	120.64	Hz
	Display period (High)	TVd	1080	1080	1080	line

[Note]-When vertical period is very long, flicker and etc. may occur.
-Please turn off the module after make it shows the black screen.
-Please make sure that length of vertical period equal to the integral multiple of length of horizontal period. Otherwise, the screen may not display properly.

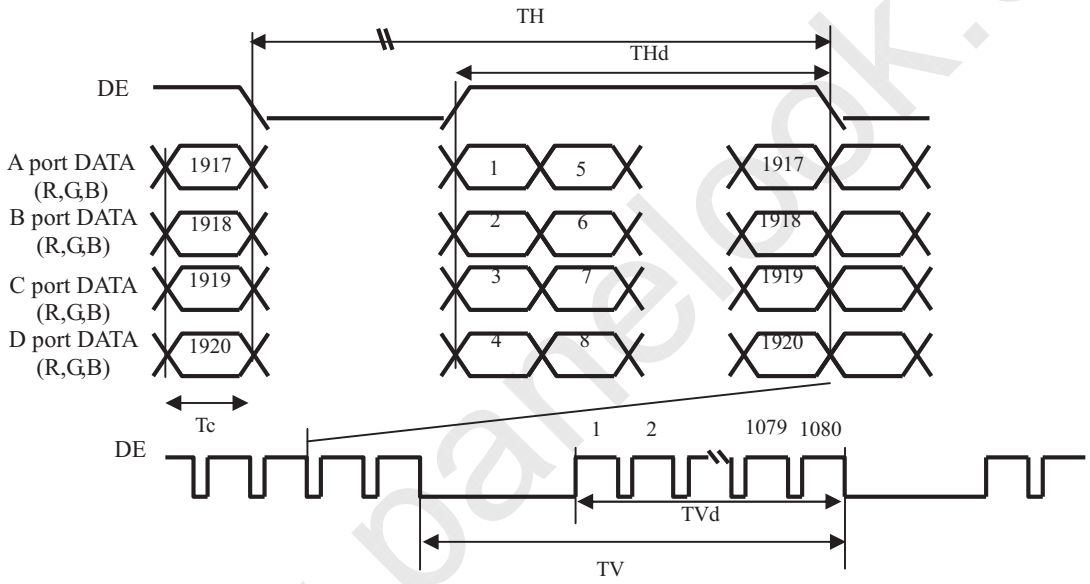


Fig.5-1 Timing characteristics of input signals

5.2 LVDS data skew

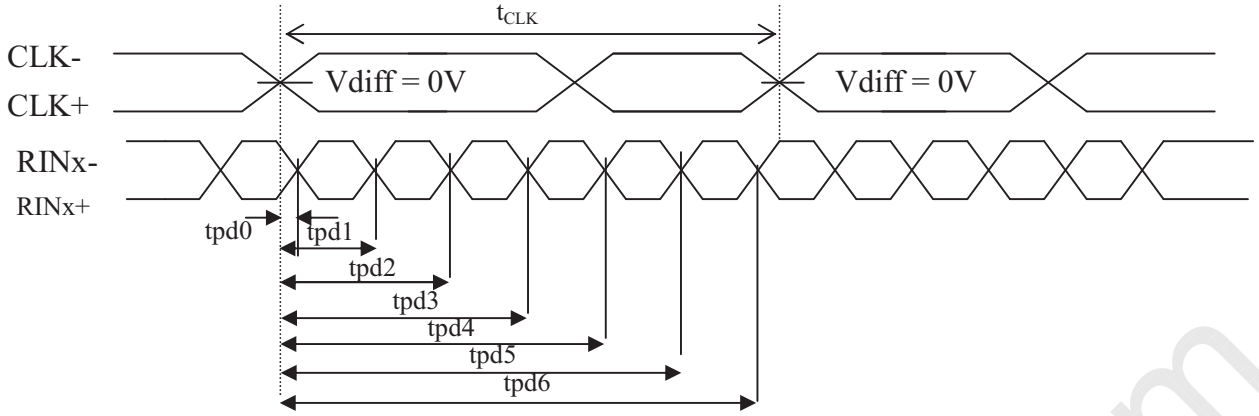
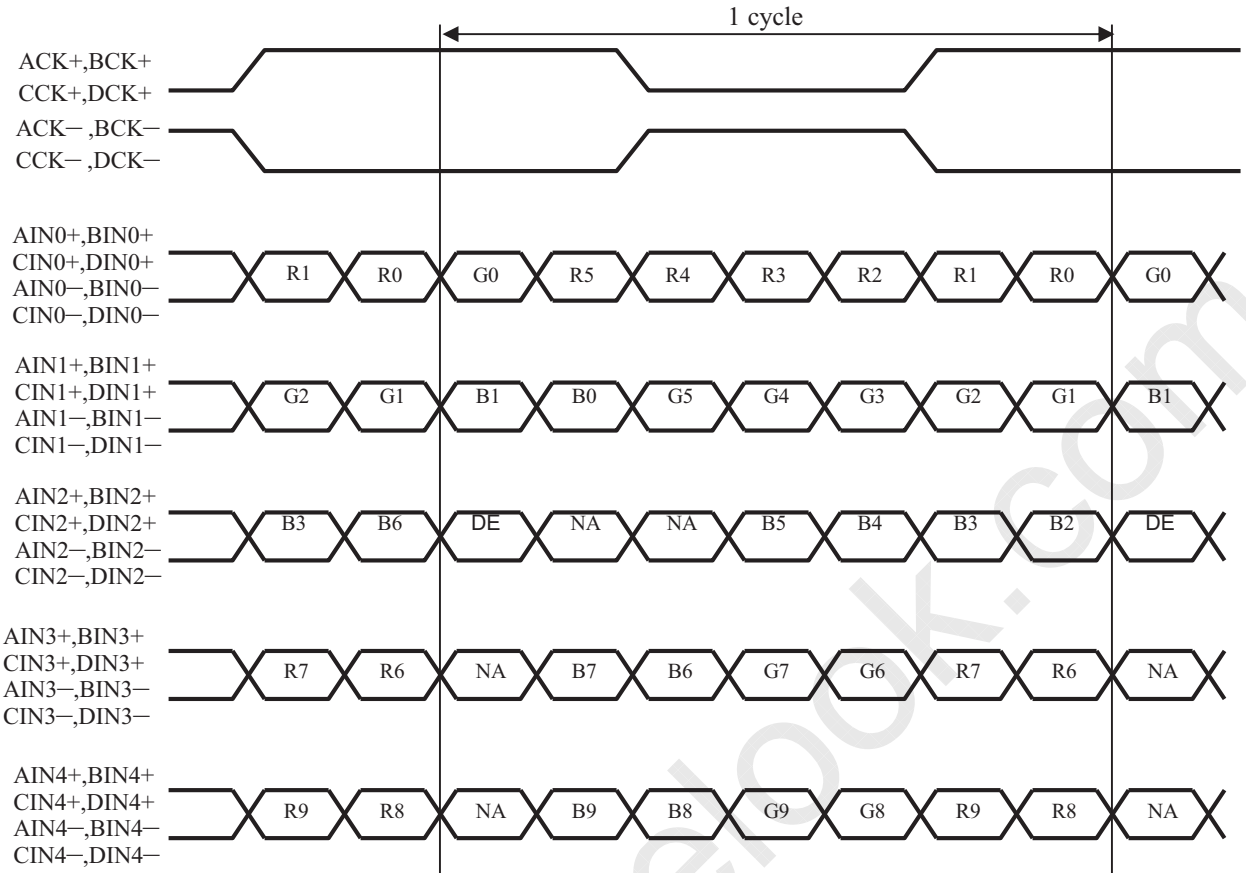


Fig.5-2 LVDS data skew

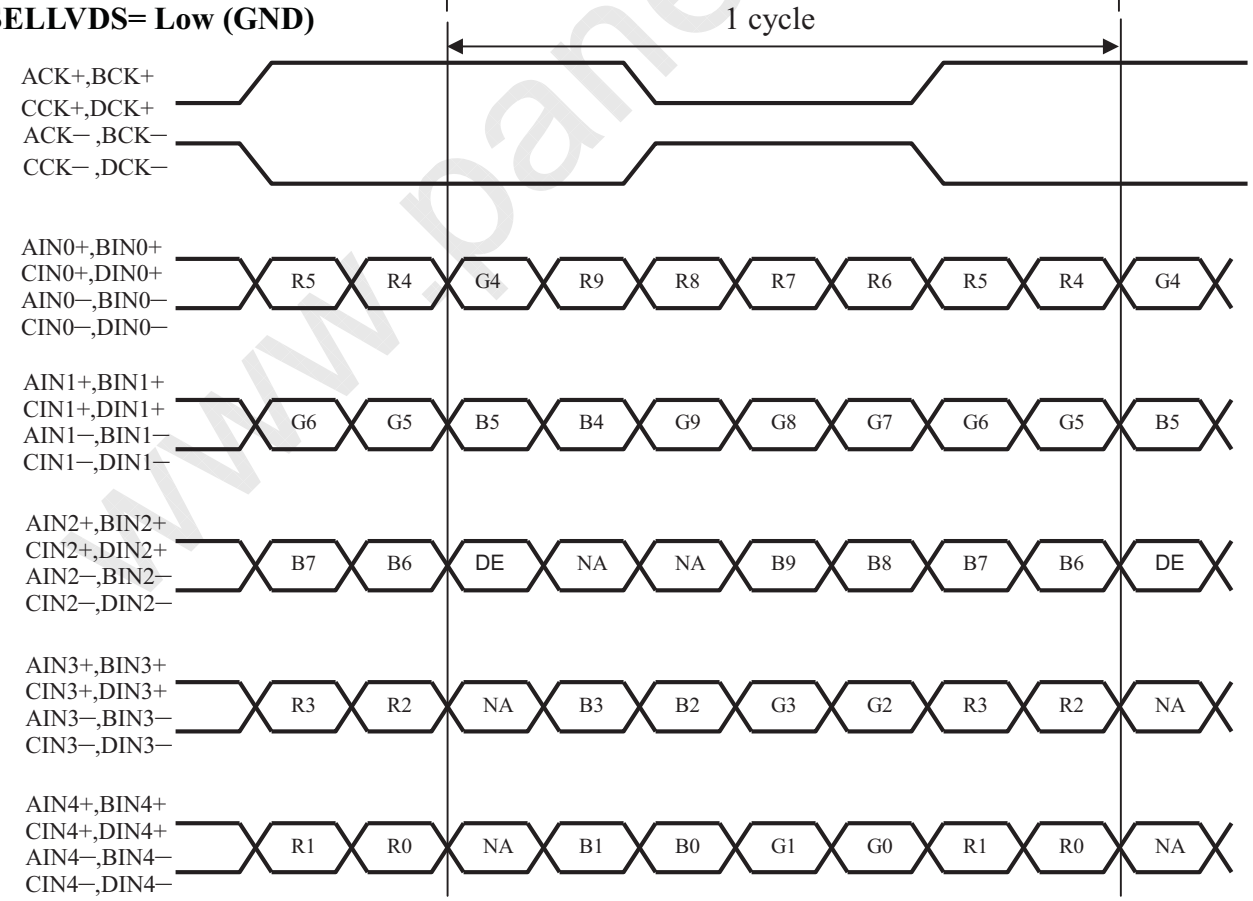
The item		Symbol	min.	typ.	max.	unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	(-0.45)	0	(0.45)	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	(1*tCLK/7-0.45)	1* tCLK /7	(1* tCLK /7+0.45)	
	Delay time, CLK rising edge to serial bit position 2	tpd2	(2* tCLK /7-0.45)	2* tCLK /7	(2* tCLK /7+0.45)	
	Delay time, CLK rising edge to serial bit position 3	tpd3	(3* tCLK /7-0.45)	3* tCLK /7	(3* tCLK /7+0.45)	
	Delay time, CLK rising edge to serial bit position 4	tpd4	(4* tCLK /7-0.45)	4* tCLK /7	(4* tCLK /7+0.45)	
	Delay time, CLK rising edge to serial bit position 5	tpd5	(5* tCLK /7-0.45)	5* tCLK /7	(5* tCLK /7+0.45)	
	Delay time, CLK rising edge to serial bit position 6	tpd6	(6* tCLK 7-0.45)	6* tCLK /7	(6* tCLK /7+0.45)	

5.3 LVDS data mapping

SELLVDS= High (3.3V) or OPEN



SELLVDS= Low (GND)



DE: Display Enable, NA: Not Available (Fixed Low)

5.4 Input Signal, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Gray Scale	Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	⇩	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Fig.5-4 input signals

0: Low level voltage, 1: High level voltage.

Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

6. OPTICAL CHARACTERISTICS

Ta=25°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ 21 θ 22	CR ≥ 10	70	88	-	Deg.	[Note1,4]
	Vertical	θ 11 θ 12		70	88	-	Deg.	
Contrast ratio		CR	θ=0 deg.	3500	5000	-	-	[Note2,4]
Response time		τ_{DRV}		-	5	-	ms	[Note3,4,5]
Luminance(White)		cd/m^2		400	450	-	-	[Note 4]
Chromaticity of white		x		Typ.-0.03	0.280	Typ.+0.03	-	[Note 4]
		y		Typ.-0.03	0.290	Typ.+0.03	-	
Chromaticity of red		x		Typ.-0.03	0.643	Typ.+0.03	-	
		y		Typ.-0.03	0.341	Typ.+0.03	-	
Chromaticity of green		x		Typ.-0.03	0.281	Typ.+0.03	-	
		y		Typ.-0.03	0.641	Typ.+0.03	-	
Chromaticity of blue		x		Typ.-0.03	0.149	Typ.+0.03	-	
		y		Typ.-0.03	0.080	Typ.+0.03	-	
Color Gamut		NTSC	-	-	72	-	%	
White variation		δW	-	-	-	1.33		[Note 6]
Crosstalk		CT	-	-	-	4	%	[Note 7]
Color temperature variation		δTc	-	-	-	1.1	-	[Note 4,8]

[Note 1]
-The measurement shall be executed 60 minutes after lighting at rating.

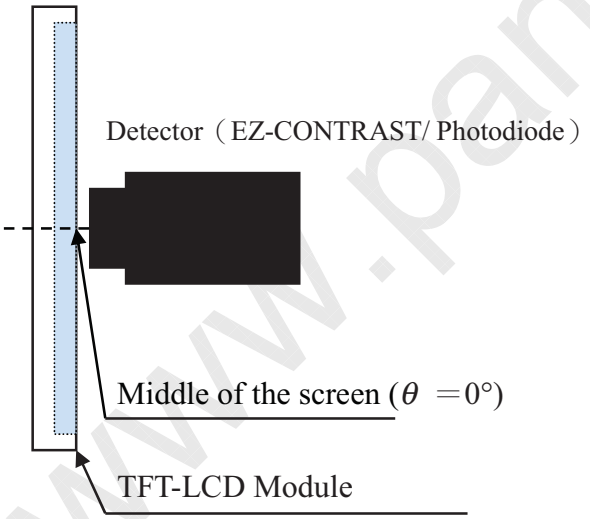


Fig.6-1 Measurement of Viewing angle range and Response time.
(Viewing angle range: EZ-CONTRAST, Response time: Photodiode)

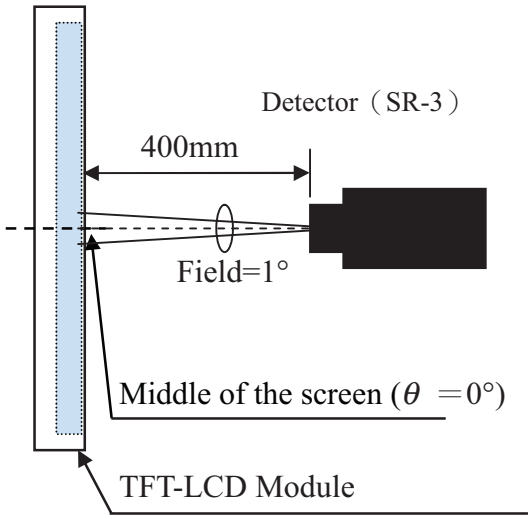


Fig.6-2 Measurement of Contrast, Luminance, Chromaticity, White variation, Crosstalk and Color temperature variation.

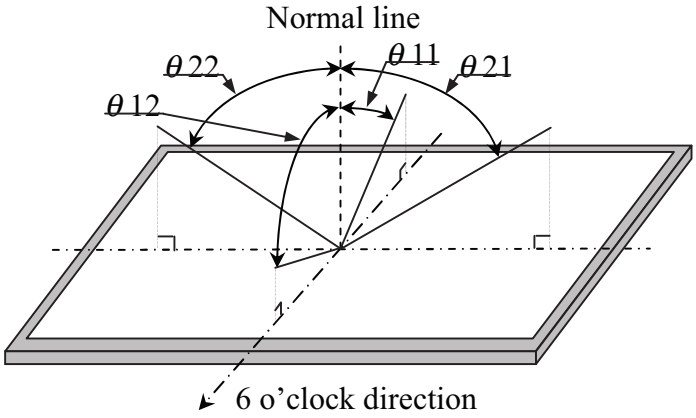


Fig.6-3 Viewing angle

[Note 2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance(Brightness) with all pixels white}}{\text{Luminance(Brightness) with all pixels Black}}$$

[Note 3] Definition of response time

The response time (τ_{DRV}) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%) and "any level of gray (0%, 25%, 50%, 75% and 100%).

	0%	25%	50%	75%	100%
0%		τ_r:0%–25%	τ_r:0%–50%	τ_r:0%–75%	τ_r:0%–100%
25%	τ_d:25%–0%		τ_r:25%–50%	τ_r:25%–75%	τ_r:25%–100%
50%	τ_d:50%–0%	τ_d:50%–25%		τ_r:50%–75%	τ_r:50%–100%
75%	τ_d:75%–0%	τ_d:75%–25%	τ_d:75%–50%		τ_r:75%–100%
100%	τ_d:100%–0%	τ_d:100%–25%	τ_d:100%–50%	τ_d:100%–75%	

τ*:x-y...response time from level of gray(x) to level of gray(y)

$\tau_{DRV} = \Sigma$ (τ*:x-y)/20

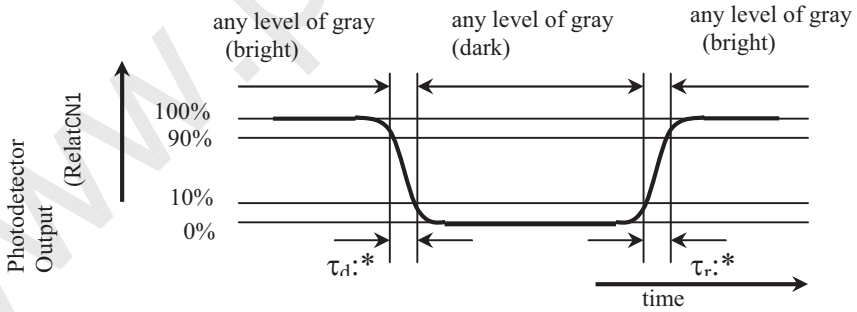


Fig.6-4 Response time

[Note 4] This shall be measured at center of the screen.

[Note 5] This value is valid when O/S driving is used at typical input time value.

[Note 6] Definition of white variation;

White variation is defined as the following with nine measurements. (1～9)

$$\delta w = \frac{\text{Maximum luminance of nine points(brightness)}}{\text{Minimum luminance of nine points(brightness)}}$$

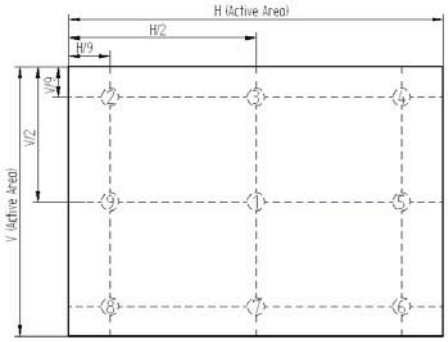


Fig.6-5 measurement locations of white variation

[Note 7]
Definition of Crosstalk (CT);

$CT=|Y_B - Y_A| / Y_A \times 100(\%)$

Where;

Y_A=Luminance of measured location without gray level 0 pattern (cd/m^2)
Y_B=Luminance of measured location with gray level 0 pattern (cd/m^2)

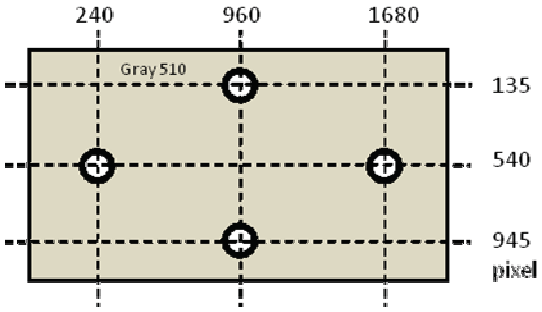


Fig.6-6 measurement locations of Y_A

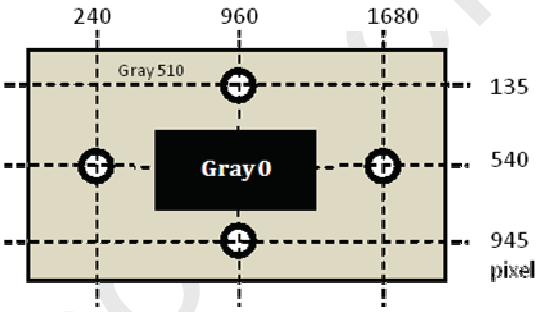


Fig.6-7 measurement locations of Y_B

[Note 8]
Definition of color temperature variation (δTc);

$$\delta Tc = \frac{\text{Maximum color temperature of gray within the range of V255 to V1023}}{\text{Minimum color temperature of gray within the range of V255 to V1023}}$$

7. CONVERTER FOR BACK LIGHTING

7.1 Electrical specification

Ta = 25°C, Turn on for 30 minutes

Item		Symbol		Min.	Typ.	Max.	Unit	Note
LED Life Time		LT		30000			hr	【Note 1】
Input Voltage		VBL		22.8	24	25.2	V	【Note 2】
Input Current		IIN			6.7	7.5	A	【Note 3】
Abnormality detection output terminal		ERR	High	2.3		4.0	V	
			LOW	0		0.8		
E_PWM	Duty Ratio	D		10		100	%	
	Frequency	Fr		160	200	240	Hz	
ON /OFF Control Voltage	ON	Von/off		2.2		5.5	V	
	OFF			0		0.8		
Power Consumption (Backlight)		PBL			160.8	180	W	【Note 3】

[Note 1] Definition of the LED life time：It means when the luminance of LED reduces to less than 50% of its initial value.
[Note 2] Ripple voltage that occur at the instant of power-on can't exceed 27V.
[Note 3] 25℃; IPW=0V(Max.), after power on for 30 Minutes；Max value of the power consumption and input current is measured at initial turn on of the backlight.

7.2 Input pin assignment

14pin: CviLux CI0114M1HR0-LF

Pin No.	Symbol	Pin configuration(function)
1	VBL	Operating Voltage Supply,+24DC regulated
2	VBL	Operating Voltage Supply,+24DC regulated
3	VBL	Operating Voltage Supply,+24DC regulated
4	VBL	Operating Voltage Supply,+24DC regulated
5	VBL	Operating Voltage Supply,+24DC regulated
6	GND	GND and Current Return
7	GND	GND and Current Return
8	GND	GND and Current Return
9	GND	GND and Current Return
10	GND	GND and Current Return
11	ERR	Abnormality detection output terminal Normal： Low; Abnormal:High
12	BLON	BL on-off high for BL on; Low for BL off
13	NC	NC
14	E_PWM	External PWM (10%-100% duty, open for 100%)

12 pin CviLux CI0112M1HR0-LF

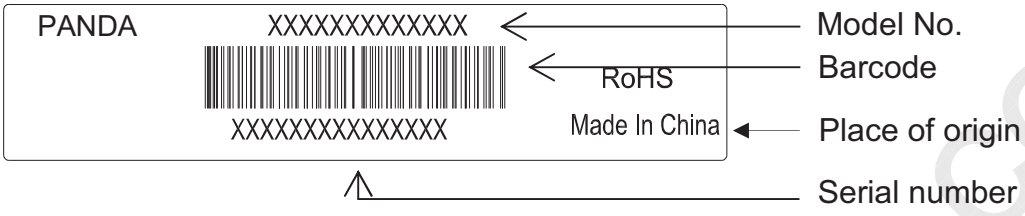
Pin No.	Symbol	Pin configuration(function)
1	VBL	Operating Voltage Supply,+24DC regulated
2	VBL	Operating Voltage Supply,+24DC regulated
3	VBL	Operating Voltage Supply,+24DC regulated
4	VBL	Operating Voltage Supply,+24DC regulated
5	VBL	Operating Voltage Supply,+24DC regulated

6	GND	GND and Current Return
7	GND	GND and Current Return
8	GND	GND and Current Return
9	GND	GND and Current Return
10	GND	GND and Current Return
11	NC	NC
12	NC	NC

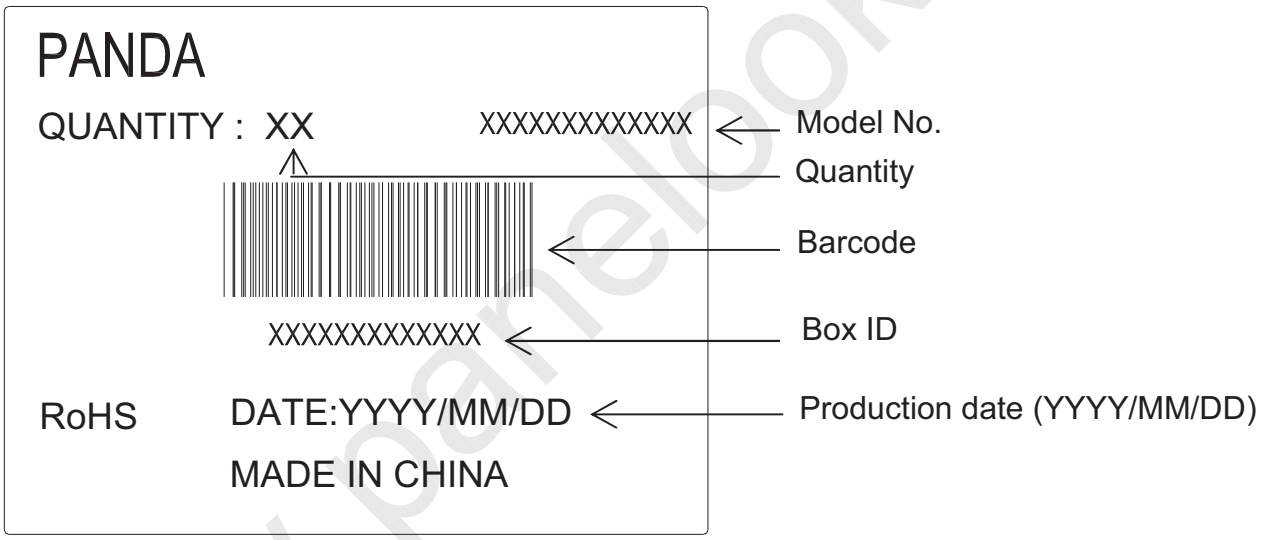
8. DEFINITION OF LABELS

8.1 MODULE LABEL

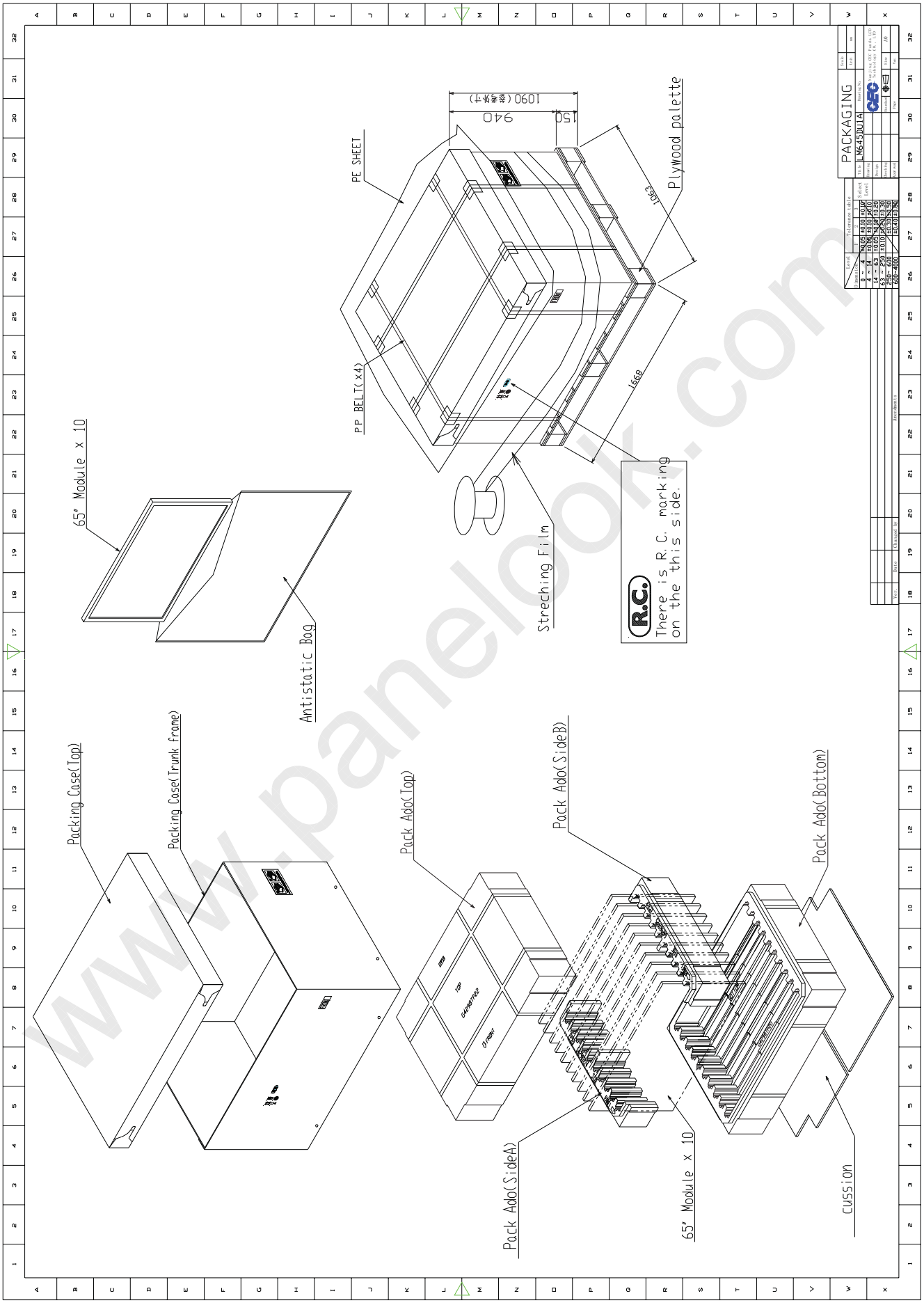
The label of displays, product model (LM645DU1A), a product number is stuck on the Module.



8.2 PACKING LABEL



9. PACKING



10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(a) Do not apply rough force such as bending or twisting to the module during assembly.

(b) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(c) Since the LCM consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, person who is handling an LCM should be grounded though adequate methods such as an anti-static wrist band. Connector pins should not be touched directly with bare hands.

Reference: Process control standard is shown as follow,

	item	Management standard value and performance standard
1	Anti-static mat(shelf)	1to50 [Mega ohm]
2	Anti-static mat(floor, desk)	1to100 [Mega ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within two seconds.
4	Anti-static wrist band	0.8 to 10 [Mega ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [℃]
7	Humidity	60 to 70 [%]

(d) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(e) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(f) Be sure to turn off the power supply when inserting or disconnecting the cable.

(g) Do not disassemble the module.

(h) Front polarizer can easily be damaged, so please pay attention on it.

(i) Using a absorbent cotton or other soft cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(j) Since long contact with drops of water may cause discoloration or spots, please wipe off them as soon as possible.

(k) The Panel will be broken or chipped when it is dropped or bumped against a hard substance.

(l) Applying too much force and stress to PWBs and drivers may cause a malfunction electrically and mechanically.

(m) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

(n) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(o) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(p) This LCM is corresponded to ROHS.

(q) When any question or issue occurs, it shall be solved by mutual discussion.

10.2 SAFETY PRECAUTIONS

(a) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(b) After the module's end of life, it is not harmful in case of normal operation and storage.

11. RELIABILITY

(a) Environment test condition

Test item	Q'ty	Condition
High temperature storage test	3	Ta= 60°C, 240h
Low temperature storage test	3	Ta= -20°C, 240h
High temperature operation test	3	Ta= 50°C, 240h
Low temperature operation test	3	Ta= 0°C,240h
Vibration test (With packing)	1(PKG)	Wave form： Random Vibration level： 1.0 Grms Bandwidth： 5-50 Hz Duration： X,Y,Z, 30 min Each direction per 10 min

(b) ESD test

Test item	Condition
Connector	200 pF， 0 Ω， ±250 V By using contact-mode to discharge each pin one time and then check the module frame.
Module	150pF， 330Ω， ±8KV(contact-mode),±15KV(air-mode) 1. Under test conditions, by using air-mode to discharge each test point 25 times continuously and then check the module frame. 2. Under test conditions, by using contact-mode to discharge each test point of panel frame 25 times continuously and then check the module frame.

[Result evaluation criteria]
Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

12. MECHANICAL DRAWING