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	SHARP CORPORATION	REPRESENTATIVE DIVISION
		■DUTY Panel
	SPECIFICATION	Development center

DEVICE SPECIFICATION for
Passive Matrix LCD Unit
(640×480 dots)

Model No.

LM64P10

REIN Components GmbH

Lötscher Weg 66 · D-41334 Nettetal
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REIN
Components

☐CUSTOMER'S APPROVAL

DATE _____

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SHARP CORPORATION

SHARP

SPEC No.	MODEL No.
LC92521A	**LM64P10**

DOC. FIRST ISSUE .

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IDENT. DATA No.

DATA	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL
JUL. 13. 1993	Page. 17	△1	LCD unit outline dimensions changed	
JUL. 13. 1993	Page. 18	△2	HMBS3A42W130C HMBSA42W130C → or FLE-30130C(AE)B	

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| | | | | LM64P10 |

1. Application

   This data sheet is to introduce the specification of LM64P10, Passive Matrix type
   LCD Unit.

2. Construction and Outline

   Construction: 640×480 dots display unit consisting of an LCD panel,
   PWB(printed wiring board) with electric components
   mounted onto, TAB(tape automated bonding) to connect the LCD panel
   and PWB electrically, and plastic chassis with CCFT backlight
   and bezel to fix them mechanically.

BEZEL   LSI (TAB)

LCD (with Anti-glare treatment.
      Pencil hardness more than 3H.)

LIGHT PIPE

PWB   BACKLIGHT HOLDER

CCFT
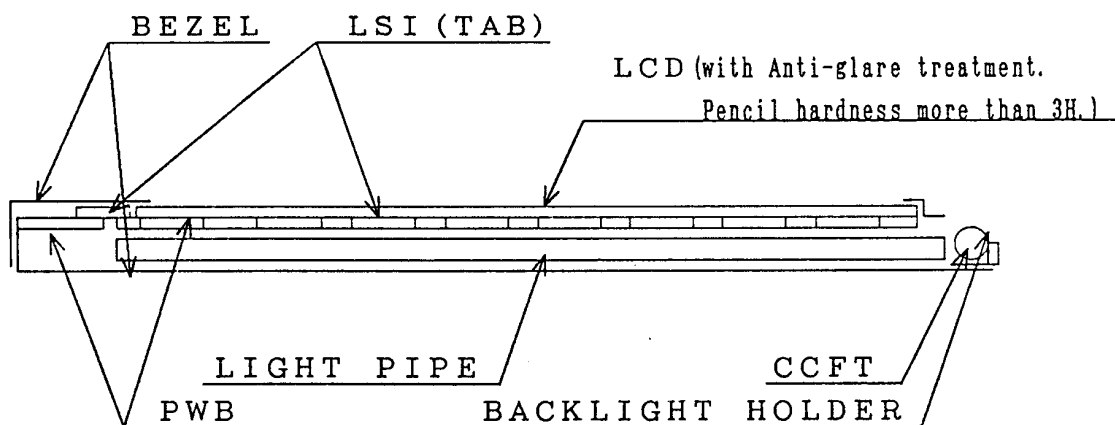
Outline   : See Fig. 10
Connection   : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	200.5 (W) × 141 (H) × 7MAX (D) ‡1‡2	mm
Effective viewing Area	151 (W) × 113.4 (H)	mm
Display format	640 (W) × 480 (H)　full dot	—
Dot size	0.21×0.21	mm
Dot spacing	0.02	mm
Dot color	White‡3‡4	—
Background color	Black‡3‡4	—
Weight	Approx. 260	g

‡1 Excluded the mounting tabs.

‡2 Excluded the allowance of deformation.

‡3 Due to the characteristics of the LC material, the colors vary
　　with environmental temperature.

‡4 Negative-type display
　　Displayed data 'H' : Dots ON : White
　　Displayed data 'L' : Dots OFF: Black

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	$V_{DD}-V_{SS}$	0	6.0	V	Ta=25 °C
Supply voltage (LCD drive)	$V_{DD}-V_{EE}$	0	28.0	V	Ta=25 °C
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25 °C

4-2 Environmental Conditions

<u>Table 3</u>

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 °C	+60 °C	0 °C	+45 °C	Note 4
Humidity	Note 1		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		6 directions (±X±Y±Z)

Note 1) Ta≦40 °C.....95 % RH Max

Ta>40 °C.....Absolute humidity shall be less than Ta=40 °C/95 % RH.

Note 2) There test conditions are in accordance with ˙IEC 68-2-6˙.

Frequency	5 Hz∼57 Hz	57 Hz∼ 500 Hz
Vibration level	−	9.8 m/s²
Vibration width	0.075 mm	−
Interval	10 Hz∼500 Hz∼10 Hz/11 mm	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation: 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X／±Y／±Z

Note 4) Care should be taken so that the LCD Unit may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characterictics

Tabel 4　　Ta=25 ℃, V_{DD}=5 V±5 %

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}			4.75	5.0	5.25	V
Supply voltage (LCD drive)	V_{SS}-V_{EE}	Note 1) Note 2)		21.7	16.9	13.3	V
Input signal voltage	V_{IN}	'H' level		0.8 V_{DD}	—	V_{DD}	V
		'L' level		0	—	0.2 V_{DD}	V
Input leakage current	I_{IL}	'H' level		—	—	250	μA
		'L' level		-250	—	—	μA
Supply voltage (Logic)	I_{DD}	Note 3)		—	25	35	mA
Supply voltage (LCD drive)	I_{EE}			—	20	26	mA
Power consumption	Pd			—	480	630	mW

Note 1) The viewing angle θ at which the optimum contrast is obtained can be set
by adjusting VEE-VSS. Refer to Fig.4 for the definition of θ.

Note 2) Max. and Min. values are specified as the Max. and Min. voltage
within the condition of operational temperature range (0～45 ℃).
Typ. values are specified as the typical voltage at 25 ℃.

Note 3) Display high frequency pattern.

V_{DD} = 5 V, V_{SS}-V_{EE} = 16.9 V , Frame frequency = 85 Hz, Display pattern = 4 bit checker

Display ■■■■□□□□■■■■□□□□■■■■□□□□
pattern □□□□■■■■□□□□■■■■□□□□■■■■
■■■■□□□□■■■■□□□□■■■■□□□□

5-2 Input capacitance

Table 5

Signal	Input capacitance
S	40 pF TYP
CP1	250 pF TYP
CP2	200 pF TYP
DU0～DU3	200 pF TYP
DL0～DL3	200 pF TYP

5-3 Interface signals

Table 6

○LCD

Pin No	Symbol	Description	Level
1	S	Scan start-up signal	˙H˙
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	DISP	Display control signal	Display on ..˙H˙ off..˙L˙
5	VDD	Power supply for logic and LCD (+5V)	
6	VSS	Ground potential	
7	VEE	Power supply for LCD (-)	
8	DU0	Display data signal (Upper half)	H (ON), L (OFF)
9	DU1		
10	DU2		
11	DU3		
12	DL0	Display data signal (Lower half)	H (ON), L (OFF)
13	DL1		
14	DL2		
15	DL3		

○CCFT

Pin No	Symbol	Description	Level
1	GND	Ground line (from Inverter)	-
2	NC	-	-
3	NC	-	-
4	HV	High voltage line (from Inverter)	-

Note) Pin No. and its location are shown in Fig. 10.

○LCD

Used connector: 53261-1510 (MOLEX)

Correspondable connector: 51021-1500 (MOLEX)

○CCFT

Used connector: M63M83-04 (MITSUMI)

Correspondable connector: M60-04-30-114P (MITSUMI)

M60-04-30-134P (MITSUMI)

M61M73-04 (MITSUMI)

COLUMN

ROW

	1dot	2dot	3dot		640dot
1dot	1· 1	1· 2	1· 3		1·640
2dot	2· 1	2· 2			
3dot	3· 1				
240dot	240· 1				240·640
241dot	241· 1				241·640
480dot	480· 1				480·640

Note) 1·2 means 1st row 2nd column dot.

COLUMN

ROW

	1 2 3 4 5 6 7 8		640
1dot	DU3 DU2 DU1 DU0 DU3 DU2 DU1 DU0		DU3 DU2 DU1 DU0
2dot	DU3 DU2 DU1 DU0 DU3 DU2 DU1 DU0		
3dot	DU3 DU2 DU1 DU0		
240dot	DU3 DU2 DU1 DU0		DU3 DU2 DU1 DU0
241dot	DL3 DL2 DL1 DL0		DL3 DL2 DL1 DL0
480dot	DL3 DL2 DL1 DL0		DL3 DL2 DL1 DL0

Fig. 1 Dot chart of display area

CP1

CP2

DU3　240·637　Invalid　1· 1　1· 5　1·637　Invalid　2· 1　2·637

DU2　240·638　Invalid　1· 2　1· 6　1·638　Invalid　2· 2　2·638

DU1　240·639　Invalid　1· 3　1· 7　1·639　Invalid　2· 3　2·639

DU0　240·640　Invalid　1· 4　1· 8　1·640　Invalid　2· 4　2·640

DL3　480·637　Invalid　241· 1　241· 5　241·637　Invalid　242· 1　242·637

DL2　480·638　Invalid　241· 2　241· 6　241·638　Invalid　242· 2　242·638

DL1　480·639　Invalid　241· 3　241· 7　241·639　Invalid　242· 3　242·639

DL0　480·640　Invalid　241· 4　241· 8　241·640　Invalid　242· 4　242·640

S

CP2 × 640/4 pulses

R
e
d
u
c
e
d

CP1

DU0~3　1·(1~640)　240·(1~640)　1·(1~640)

DL0~3　241·(1~640)　480·(1~640)　241·(1~640)

S

CP1 × 240 pulses

Fig.2 Data input timing

Fig.3 Interface timing chart

$V_{IH}=0.8$ vDD
$V_{IL}=0.2$ V_{DD}

* 1   See table 7

Table 7　Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0[*1]		16.9	ms
CP2 clock cycle	T_{CP2}	152			ns
'H' level clock width	t_{CWH}	65			ns
'L' level clock width	t_{CWL}	65			ns
'H' level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_{H}	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{S21}	0			ns
CP1↑ clock allowance time from CP2↓	t_{S12}	0			ns
Clock rise/fall time	tr, tf			t_{rf}[*2]	ns

*1 : LCD unit functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125 Hz). Owing to the characteristics of LCD unit, 'shadowing' will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and 'shadowing'. But since judgement of display quality is subjective and display quality such as 'shadowing' is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD unit is propotional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 :　$t_{rf} = 50$　in case　$t_{CT} = (T_{CP2} - t_{CWH} - t_{CWL})/2 \geqq 50$
　　　　$t_{rf} = t_{CT}$　in case　$t_{CT} = (T_{CP2} - t_{CWH} - t_{CWL})/2 < 50$

6. Unit Driving Method

　6.1 Circuit configuration

　　Fig.9 shows the block diagram of the Unit's circuitry.

　6.2 Display Face Configuration

　　The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640×240 dots) is driven at 1/240 duty ratio.

　6.3 Input Data and Control Signal

　　The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

　　Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

　　When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

　　At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

　　While the 1st rows of data are being displayed, the 2nd rows of data are entered When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

　　Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. The data input proceeds to the next display face.

　　Scan start-up signal S generates scan signal to drive horizontal electrodes.

　　Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of tranferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3} (upper display segment) and DL_{0-3} (lower display segment).

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.

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7. Optical Caracteristics

Ta=25 °C,

$V_{DD}-V_{EE}=Vmax$

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0$) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx		$\theta y=0$	−25	−	25	dgr.	
		θy	Co) 4.0	$\theta x=0$	−10	−	20	dgr.	Note 1
Contrast ratio		Co	$\theta x=\theta y=0$		10	18		−	Note 2
Response time	Rise	τr	$\theta x=\theta y=0$		−	70	120	ms	
	Decay	τd	$\theta x=\theta y=0$		−	80	130	ms	Note 3

Note 1) The viewing angle range is defined as shown Fig. 4.

Note 2) Contrast ratio is defined as follows:

$$Co= \frac{\text{Luminance (brightness) all pixels 'white' at Vmax}}{\text{Luminance (brightness) all pixels 'dark' at Vmax}}$$
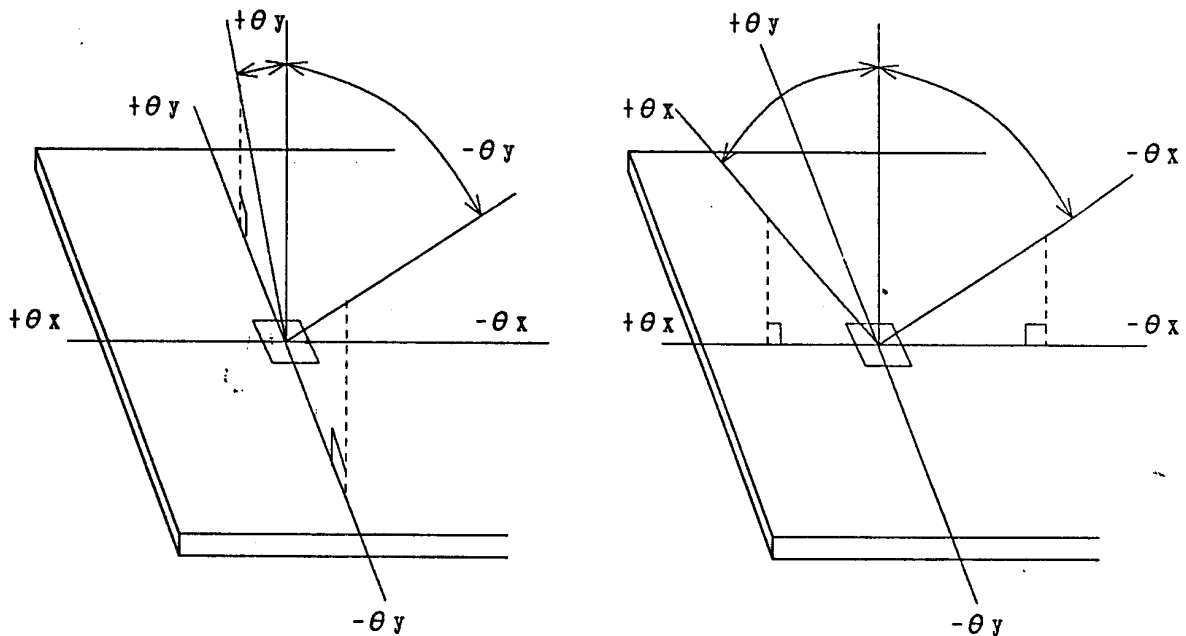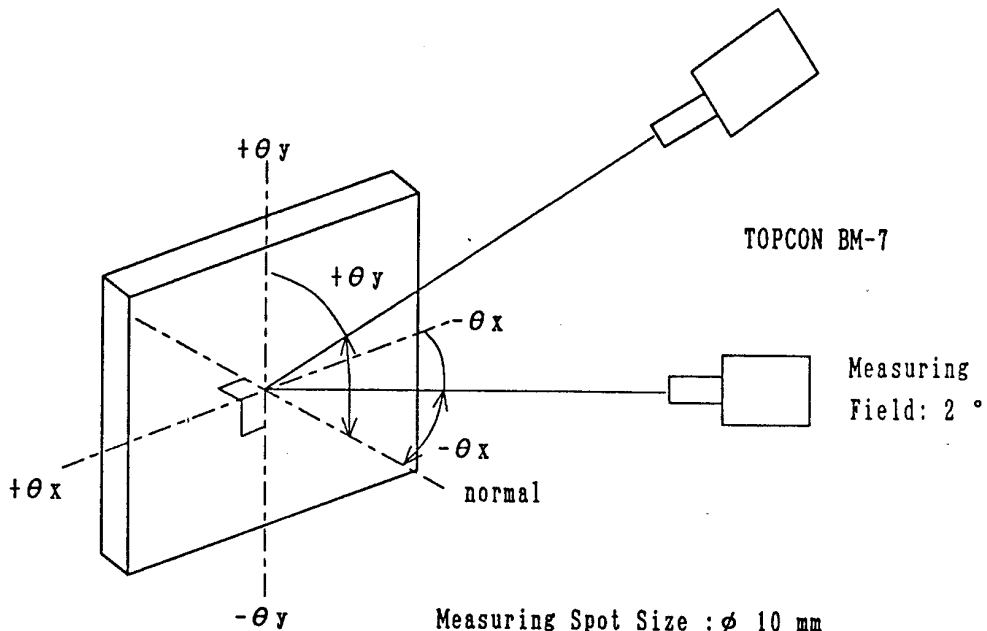
Vmax is defined in Fig. 6.

Fig. 4 Definition of Viewing Angle

Note 4) The response characteristics of photo-detector output are measured as shown in Fig. 7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 8.

TOPCON BM-7

Measuring
Field: 2 °

Measuring Spot Size : φ 10 mm

θ x : Angl from 'normal' to viewing surface
rotated about the horizontal axis.

θ y : Angle from 'normal' to viewing surface
rotated about the vertical axis.

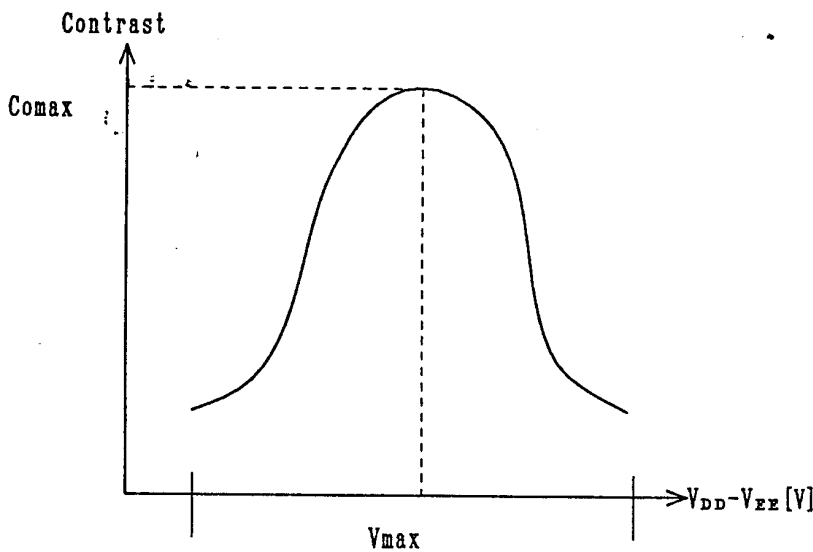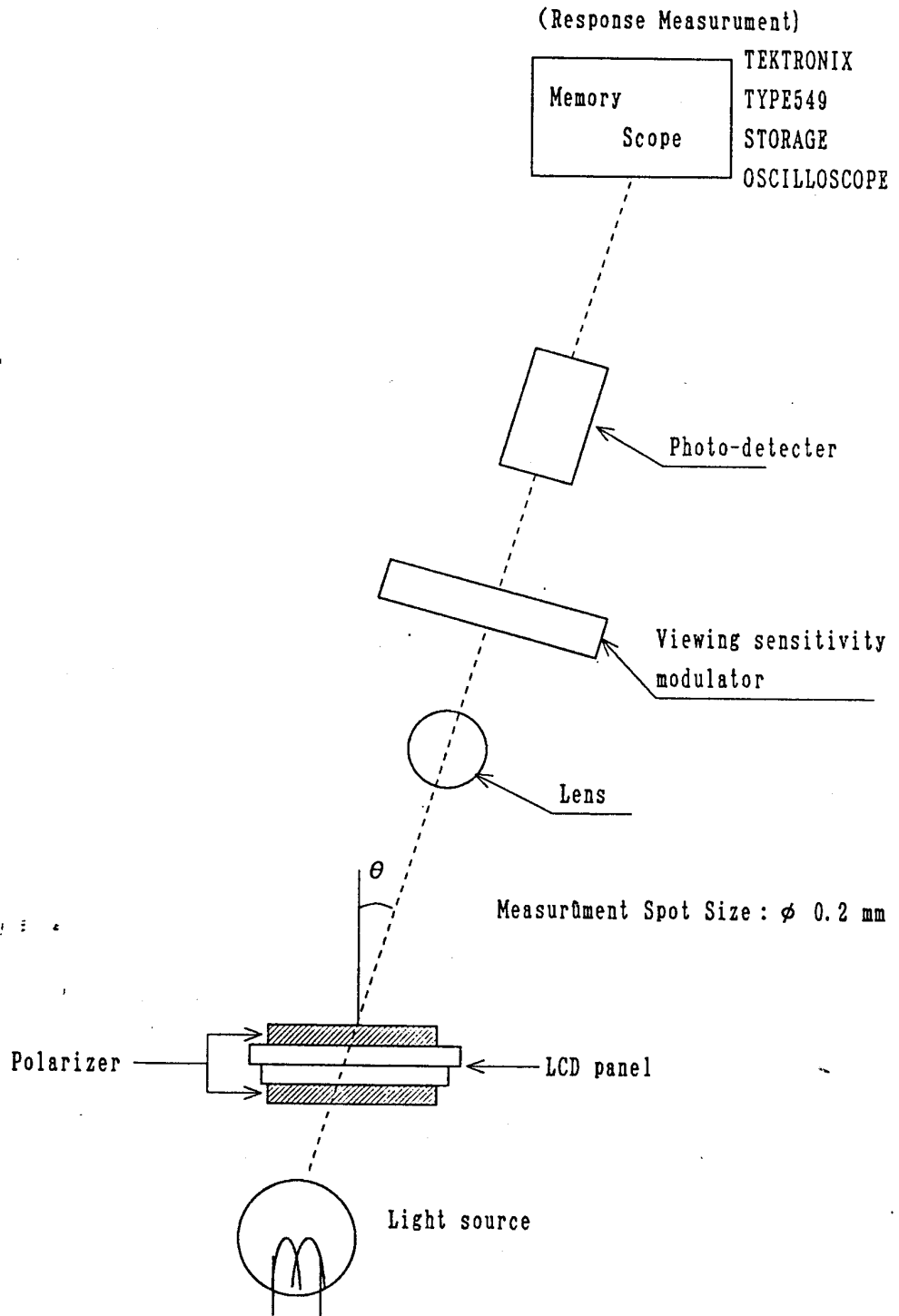Fig. 5 Optical Characteristics Test Method I

Fig. 6 Definition of Vmax

(Response Measurument)

Memory   TEKTRONIX
     Scope   TYPE549
               STORAGE
               OSCILLOSCOPE

Photo-detecter

Viewing sensitivity modulator

Lens

θ

Measurûment Spot Size : ϕ 0.2 mm

Polarizer ———→ ←—— LCD panel

Light source

Fig.7 Optical Characteristics Test Method II

[Drive waveform]

1/240Duty

Non-select
—— waveform ——

Select
waveform ——

Non-select
waveform ——

[Responce waveform]

OUTPUT

100%

90%

10%

τr

τd

τr : Rise time
τd : Decay time
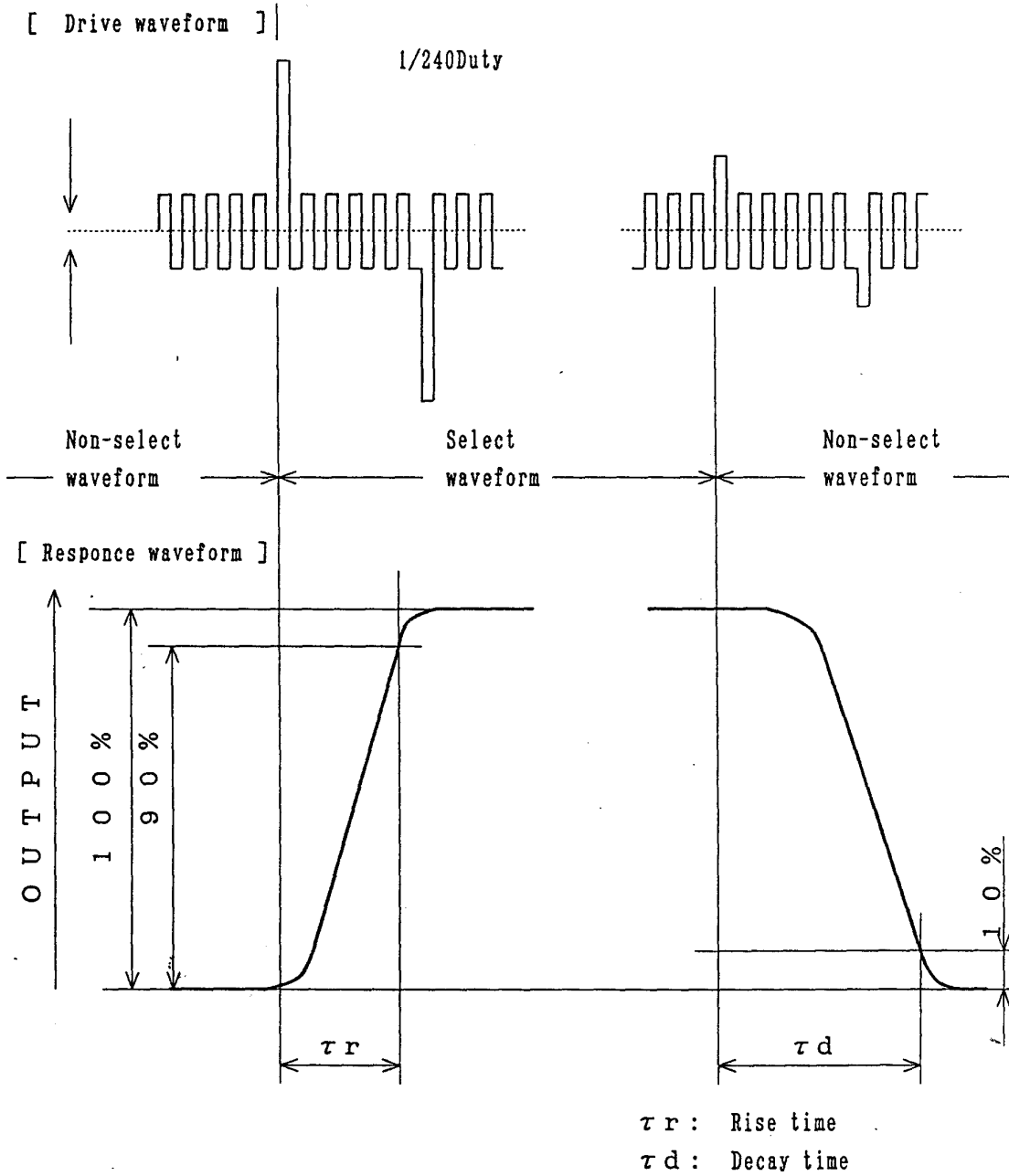
Fig.8 Difinition of Response Time

DU0～DU3
Control DL0～DL3   M
DISP
CP2
CP1
S

C
P
U

LSI

RAM

SEG Drivers (Upper)

C O M D r i v e r s

*1 MG

640×480 LCD PANEL

SEG Drivers (Lower)

Inverter

CCFT
B/L

V_{DD}, V_{SS}, V_{EE}

*2 BG
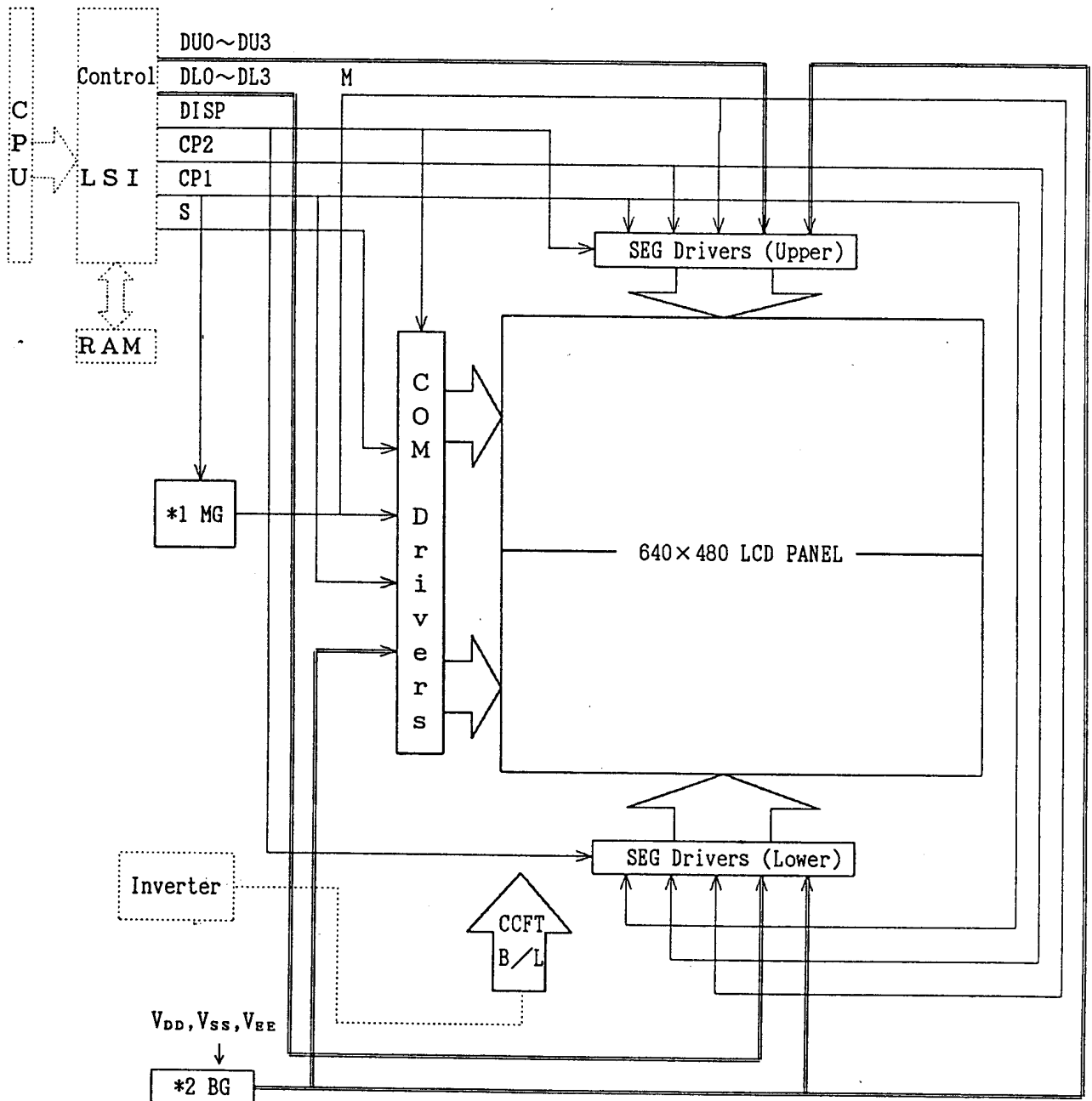
*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR CIRCUIT

Fig.9 Circuit block diagram

Fig.10

SHARP

SPEC No. LC92521A | MODEL No. LM64P10

*3 BEZEL HOLL
CHASSIS
BEZEL
*6.5 CHASSIS HOLL
A-A SECT

BEZEL/DISPLAY POSITION
VIEWING AREA
ACTIVE AREA

VIEWING AREA
ACTIVE AREA

1)TOL(TOLERANCE)X-direction A:2.91±0.8
2)TOL(TOLERANCE)Y-direction B:2.51±0.8
3)OBLIQUITY of DISPLAY AREA (C-D)<0.8

① CCFT CONNECTOR
M63M83-04 (MITSUMI)

② INTER FACE CONNECTOR
(15Pins)
53261-1510 (MOLEX)

UL 3239

Excluded the allowance of deformation.

151×113.4
EFFECTIVE
VIEWING AREA

147.18×110.38
ACTIVE AREA

640×480 DOTS

INTER FACE PIN LAYOUT

PIN#	1	2	3	4	5	6	7	8
SYMBOL	S	CP1	CP2	DISP OFF	VDD	VSS	VEE	DU0
PIN#	9	10	11	12	13	14	15	
SYMBOL	DU1	DU2	DU3	DL0	DL1	DL2	DL3	

LCD.UNIT
OUTLINE
DIMENSIONS

	NAME
LM64K101	
LM64P101	

MODEL
SYMBOL
SCALE
PARTS CODE

SHARP CORPORATION
シャープ株式会社 (本社)

NEW B/W LCD P/T

1993·MAY·28·

DRAWING. No

2-4.3⁺⁰·² CHASSIS HOLL

2-46.5±0.4 CHASSIS HOLL

8. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating (NOTE)

Parameter	Min	Typ	Max	Unit
Brightness	50	70	—	cd/m²

2) Measurement circuit : LM000106 (SHARP) (at IL=5 mArms)

3) Measurement equipment: BM-7 (Tokyo Optical Machinery Corporation)

4) Measurement conditions

4-1 Measurement circuit voltage: DC=12 V at primary side

4-2 LCD: All digits WHITE, VDD=3 V, VDD-VEE=Vmax, DU0~DU3

(refer Fig. 6) DL0~DL3='H' (WHITE)

4-3 Ambient temperature: 25 °C

Measurement shall be executed 30 minutes after turning on.

5. Used lamp: HMBS3A42W130C or FLE-30130(AE)B 1pc

5-1 Ratings (1pc)

Parameter		Max. allowable value
Circuit voltage (VS)	1 000 Vrms MIN	1 500 Vrms
Discharging tube current (IL)	5 mArms TYP	6 mArms ‡
Power comsumption	1.6 W	—
Discharging tube voltage (VL)	320 Vrms TYP	—
Brightness (B)	23 000 cd/m² TYP	—

Within no conductor closed.

‡ It is recommended that IL be not more than 5 mArms so that heat radiation of CCFT backlight may least affect the display quality.

5-2 Operating life

The operating life time is 10 000 hours or more at 5 mA.

(Operating life with LM000106 or equivalent)

The inverter should meet the following conditions;

-Sine, symmetric waveform without spike in positive and negative.

-The voltage at the secondary side is 1,000 Vrms or more.

-Illuminance frequency is from 25 kHz to 45 kHz.

The operating life time is defined as having ended when any of the following conditiones occur; (25±5 °C)

-When the voltage required for initial discharge has reached 900Vrms or when it has reached 10.8 V-DC when used an inverter.

-When the illuminence or quantity of light has decreased to 50 % of the initial value.

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig.11.
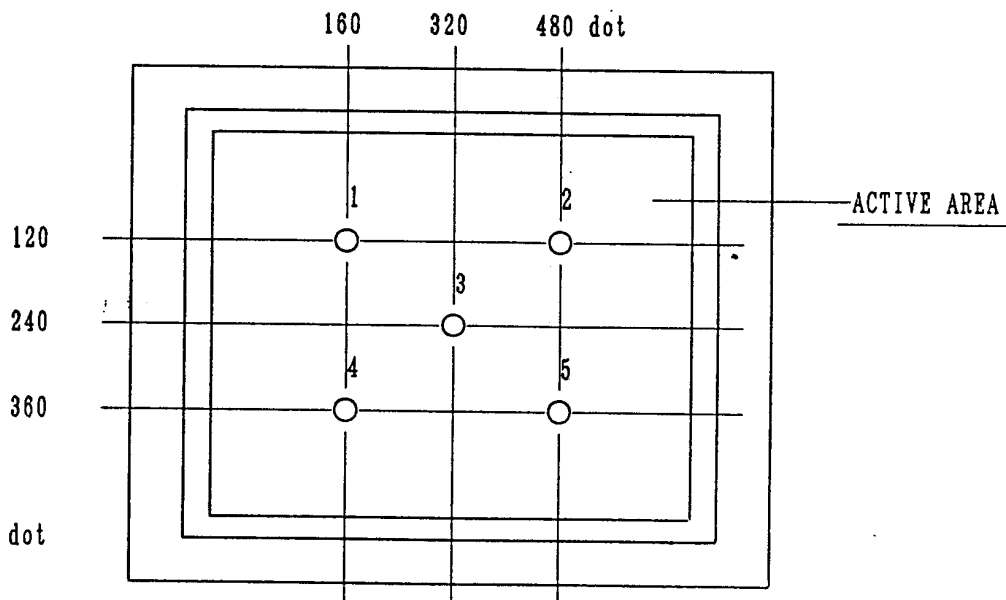
Fig. 11 Measuring points (1~5)

9. Precautions

1) Industrial (Mechanical) design of the product in which this LCD unit will be incorporated must be so made that the viewing angle characteristics of the LCD may be optimized.

This unit's viewing angle is illustrated in Fig. 12.

θ ymin < viewing angle < θ ymax (θ ymin<0 ° θ ymax$\geq$0 °)

(For the specific values of θ ymin, θ ymax, refer to the table 8.)

Please consider the optimum viewing conditions according to the purpose when installing the unit.

θ y=0 ° (Normal line)

+θ y

-θ y

(Panel surface)
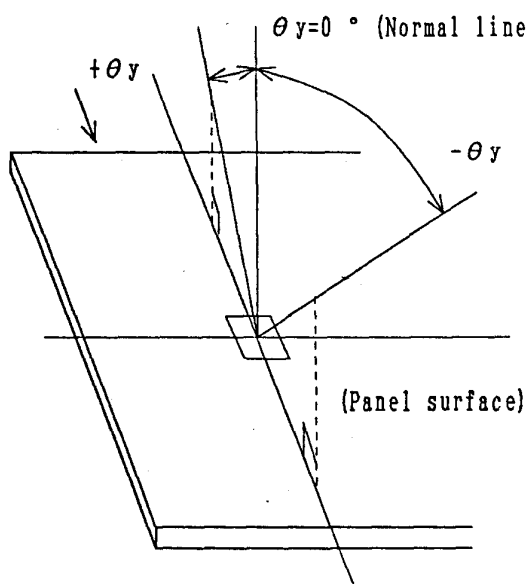
Fig. 12 Dot matrix LCD viewing angle

2) This unit is installed using mounting tabs at the four corners of PCB or bezel.

When installing the unit, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

3) Since the front polarizer is easily damaged, please pay attention not to scratch on its face.

4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc. if remained for a long time.

6) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs from the main system the electrified with static electricity.
   (1) Earth the metallic case of the main system (contact of the unit and main system).
   (2) Insulate the unit and main system by attaching insulating washers made of bakelite or nylon, etc.

8) The unit should be driven according to the specified ratings to avoid malfunction of parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continous application of the signal M. Especially the power ON/OFF sequence shown on next page is strongly recommended to avoid latch-up of driver LSIs and application of DC voltage to LCD panel.

9) Avoid to expose the unit to the direct sun-light, strong ultra-violet light, etc. for a long time.

10) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. As far as possible always store at normal room temperature.

11) Disassembling the LCD unit can cause permanent damege and should be strictly avoided.

Supply voltage sequence condition
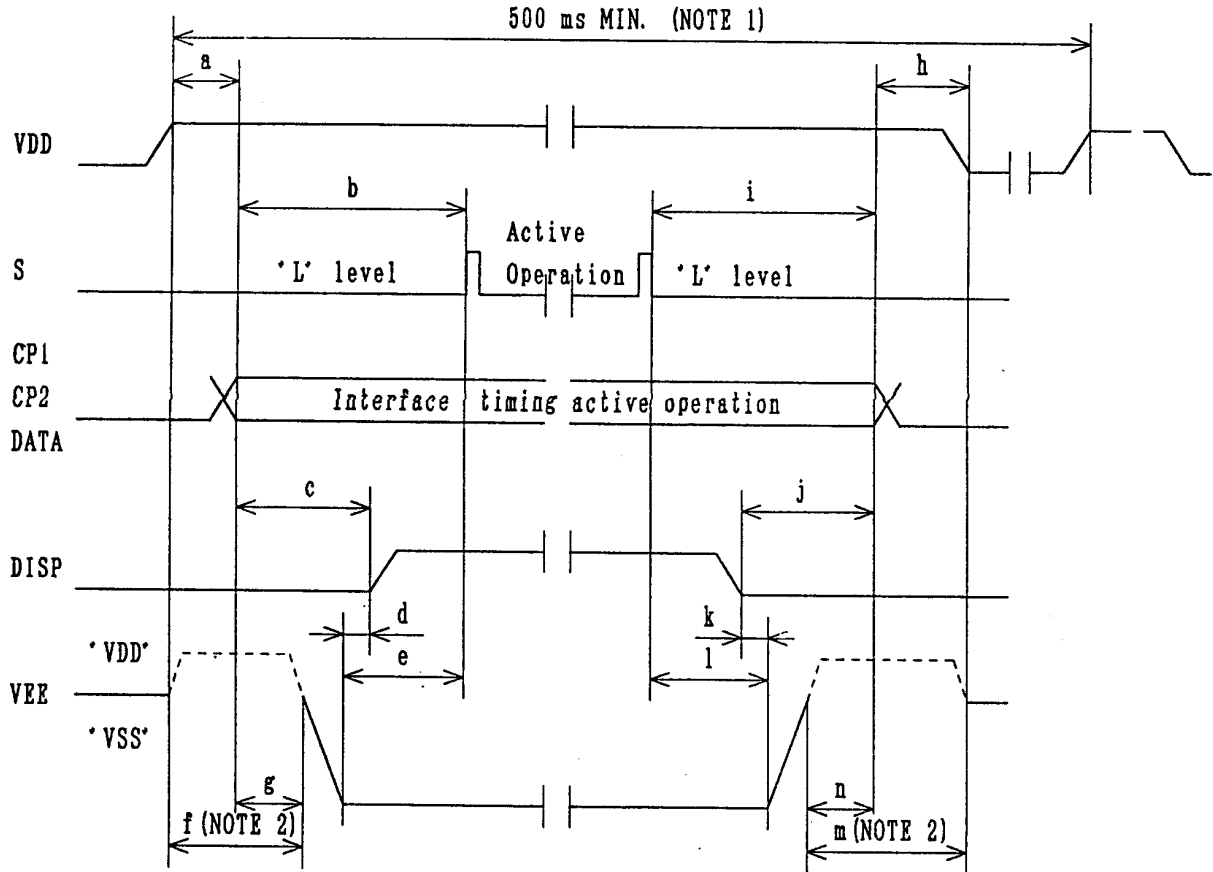
POWER ON		
SYMBOL	With DISP control	Without DISP control
a	0 ms MIN.	0 ms MIN. 20 ms MAX.
b	0 ms MIN.	20 ms MIN.
c	20 ms MIN.	-
d	0 ms MIN.	-
e	-	0 ms MIN.
f	0 ms MIN.	(NOTE2)
g	-	0 ms MIN. 100 ms MAX.

POWER OFF		
SYMBOL	With DISP control	Without DISP control
h	0 ms MIN.	0 ms MIN. 20 ms MAX.
i	0 ms MIN.	20 ms MIN.
j	20 ms MIN.	-
k	0 ms MIN.	-
l	-	0 ms MIN.
m	0 ms MIN.	(NOTE2)
n	-	100 ms MIN.

(Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with
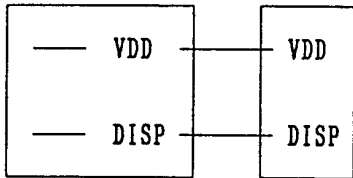above sequence in case of power ON/OFF.

(Note 2) VEE to be set at 'VDD level' or 'open'. VEE should be in accordance with the dotted
line when DISP (display control signal) is not used.

(note3) Connection of DISP (pin. No. 4)
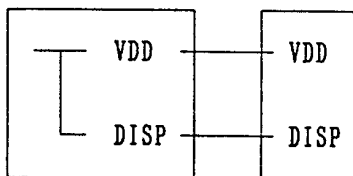
○With DISP control

    Input DISP control signal shown on page. 22

```
┌──────────┐   ┌──────────┐
│ ── VDD ──┼───┼── VDD    │
│          │   │          │
│ ── DISP ─┼───┼── DISP   │
└──────────┘   └──────────┘
```

  Control Circuit   LCD UNIT

○Without DISP control

    DISP to be connected with VDD.

```
┌──────────┐   ┌──────────┐
│ ┬─ VDD ──┼───┼── VDD    │
│ │        │   │          │
│ └─ DISP ─┼───┼── DISP   │
└──────────┘   └──────────┘
```

  Control Circuit   LCD UNIT

10. Lot number

Lot number is shown at the position mentioned in Fig. 13 in accordance with the following numbering rule.
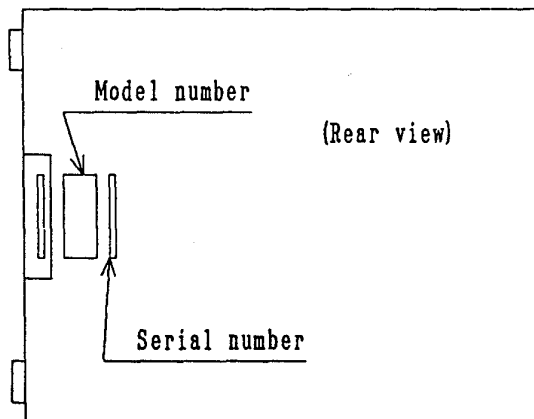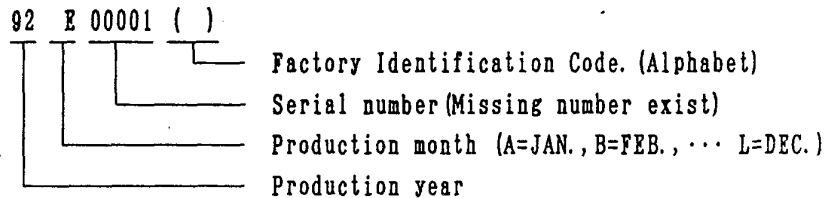
(Example)

92 E 00001 ( )

```
          └──── Factory Identification Code. (Alphabet)
        └────── Serial number(Missing number exist)
     └───────── Production month (A=JAN.,B=FEB.,··· L=DEC.)
  └──────────── Production year
```

Model number

(Rear view)

Serial number

<u>Fig.13</u>

11. Applicable inspection standard

The LCD unit shall meet the following inspection standard
:S-U-012-01

12. This specification,describes display quality in case of no gray scale.
Since display quality can be affected by gray scale methods, display quality
shall be carefully evaluated for the usability of the LCD UNIT in case gray
scale is displayed on the LCD UNIT.

WARNING

DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINES'
HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT
CHANGE POLARIZER COLOR OWING TO GAS.