Memory/Clock Drivers

LM75324 memory driver with decode inputs

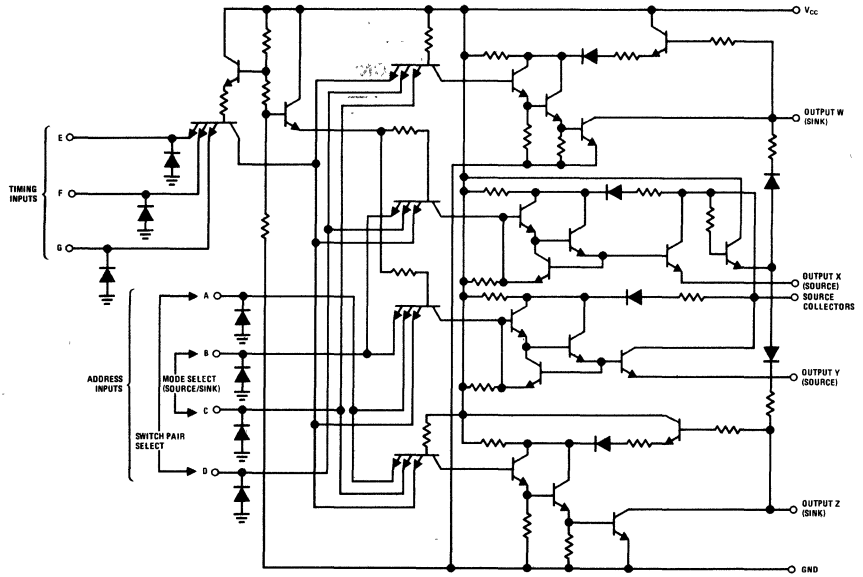
general description

The LM75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X)

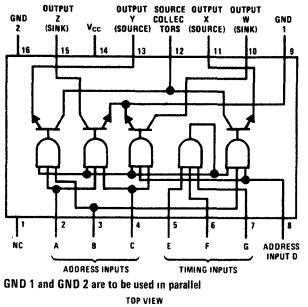
features

- Output capability 400 mA
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- Operation 0°C to +70°C
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



Dual-In-Line Package (J)

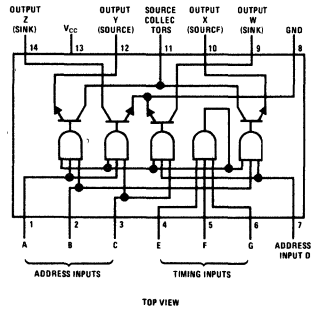


GND 1 and GND 2 are to be used in parallel

TOP VIEW

Order Number LM75324J
See Package 17

Dual-In-Line Package (N)



TOP VIEW

Order Number LM75324N
See Package 22

absolute maximum ratings

Supply Voltage V_{CC} (Note 1)	17V
Input Voltage (Note 2)	5.5V
Operating Case Temperature Range	0°C to +70°C
Continuous Total Power Dissipation at (or Below) +70°C Case Temperature	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Required to Insure Logical "1" At Any Input ($V_{IN(1)}$)	Figure 1	3.5			V
Input Voltage Required to Insure Logical "0" At Any Input ($V_{IN(0)}$)	Figure 1			0.8	V
Logical "1" Level Address Input Current ($I_{IN(1)}$)	V_{IN} = 5V, Figure 1			200	μA
Logical "1" Level Timing Input Current ($I_{IN(1)}$)	V_{IN} = 5V, Figure 1			100	μA
Logical "0" Level Address Input Current ($I_{IN(0)}$)	V_{IN} = 0V, Figure 1			−6	mA
Logical "0" Level Timing Input Current ($I_{IN(0)}$)	V_{IN} = 0V, Figure 1			−12	mA
Sink Saturation Voltage (V_{sat})	$I_{SINK} \simeq$ 420 mA, R_L = 53Ω, Figure 2		0.75	0.85	V
Source Saturation Voltage (V_{sat})	$I_{SOURCE} \simeq$ −420 mA, R_L = 47.5Ω, Figure 2		0.75	0.85	V
Output Reverse Current (Off State) (I_{OFF})	V_{IN} = 0V, Figure 1		125	200	μA
Supply Current, All Sources and Sinks Off (I_{CC})	V_{IN} = 0V, Figure 3		12.5	15	mA
Supply Current, Either Sink Selected (I_{CC})	Figure 4		30	40	mA
Supply Current, Either Source Selected (I_{CC})	Figure 4		25	35	mA
Input Clamp Voltage (V_1)	I_{IN} = −12 mA, T_A = 25°C			−1 5	V

ac switching characteristics (V_{CC} = 14V, T_C = 25°C)

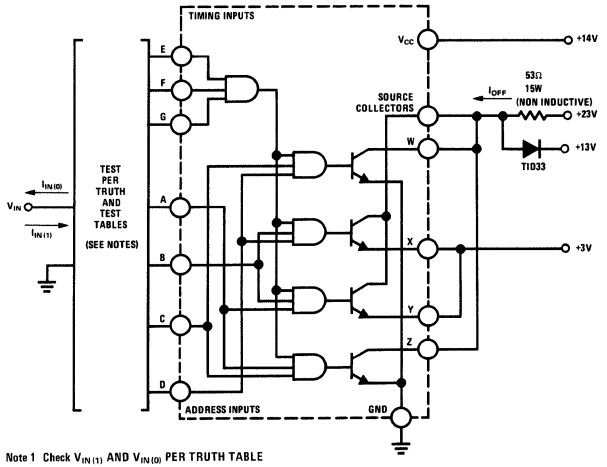
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" Level, Source Output (t_{pd1})	R_{L1} = 53Ω, R_{L2} = 500Ω, C_L = 20 pF, Figure 5			90	ns
Propagation Delay Time to Logical "0" Level, Source Output (t_{pd0})				50	ns
Propagation Delay Time to Logical "1" Level, Sink Output (t_{pd1})	R_L = 53Ω, C_L = 20 pF, Figure 6			110	ns
Propagation Delay Time to Logical "0" Level, Sink Output (t_{pd0})				40	ns
Sink Storage Time (t_s)				70	ns

Note 1: Voltage values are with respect to network ground terminal.
Note 2: Input signals must be zero or positive with respect to network ground terminal.

truth table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

test circuits and switching time waveforms



Note 1 Check $V_{IN(1)}$ AND $V_{IN(0)}$ PER TRUTH TABLE

Note 2 Measure $I_{IN(0)}$ per test table

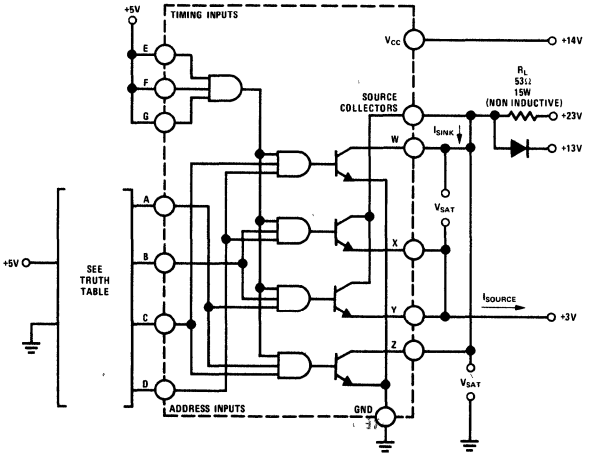
Note 3 When measuring $I_{IN(1)}$, all other inputs are at GND Each input is tested separately

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$, and I_{OFF}

test circuits and switching time waveforms (con't)



Note This parameter must be measured using pulse techniques
t_P = 500 ns, duty cycle ≤ 1%

FIGURE 2. $V_{(SAT)}$

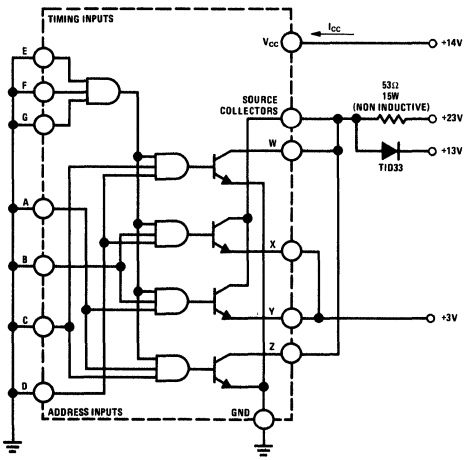
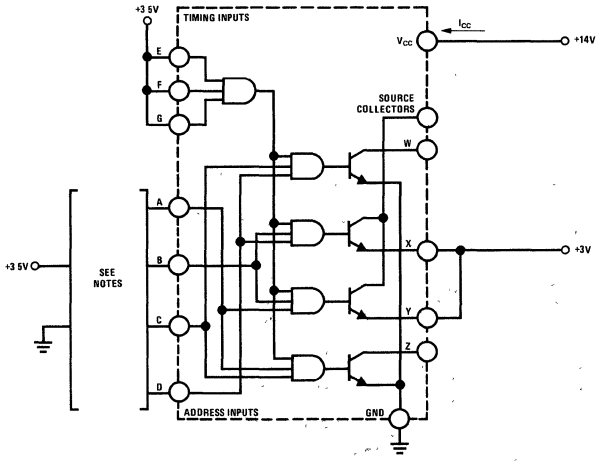


FIGURE 3. I_{CC} (All Outputs Off)

test circuits and switching time waveforms (con't)



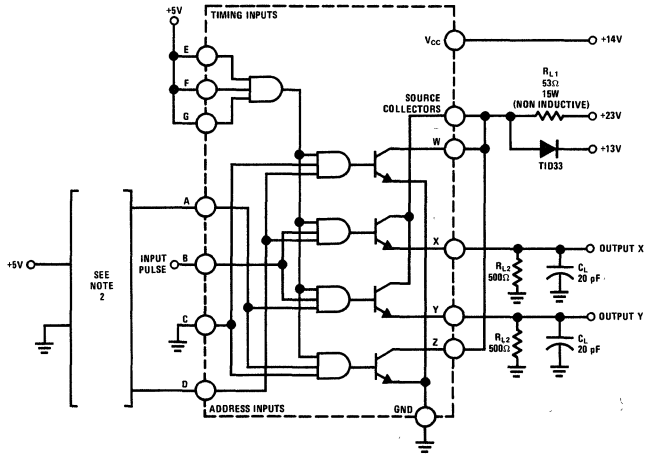
Note 1 GND A and B, apply +3.5V to C and D, and measure I_{CC} (output W is on)

Note 2 GND B and D, apply +3.5V to A and C, and measure I_{CC} (output Z is on)

Note 3 GND A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on)

Note 4 GND C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on)

FIGURE 4. I_{CC} (One Output On)



Note 1 The input waveform is supplied by a generator with the following characteristics $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$

Note 2 When measuring delay times at output X, apply +5V to input D, and GND A. When measuring delay times at output Y, apply +5V to input A, and GND D

Note 3 C_L includes probe and jig capacitance

Note 4 Unless otherwise noted all resistors are 0.5W

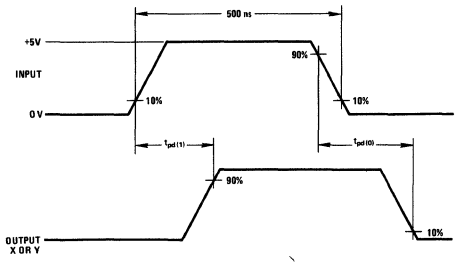
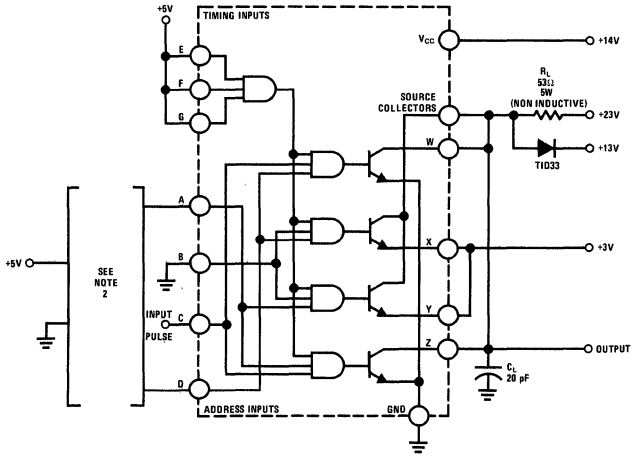


FIGURE 5. Source-Output Switching Times

test circuits and switching time waveforms (con't)



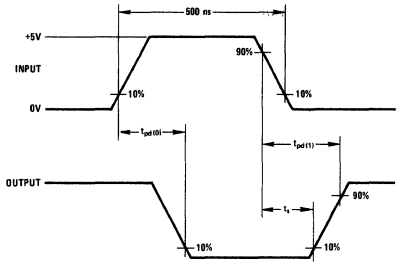


FIGURE 6. Sink-Output Switching Times

Note 1 The input waveform is supplied by a generator with the following characteristics. $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2 When measuring delay times at output W, apply +5V to input D, and GND A When measuring delay times at output Z, apply +5V to input A, and GND D

Note 3 C_L includes probe and jig capacitance