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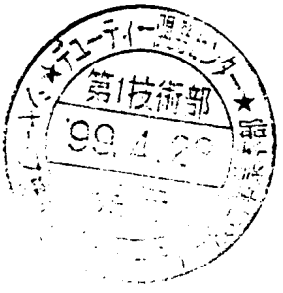
		REPREZNTATIVE DIVISION ENGINEERING DEPARTMENT I DUTY LCD DEVELOPMENT CENTER DUTY LIQUID CRYSTAL DISPLAY GROUP

SPECIFICATION

DEVICE SPECIFICATION for
Passive Matrix Monochrome LCD Module
(640 × 240 dots)

Model No.

LM7MS623



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SHARP

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○Precautions

1) Industrial (Mechanical) design of the product in which this LCD module will be incorporated must be made so that the viewing angle characteristics of the LCD may be optimized.

This module's viewing angle is illustrated in Fig.1.

θ y MIN. < viewing angle < θ y MAX.

(For the specific values of θ y MIN., and θ y MAX., refer to the table 8)

Please consider the optimum viewing conditions according to the purpose when installing the module.

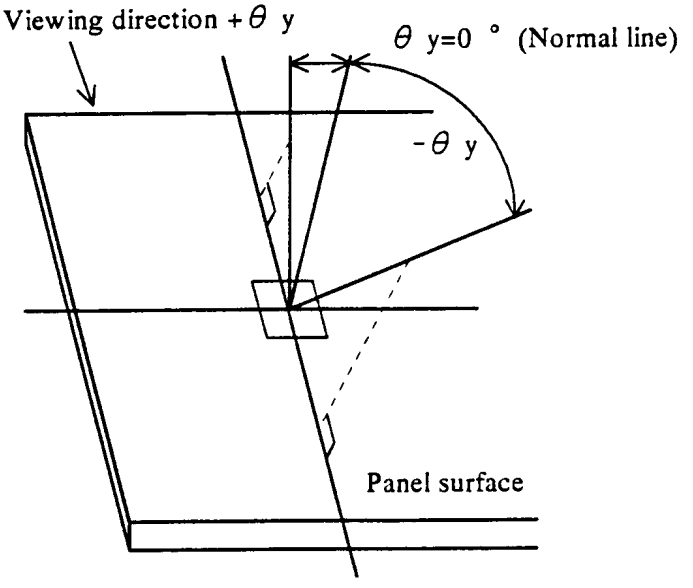


Fig.1 Definition of viewing angle

2) This module should be installed using mounting holes at the two corners of modules.
When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.
It is recommended to use a transparent acrylic resin board or other type of protective panel on the surface of the LCD module to protect the polarizer, LCD panel, etc..

4) If the surface of the LCD panel is required to be cleaned, wipe it swiftly with cotton or other soft cloth.
If it is not still clear completely, blow on and wipe it.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc., if it remained for a long time.

6) Since LCD is made of glass substrate, dropping the module or banging it against hard objects may cause cracking or fragmentation.

7) Since CMOS LSIs are equipped in this module, following countermeasures must be taken to avoid electrostatics charge.

1.Operator

Electrostatic shielding clothes shall be had because it is feared that the static electricity is electrified to human body in case that operator have a insulating garment.

2.Equipment

There is a possibility that the static electricity is charged to equipment which have a function of peeling or mechanism of friction(EX: Conveyer, soldering iron, working table), so the countermeasure(electrostatic earth:$1\times10^{8}\ \Omega$) should be made.

3.Floor

Floor is a important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor,so the countermeasure(electrostatic earth:$1\times10^{8}\ \Omega$) should be made.

4.Humidity

Humidity of working room may lower electrostatics generating material's resistance and have something to prevent electrifying. So, humidity should be kept over 50% because humidity less than 50 % may increase material's electrostatic earth resistance and it become easy to electrify.

5.Transportation/storage

The measure should be made for storage materials because there is a possibility that the static electriicity, which electrify to human body or storage materials like container by friction or peeling, cause the dielectric charge.

6.Others

The laminator is attached on the surface of LCD module to prevent from scratches, fouling and dust. It should be peeled off unhurriedly with using static eliminator.

And also, static eliminator should be installed to prevent LCD module from electrifying at assembling line.

8) Don't use any materials which emit gas from epoxy resin(amines' hardener) and silicon adhesive agent(dealcohol or deoxym) to prevent change polorizer color owing to gas.

9) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

10) If stored at temperatures under specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. Therefore, the module should be always stored at normal room temperature.

11) Disassembling the LCD module can cause permanent damage and should be strictly avoided.

12) Do not use touch TCP/LCD connection area to prevent interconnection breakdown.

13) Do not apply organic solvent to TCP/LCD connection area where organic materials are used.

14) This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of LCD module in case gray scale is displayed on the LCD module.

15) The module should be driven according to the specified ratings to avoid permanent damage.
DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on Page 22 should be kept to avoid latch-up of drive LSI and application of DC voltage to LCD panel

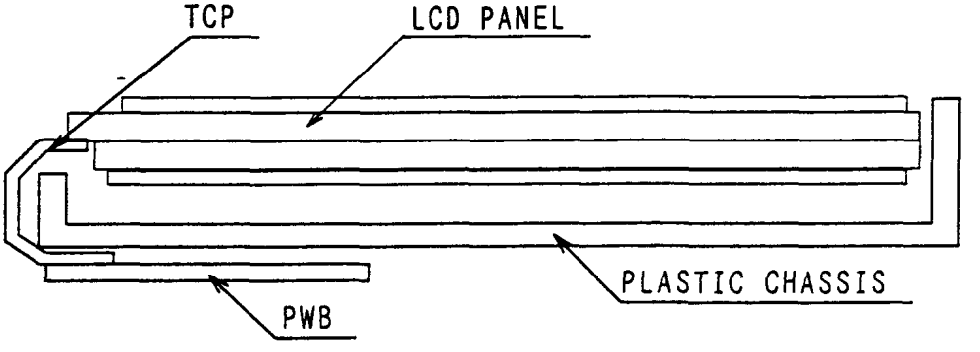
○Contents

1.Application

This data sheet is to introduce the specification of LM7MS623, passive Matrix type LCD module.

2.Construction and Outline

Construction: 640×240 dots display module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis.



Outline :See Fig. 14,15

Connection :See Fig. 15 and Table 6-1

3.Mechanical Specification

Table1

Parameter	Specifications	Unit
Outline dimensions	172.7 (W)×76.2 (H)×5.5 MAX (D) *1	mm
Active area	153.59(W)×57.59 (H)	mm
Display format	640 (W)×240 (H) Dots	-
Dot size	0.23×0.23	mm
Dot spacing	0.01	mm
*2 Dot color	Black *3	-
*2 Base color	White *3	-
Weight	Approx. 75	g

*1 Excluded the mounting portions and connectors.
Flatness is 1mmMAX for each specified thickness.

*2 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*3 Positive-type display
Display data "H" : Dots ON → Black
Display data "L" : Dots OFF → White

4.Absolute Maximum Ratings

4-1.Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage(Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 ℃
Supply voltage(LCD drive)	V_{EE}-V_{SS}	0	32.0	V	Ta=25 ℃
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25 ℃

4-2.Environment Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-30 ℃	+80 ℃	-10 ℃	+60℃	Note 3)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		
Shock					

Note 1) Ta≦40 ℃.....95 % RH Max.

Ta＞40 ℃.....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

The temperature gradient for storage condition and packing condition shall be less than 50℃/hrs. And no dew condensation.

Note 2) Since this module does not have enough mounting mechanism , it is impossible to conduct vibration and shock test at SHARP side. Therefore ,assemble it to your cabinet and then these test shall be conducted to be satisfied the necessary condition in according with ① and ② condition (Non operating).

① Vibration test

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	-	9.8 m/s^2
Vibration width	0.075 mm	-
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

② Shock test

Acceleration : 490 m/s^2

Pulse width : 11 ms

3 times for each directions of ±X/±Y/±Z

Note 3) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

5.Electrical Specifications

5-1.Electrical characteristics

Table 5-1

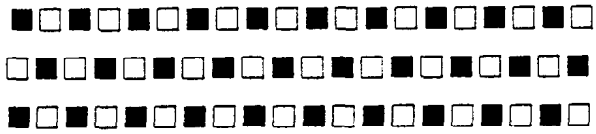
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS	Ta=-10~60℃	3	3.3	5.25	V
Supply voltage (LCD) Note 1)	VEE-VSS	Ta=-10℃	22.1	24.5	27.0	V
		Ta=25℃	18.8	20.9	23.0	V
		Ta=60℃	16.7	18.5	20.4	V
Input signal voltage	VIL	"L" level	0	-	0.2VDD	V
	VIH	"H" level	0.8VDD	-	VDD	V
Input leakage current	IIL	"L" level	-	-	20	μA
	IIH	"H" level	-20	-	-	μA
Supply current (Logic)	IDD	Note 2)	-	0.25	0.35	mA
		Note 3)	-	0.3	0.4	mA
Supply current (LCD drive)	IEE	Note 2)	-	0.7	0.82	mA
		Note 3)		3.8	4.5	mA
Power consumption	Pd	Note 2)	-	15.5	18.5	mW
		Note 3)	-	80	95	mW

Note 1) The voltage [VEE-VSS] for obtaining maximum contrast is different in individual modules.
And it change because of temperature.
Therefor it is needed adjusting the voltage [VEE-VSS] for obtain to proper contrast.

Note 2) Under the following condition.;
VDD-VSS=3.3V, VEE-VSS=20.9V, Frame frequency=70Hz, Ta=25℃
Display pattern=Full dots ON

Note 3) Under the following condition.;
VDD-VSS=3.3V, VEE-VSS=20.9V, Frame frequency=70Hz, Ta=25℃

Display pattern



5-2.Interface signals

Table 6-1 CN3

Pin No.	Symbol	Description	Level
1	D0	Display data signal	"H"(ON), "L"(OFF)
2	D1		
3	D2		
4	D3		
5	LP(CP1)	Data input latch signal	"H"→"L"
6	CLK(CP2)	Data input clock signal	"H"→"L"
7	DISP OFF	Display Control signal	"H"(Display on) "L"(Display off)
8	FRAME(S)	Scan start-up signal	"H"
9	DF(M)	LCD drive waveform alternating signal	H/L
10	VDD	Power supply for Logic	+3.3V
11	VDD		
12	VEE	Power supply for LCD drive	(+16~27V)
13	NC	-	-
14	NC		
15	VSS	Ground potential	-
16	VSS		
17	A	Extra signals (for Logic level only) Note 1)	-
18	B		
19	C	Extra signals (for Touch panel signal) Note 1)	-
20	D		
21	E		
22	F		

Note 1) these signals are not concerned with driving the LCD module.

Table 6-2 CN2

Pin No.	Symbol	Description	Note
1	C	Extra signals (for Touch panel signal)	-
2	D		
3	E		
4	F		

Table 6-3 CN1

Pin No	Symbol	Description	Note
1	A	Extra signals (for Logic level only)	-
2	B		

Used connector CN1 : SM02B-SSR-H [JST]

CN2 : 04 6227 004 100 800 [KYOCERA ELCO]

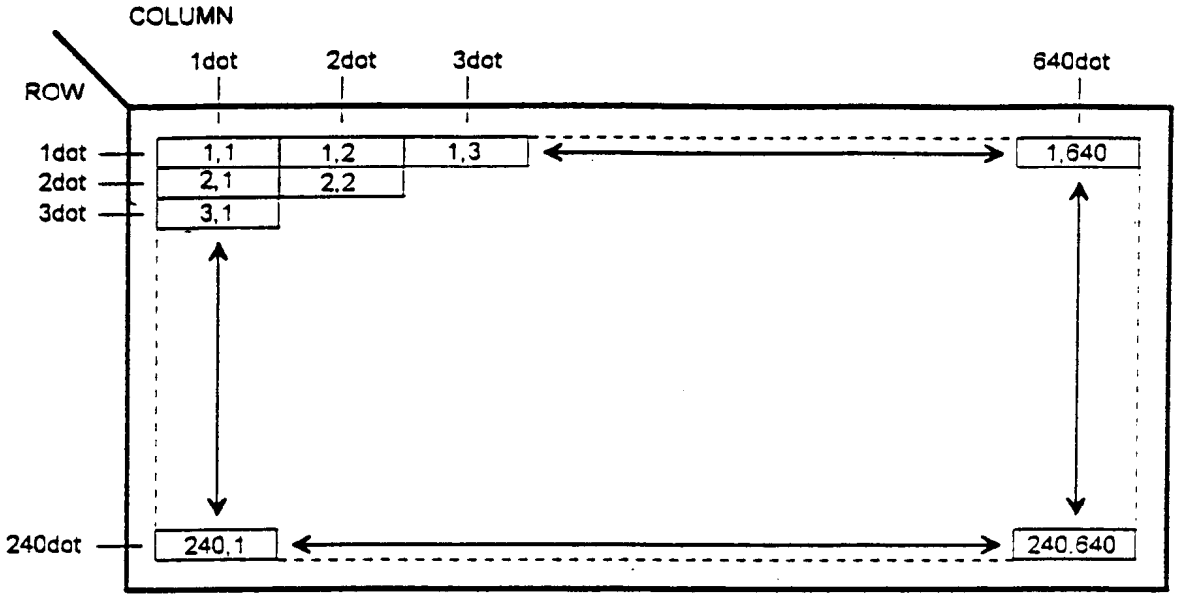
CN3 : 0.5mm pitch ,FPC

Correspondable connector CN1 : 02SSR-32H [JST]

CN2 :1.0mm pitch ,FPC/FFC

CN3 :FH12-22S-0.5SH [HIROSE]

Except above connector shall be out of guaranty.



Note) 1,2 means 1st row 2nd column dot.

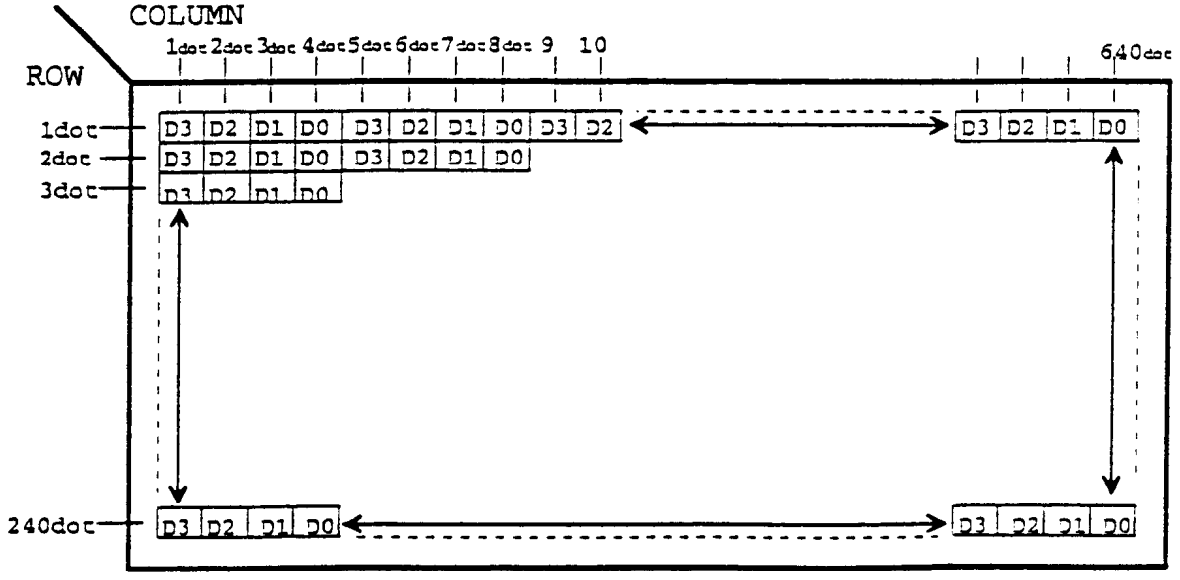


Fig.1 Dot chart of display area

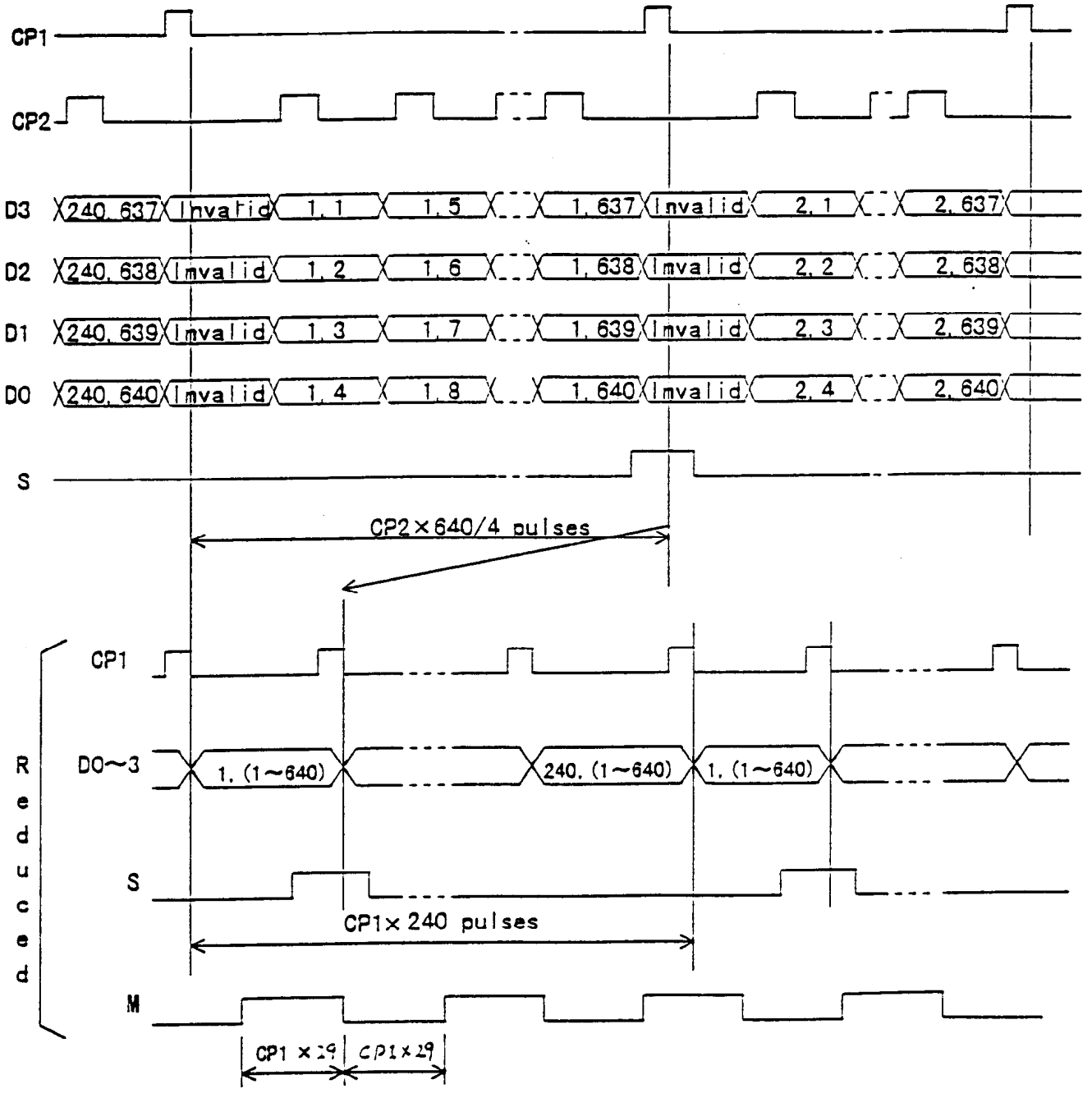


Fig. 2 Data input timing chart

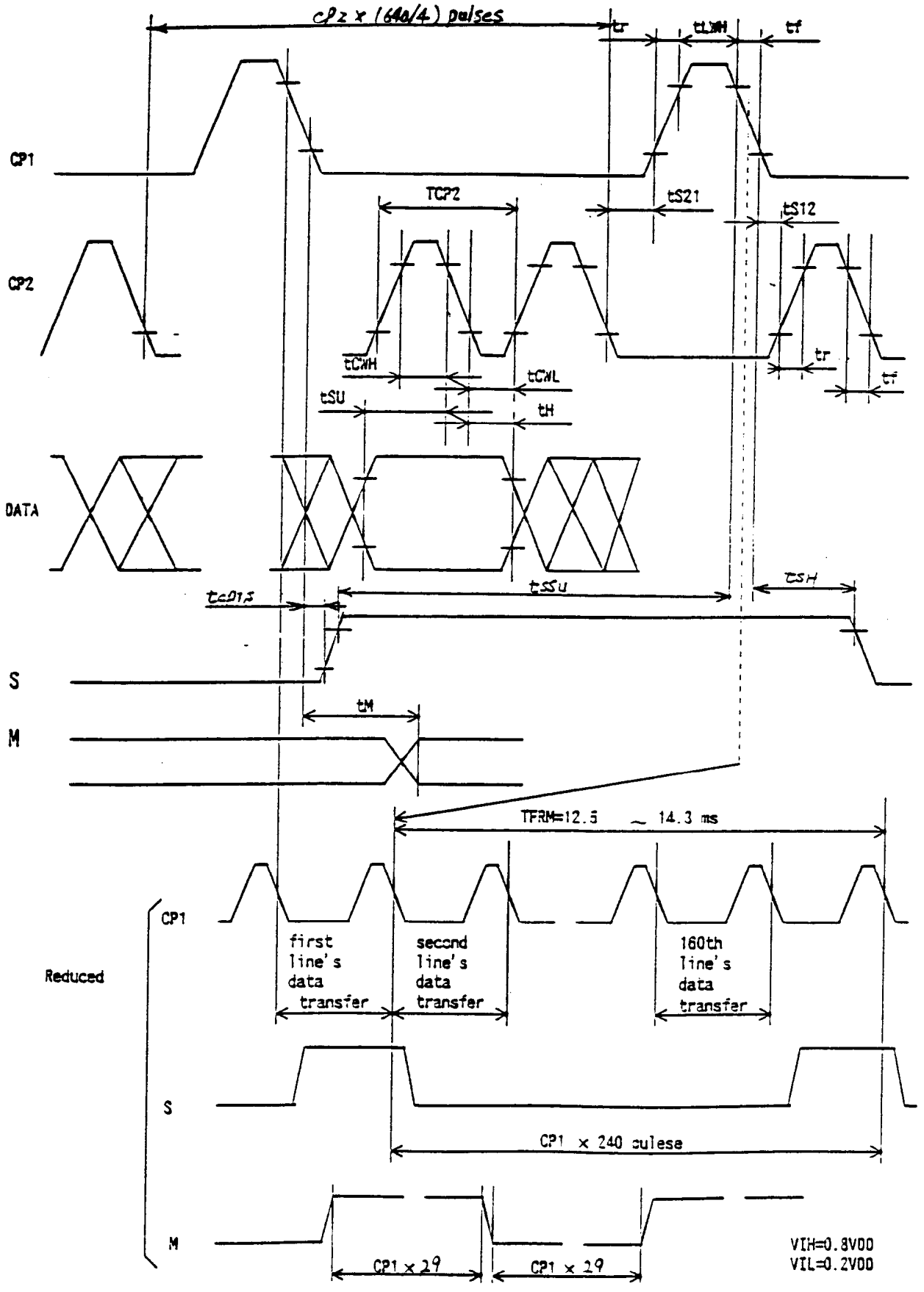


Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	TFRM	12.5	-	14.3	ms
CP2 clock cycle	TCP2	153	-	-	ns
"H" level clock width	tCWH	100		-	ns
"L" level clock width	tCWL	100	-	-	ns
"H" level latch clock width	tLWH	100	-	-	ns
Data set up time	tSU	80	-	-	ns
Data hold time	tH	80	-	-	ns
CP2 ↑ clock allowance time from CP1 ↓	tS12	0	-	-	ns
CP1 ↑ clock allowance time from CP2 ↓	tS21	0	-	-	ns
Input signal rise/fall time (Note2)	tr,tf	-	-	trf	ns
S signal data set up time	tSSU	100	-	-	ns
S signal data hold time	tSH	100	-	-	ns
S ↑ clock allowance time from CP1 ↓	tcp1s	100	-	-	ns
M delay time	tM	-	-	50	ns

Note 1)

Owing to the characteristics of LCD module, "shadowing" will become more eminent as frame frequency goes up, flicker will become more eminent as frame frequency goes down. So it is recommended that the module should be driven according to the specified limit.

Note 2)

trf = 50 in case t_{CT} = (TCP2- tCWH - tCWL) / 2 ≧ 50

trf = t_{CT} in case t_{CT} = (TCP2 - tCWH - tCWL) / 2 < 50

6. Module Driving Method

6-1. Circuit configuration

Fig.11 shows the block diagram of the module's circuitry.

6-2. Display face configuration

The display consists of 640×240 dots as shown in Fig. 2.

The interface is single panel with single drive to be driven at 1/240 duty ratio.

6-3. Input data and control signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Display data which are externally divided into data for each row (640 dots) will be sequentially transferred in the form of 4- bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When input of one row (640 dots) is completed, the data will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal (CP1) then, the corresponding drive signals will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (S) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the 1st rows of data are being displayed, the 2nd row of data are entered. When 640 dots of data have been transferred, they latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.
Then data input proceeds to the next display frame.

Scan start -up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel. drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up as the operating frequency CP2. Thanks to the 4 lines of shift registers to reduce the data transfer speed CP2 Thanks to the LSI, the power consumption of the display module will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of D0 -3.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right next side is selected when data of 160 dot (40CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

Thus data input will be made through 4-bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in fig. 3 and Table 7.

7.Optical Characteristics

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction($\theta x = \theta y = 0°$) will be MAX..

Ta=25℃, Frame frequency=70Hz

Table 8

1/240DUTY, V_{DD}-V_{SS} = 3.3 V, V_{EE}-V_{SS} = Vmax

Parameter		Symbol	Condition			MIN.	TYP.	MAX.	Unit	Remark	
Viewing angle range		θx	Co≧2	$\theta y=0°$	$\theta x \geqq 0°$	20	-	-	dgr.	Note 1)	
					$\theta x < 0°$	-	-	-20	dgr.		
		θy		$\theta x=0°$	$\theta y \geqq 0°$	20	-	-	dgr.		
					$\theta y < 0°$	-	-	-25	dgr.		
Contrast ratio		Co	$\theta x = \theta y = 0°$			4	6	-	-	Note2)	Fig.5
						8	10	-	-		Fig.8
Response time	Rise	τ r	$\theta x = \theta y = 0°$			-	190	240	ms	Note3)	
	Decay	τ d	$\theta x = \theta y = 0°$			-	220	270	ms		

Note 1) The viewing angle range is defined as shown Fig.4.

Measureing spot size : Φ 10mm

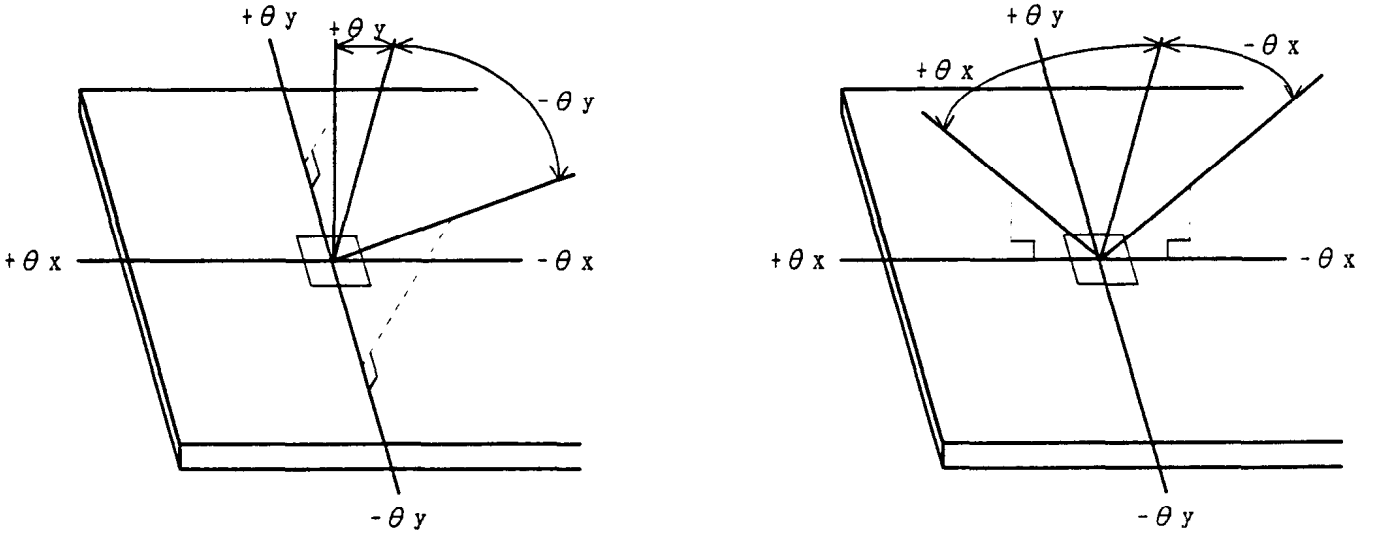


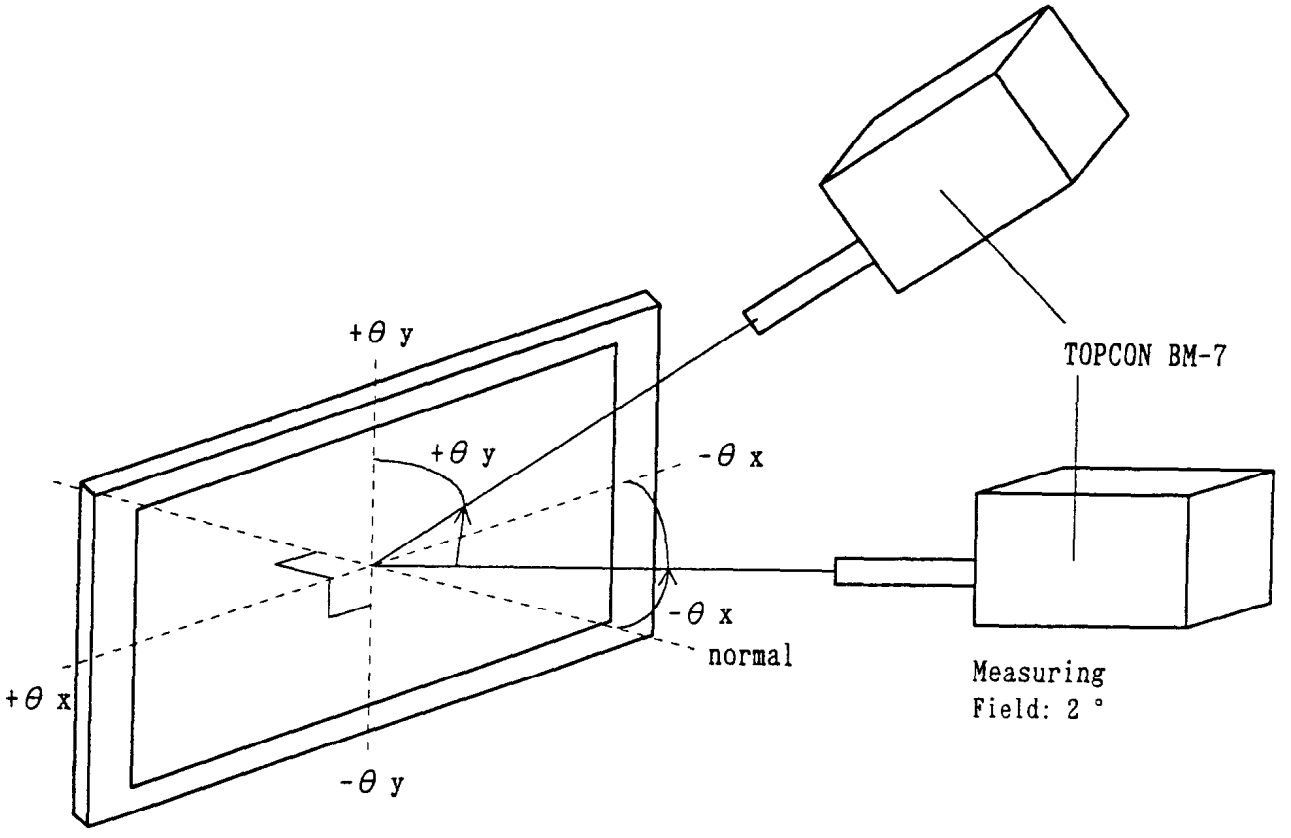
Fig.4 Definition of Viewing Angle

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixes "White" at Vmax}}{\text{Luminance(brightness) all pixes "dark " at Vmax}}$$

Vmax is defined in Fig.6.

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.9, assuming that input signals are applied so as to select and deselect the dot to be measured, in the optical characteristics test method shown in Fig.10.



Measuring Spot Size : ϕ 10 mm

θ x : Angle from "normal" to viewing surface rotated about the horizontal axis.

θ y : Angle from "normal" to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Method I

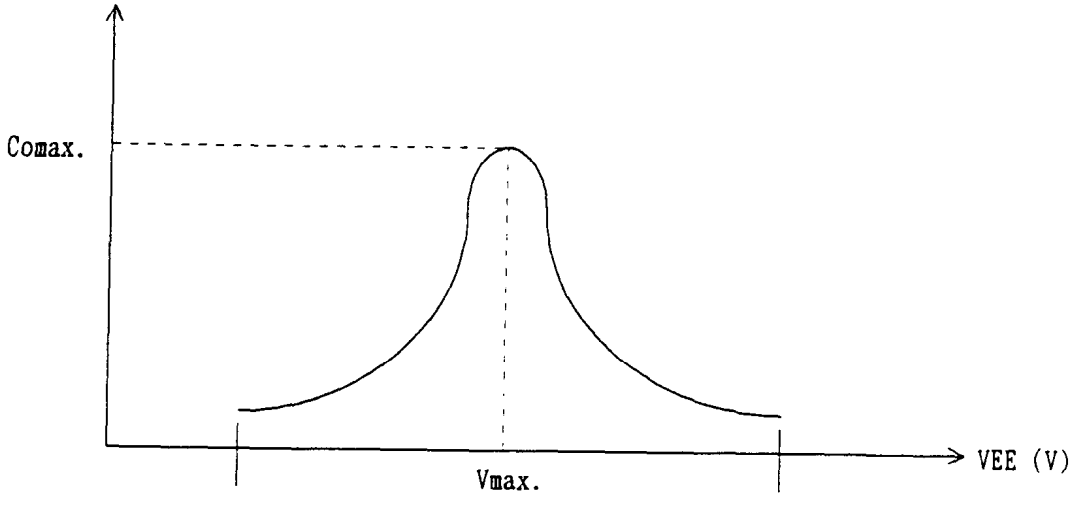


Fig.6 Definition of Vmax

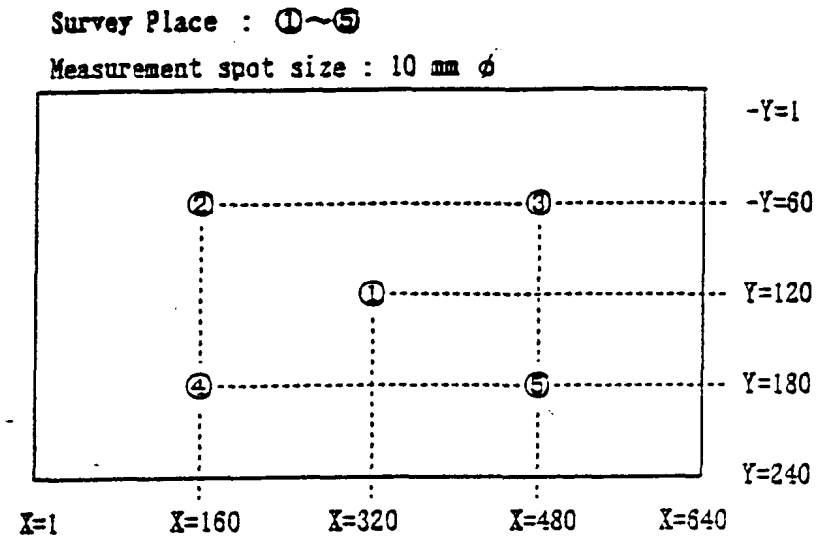


Fig.7 Measuring points(1~5)

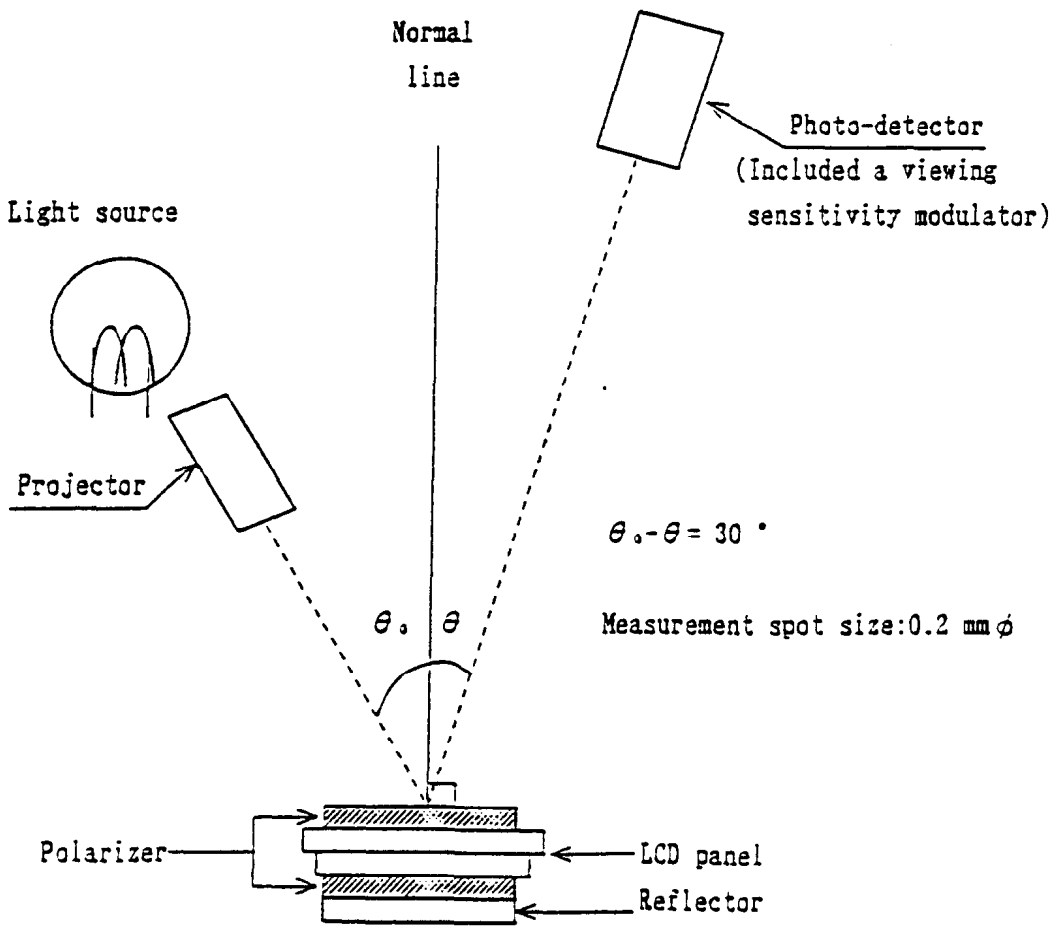
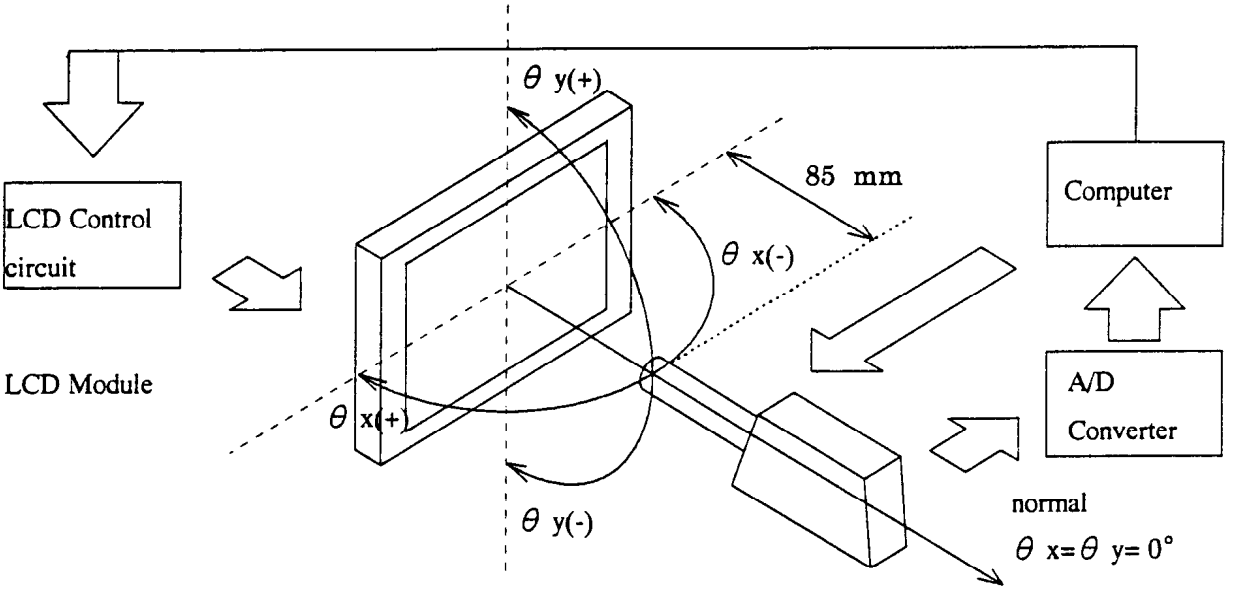


Fig. 8 Optical Characteristics Test Method Ⅱ

(Response Measurement)

Ta = 25 ℃

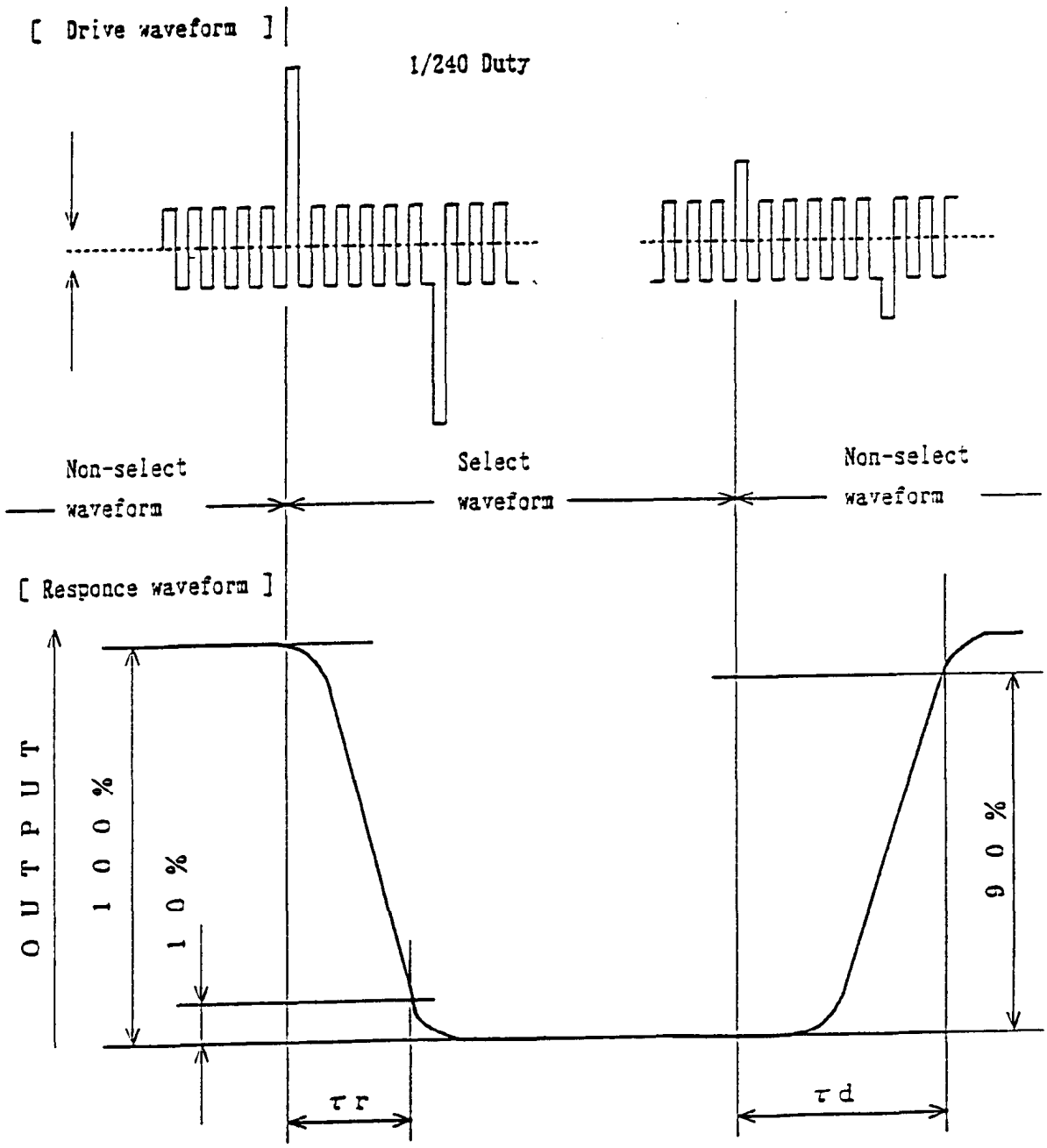
In dark room



TOPCON BM7 + quartz fiber

(Measuring spot size : ϕ 10 mm, Measuring Field : 2 °)

Fig. 9 Optical Characteristics Test Method I



τ r : Rise time

τ d : Decay time

Fig.10 Difinition of Response Time

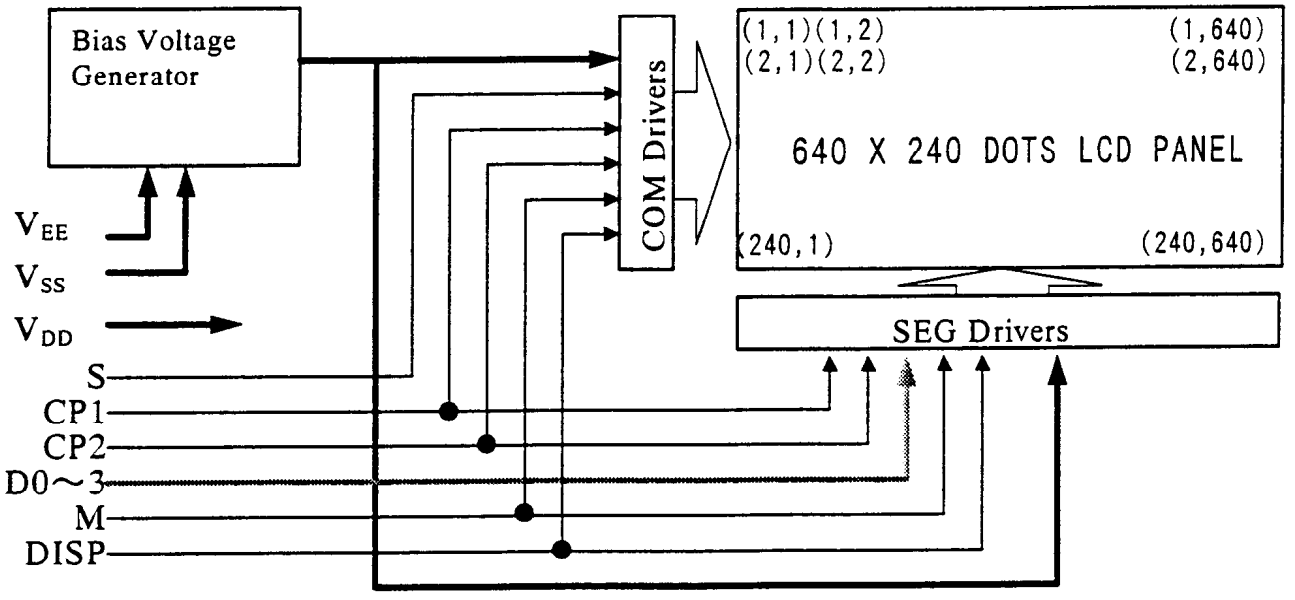


Fig.11 Circuit block diagram

9.Supply voltage sequence condition

The power ON/OFF sequence shown on Fig.12 shall be followed to avoid latch-up of drive LSI and application of DC voltage to LCD panel.

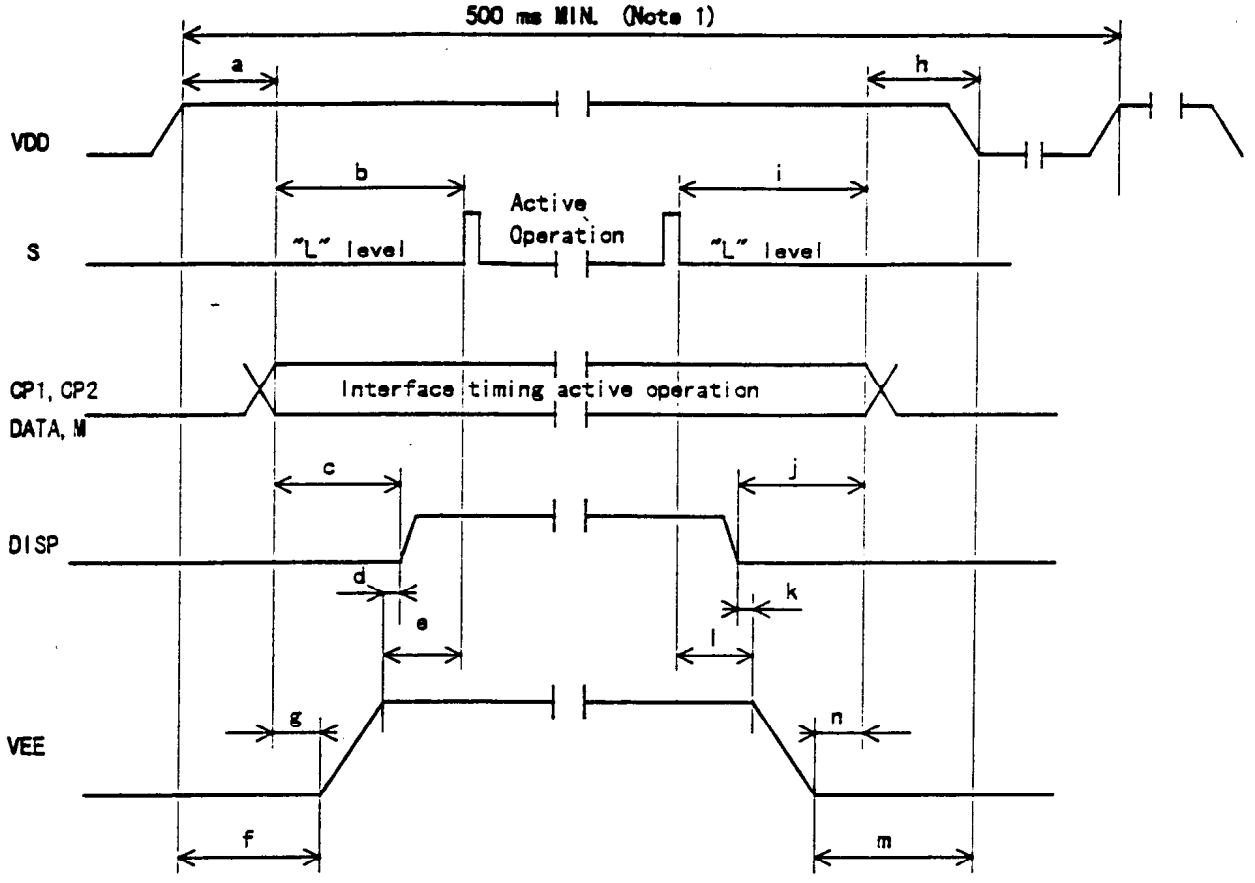


Fig.12 Power ON/OFF sequence

Table 9 Sequence timing ratings

POWER ON		
SYMBOL	With DISP control	Without DISP control
a	0 ms MIN.	0 ms MIN. 20 ms MAX.
b	0 ms MIN.	20 ms MIN.
c	20 ms MIN.	-
d	0 ms MIN.	-
e	-	0 ms MIN.
f	0 ms MIN.	(Note 2)
g	-	20 ms MIN.

POWER OFF		
SYMBOL	With DISP control	without DISP control
h	0 ms MIN.	0 ms MIN. 20 ms MAX.
i	0 ms MIN.	20 ms MIN.
j	20 ms MIN.	-
k	0 ms MIN.	-
l	-	0 ms MIN.
m	0 ms MIN.	(Note 2)
n	-	0 ms MIN.

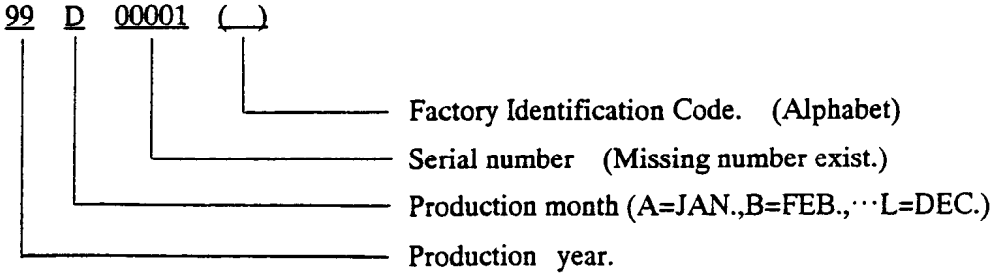
Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

Note 2) VEE to be set at "VSS level"

10.Lot number

Lot number is shown at the position mentioned in Fig .13 in accordance with the following numbering rule.

(Example)



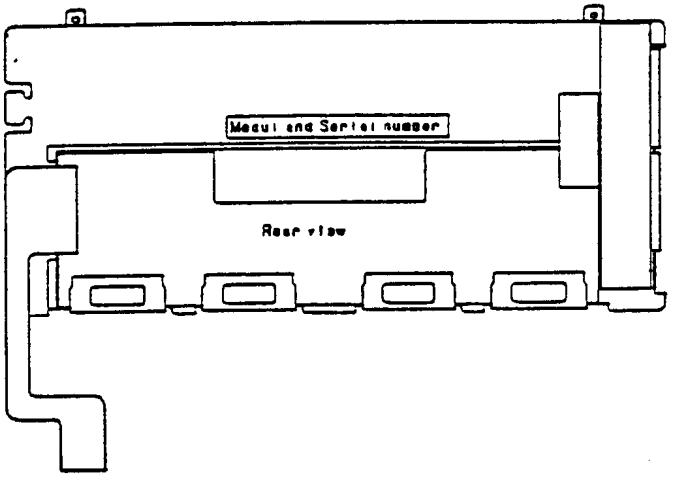


Fig.13.

11.Applicable inspection standard

The LCD panel shall meet the following inspection standard : S-U-012-01

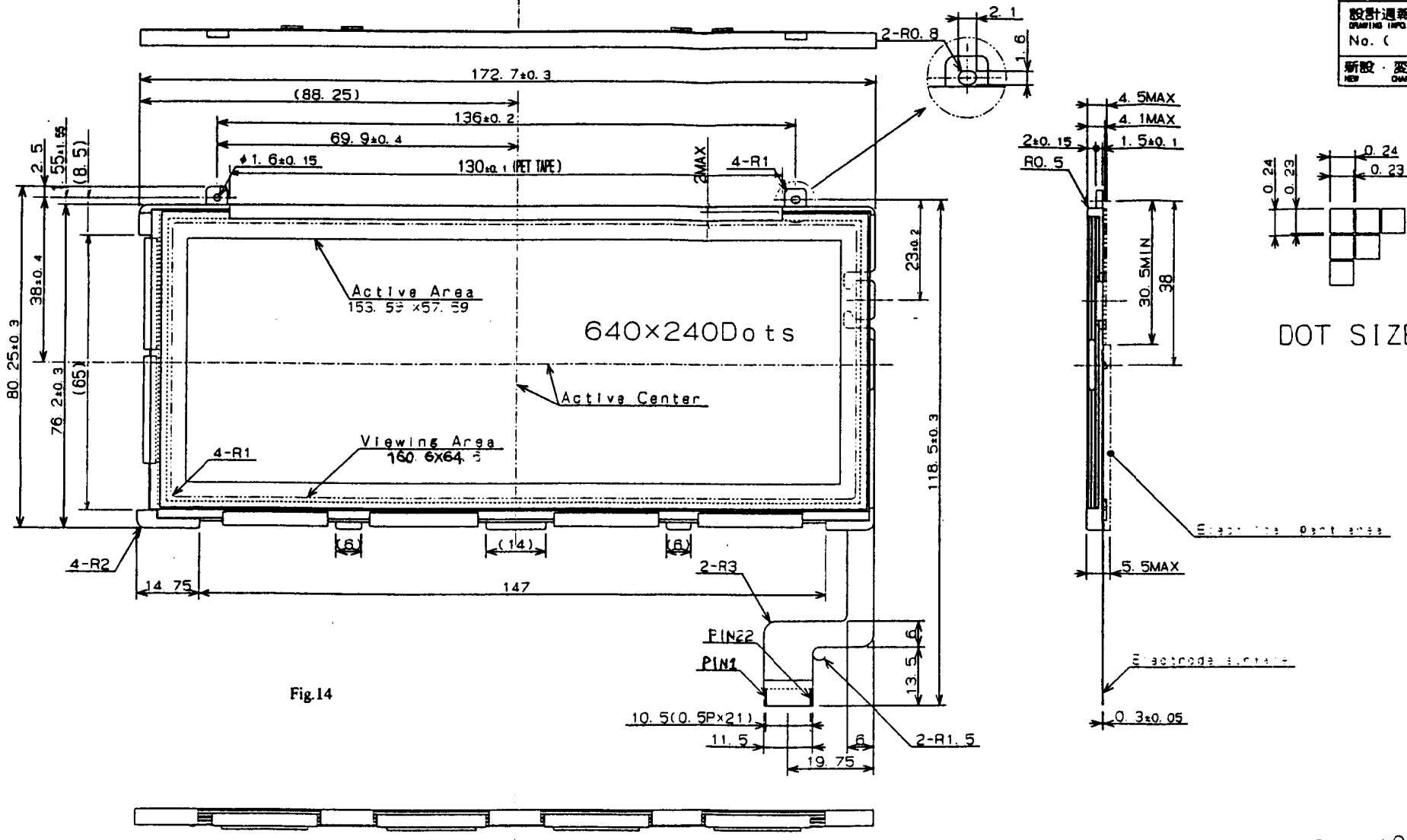
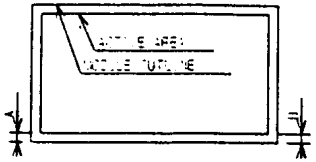


Fig.14

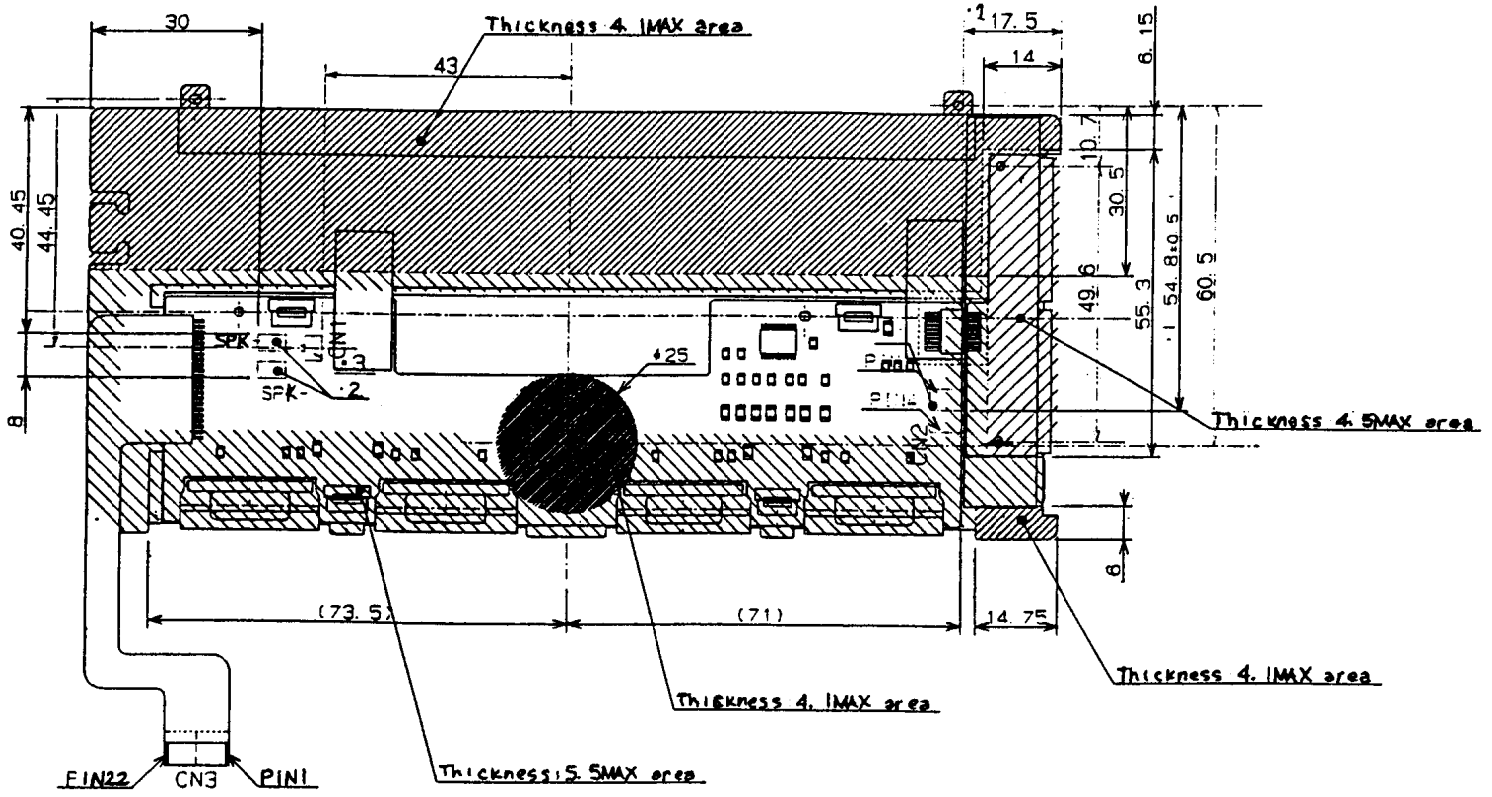
MODULE DISPLAY POSITION



DISTANCE OF DISPLAY AREA (A-B)±0.4

					LM7MS623	LCD Module
					640x240Dots	OUTLINE DIMENSION
					1/1	(BOTTOM VIEW)
DESIGN	DRAWN	CHECK	CHECK	APPROVE	SHARP CORPORATION	1999 APR 19
M Shibuya					Duty Panel Development Engineering Department 1	

±0.5



PIN LAYOUT

CN3

Pin No.	SIMBOL
1	D0
2	D1
3	D2
4	D3
5	LP(CP1)
6	CLK(CP2)
7	DISP OFF
8	FRAME(S)
9	DFTM
10	VDD
11	VDD
12	VEE
13	NC
14	NC
15	VSS
16	VSS
17	A
18	B
19	C
20	D
21	E
22	F

CN2

Pin No.	SIMBOL
1	C
2	D
3	E
4	F

CN1

Pin No.	SIMBOL
1	A
2	B

Fig.15

*3. Connector CN1 [SM02B-SSR-H(JST)] t:6.2MAX
*2. Pad[5x3]
*1. Connector CN2 [04 6227 004 100 800(KYOCERA ELCO)] t:6.2MAX

Note) Flatness is 1mmMAX for each specified thickness.

LM7MS623 640x2400dots		LCD Module OUTLINE DIMENSION (BOTTOM VIEW)
SCALE 1/1		
SHARP CORPORATION		APR 19
Duty Panel Development Engineering Department 1		

graphics, HVGA, 1/2 VGA, monochrome, passive, LM7MS623