National Semiconductor

September 3, 2010

LM96511

Ultrasound Receive Analog Front End (AFE)

General Description

The LM96511 is an 8-channel integrated analog front end (AFE) module for multi-channel applications, particularly medical ultrasound. Each of the 8 signal paths consists of a low noise amplifier (LNA), a digitally programmable variable gain amplifier (DVGA) and a 12-bit, 40 to 50 Mega Samples Per Second (MSPS) analog-to-digital converter (ADC) with Instant Overload Recovery (IOR). The architecture of the DVGA is a digitally-controlled linear-in-dB step attenuator driving a fixed-gain post-amplifier (PA). The ADC uses a Continuous-Time-Sigma-Delta (CTΣΔ) architecture with digital decimation filtering to maximize dynamic performance and provide an alias free input bandwidth to ADC CLK / 2. The ADC digital outputs are serialized and provided on differential LVDS outputs. The ADC includes an on-chip clock cleaner PLL.

In addition, for baseband CW Doppler Beamformer applications, an 8-channel demodulator with 16 discrete phase rotation angles is included.

Selective power reduction is included to minimize consumption of idle sections during interleaved imaging modes.

An SPI™ compatible serial interface allows dynamic digital programming and control. National Semiconductor offers a full development package for sale which includes acquisition analysis hardware and software with user friendly GUI for device programming and control.

Features

- 8-channel LNA, DVGA, and 12-bit Continuous Time ∑Δ ADC
- Programmable Active Termination LNA
- 8-channel, integrated CW Doppler Beamforer
- Low-power consumption
- Embedded ADC Digital Filter
- ADC Instant Overload Recovery
- Embedded ADC “clock-cleaning” PLL
- 11 mm x 17 mm RoHS BGA Package

Key Specifications

(Full path unless noted)

B-Mode:	
Total Input Voltage Noise (RTI)	0.9 nV/vHz
Max AFE Gain	58 dB
Single-Ended Input Swing	500mVpp
Programmable Maximum DVGA Attenuation	38, 36, 34, 32 dB
Programmable Post Amp Gain	31 or 38 dB
Attenuator Step Resolution	0.05 or 0.1 dB
ADC Resolution	12 bits
Conversion Rate (ADC CLK)	40 to 50 MSPS
ADC Digital Filter stop band attenuation	72 dB
ADC Digital Filter Passband Ripple	± 0.01 dB
ADC Instant Overload Recovery	1 ADC Clock Period
Power Consumption (per channel)	110 mW
CW Doppler Mode:	
Phase Rotation Resolution	22.5 degrees
Phase Noise (Per Channel, Offset = 5KHz)	-144 dBc/Hz
Dynamic Range	-161 dB/Hz
Amplitude Quadrature Error (I to Q)	± 0.04 dB
Phase Quadrature Error (I to Q)	± 0.10°
Power Consumption (Per Channel)	208 mW
Common Specifications:	
LNA Input Voltage Noise	0.82 nV/vHz
Operating temp. Range	0 to +70°C

Applications

- Ultrasound Imaging
- Communications
- Portable Instrumentation
- Sonar

Simplified LM96511 Block Diagram

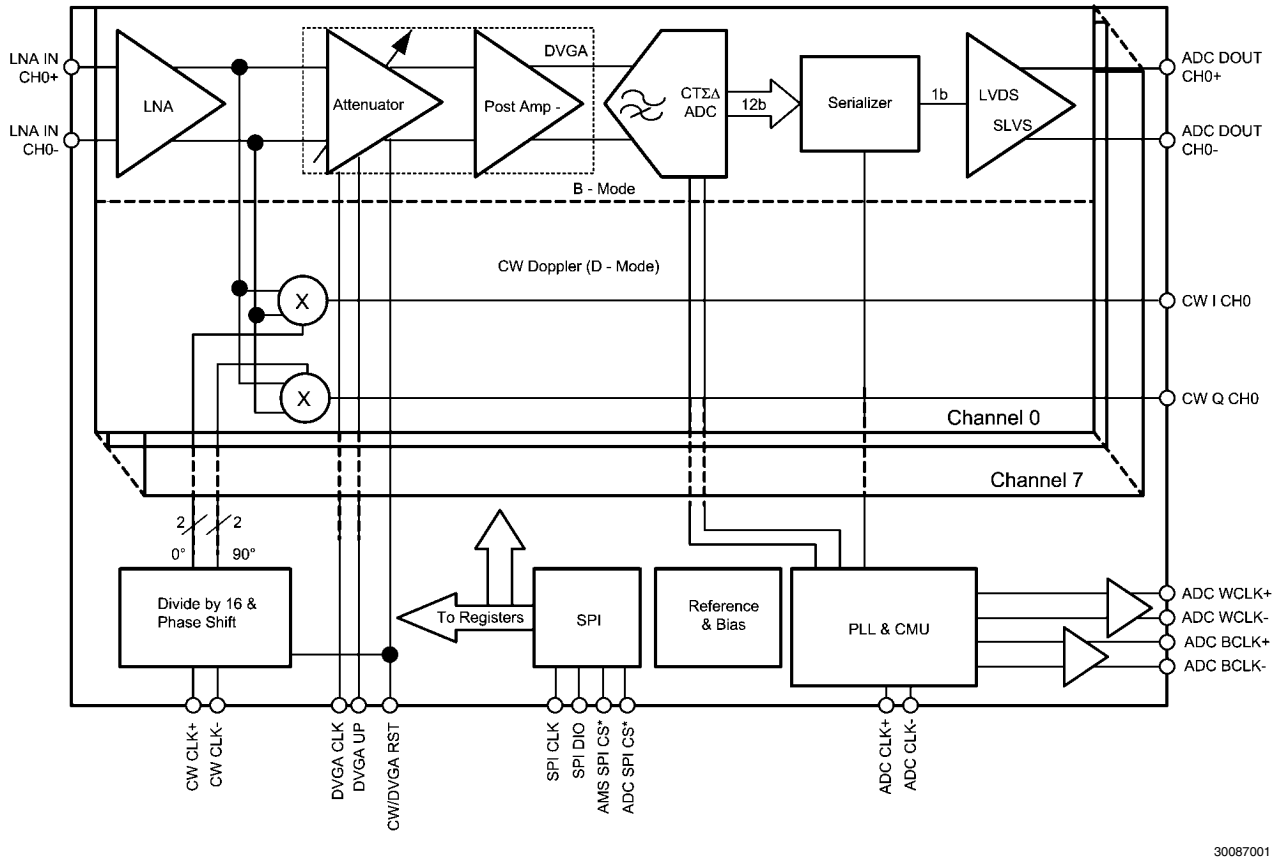
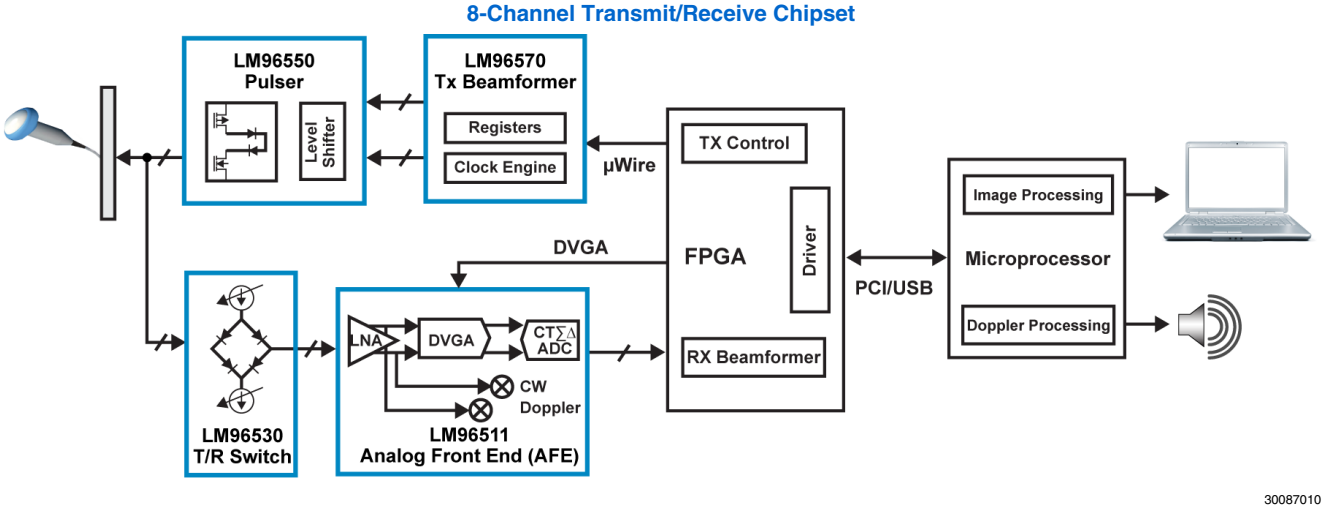


FIGURE 1. Simplified LM96511 Block Diagram

Typical Application



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A	LNA PD	DVGA PD	AMP RST	$\overline{\text{AMP SPI CS}}$	$\overline{\text{ADC SPI CS}}$	DVGA INIT MSB	AMP DVDD	AMP DGND	AGND	AMP AVCC A	CW I CH7	AGND	AGND	CW DGND	CW DGND	AGND	A
B	DVGA PA HI	CW AVCC	SPI CLK	SPI DIO	DVGA INIT LSB	AMP IO DVDD	AMP DVDD	AMP AVCC A	DVGA BYP CH7	CW AVCC	CW Q CH7	CW DGND	CW DGND	CW AVCC	CW AVCC	CW I CH6	B
C	NC	CW AVCC	AGND	NC										CW AVCC	DVGA BYP CH6	AMP AVCC A	C
D	LNA IN CH7-	LNA IN CH7+	AGND	LNA OUT CH7-										AMP AVCC A	AMP AVCC A	DVGA BYP CH5	D
E	LNA IN CH6+	CW AVCC	NC	AMP AVCC A										AMP AVCC A	CW I CH5	CW AVCC	E
F	LNA OUT CH6-	LNA IN CH6-	AGND	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			CW Q CH5	CW DGND	CW DGND	F
G	LNA IN CH5+	NC	AMP AVCC A	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			CW Q CH4	CW AVCC	CW I CH4	G
H	LNA OUT CH5 -	LNA IN CH5-	AGND	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			AMP DGND	CW AVCC	AMP DVDD	H
J	LNA IN CH4+	NC	AMP AVCC A	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			CW CLK+	CW CLK-	AMP AVCC A	J
K	LNA OUT CH4-	LNA IN CH4-	AGND	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			DVGA CLK	CW/DVGA RST	AMP CW/DVGA	K
L	LNA IN CH3+	NC	AMP AVCC A	CW AVCC			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			AMP IO DVDD	DVGA BYP CH3	AMP AVCC A	L
M	LNA OUT CH3-	LNA IN CH3-	AGND	AMP AVCC A			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			CW AVCC	CW AVCC	CW I CH3	M
N	LNA IN CH2+	CW AVCC	NC	AMP AVCC A			AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND	AMP THRM GND			CW Q CH3	CW DGND	CW DGND	N
P	LNA OUT CH2-	LNA IN CH2-	AGND	CW AVCC										AGND	CW I CH2	CW AVCC	P
R	LNA IN CH1+	NC	AMP AVCC A	AGND										AMP AVCC A	AMP AVCC A	DVGA BYP CH2	R
T	LNA OUT CH1-	LNA IN CH1-	CW AVCC	AMP AVCC A										AMP AVCC A	AMP AVCC A	CW AVCC	T
U	LNA IN CH0+	NC	AGND	AMP AVCC A	AMP DGND	AGND	AMP AVCC A	AMP AVCC A	CW AVCC	CW Q CH0	CW DGND	AGND	AMP AVCC A	AMP DVDD	AMP DVDD	CW AVCC	U
V	LNA IN CH0-	LNA OUT CH0-	AGND	AMP AVCC A	AMP DVDD	AMP AVCC A	NC	DVGA BYP CH0	CW AVCC	CW I CH0	AGND	AGND	AMP AVCC A	CW I CH1	AGND	CW DGND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

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	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
A	CW Q CH6	NC	ADC AVDD	NC	NC	ADC CLK-	AGND	AGND	AGND	ADC DVDD	ADC IO DGND	ADC IO DGND	ADC WCLK-	ADC WCLK+	ADC BCLK-	ADC BCLK+	A
B	AGND	NC	AGND	AGND	AGND	ADC CLK+	AGND	AGND	ADC DVDD	ADC DVDD	ADC IO DGND	ADC IO DGND	AGND	ADC IO DVDD	AGND	ADC DOUT CH7-	B
C	AMP AVCC A	ADC AVDD	AGND												AGND	ADC DOUT CH7+	C
D	AMP AVCC A	AGND	AGND												ADC IO DGND	ADC DOUT CH6-	D
E	CW AVCC	NC	NC												ADC IO DGND	ADC DOUT CH6+	E
F	AGND	ADC AVDD	AGND				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				AGND	ADC DOUT CH5-	F
G	AGND	AGND	AGND				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				ADC IO DVDD	ADC DOUT CH5+	G
H	AMP DVDD	NC	NC				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				ADC IO DVDD	ADC DOUT CH4-	H
J	DVGA BYP CH4	ADC AVDD	AGND				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				AGND	ADC DOUT CH4+	J
K	AMP AVCC A	NC	AGND				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				AGND	ADC DOUT CH3-	K
L	DVGA UP	AGND	NC				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				AGND	ADC DOUT CH3+	L
M	AGND	AGND	ADC AVDD				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				ADC IO DGND	AGND	M
N	AGND	AGND	NC				ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND	ADC THRM GND				ADC IO DGND	ADC DOUT CH2-	N
P	CW Q CH2	AGND	NC												AGND	ADC DOUT CH2+	P
R	CW AVCC	AGND	ADC AVDD												AGND	NC	R
T	DVGA BYP CH1	AGND	AGND												NC	ADC DOUT CH1-	T
U	AMP DGND	NC	ADC AVDD	NC	AGND	AGND	ADC RREF	ADC AVDD	$\overline{\text{ADC RST}}$	ADC AVDD	ADC DVDD	ADC AVDD	ADC IO DGND	AGND	ADC IO DVDD	ADC DOUT CH1+	U
V	CW Q CH1	NC	AGND	NC	ADC VREF GND	ADC VREF	ADC LPF BYP	AGND	AGND	ADC CW/DVGA	ADC AVDD	ADC DVDD	ADC AVDD	ADC IO DGND	ADC DOUT CH0+	ADC DOUT CH0-	V
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

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FIGURE 2. 376–Pin BGA Package Top View (18 Rows by 32 Columns)

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM96511CCSM NOPB	TFBGA 376	SLM376A	Trays

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Pin Descriptions

Ball Id. (Row_Column)	Pin Name	Function	Description
Amplifier Signals			
U1	LNA IN CH0+	Input	LNA Non-Inverting Input
R1	LNA IN CH1+		
N1	LNA IN CH2+		
L1	LNA IN CH3+		
J1	LNA IN CH4+		
G1	LNA IN CH5+		
E1	LNA IN CH6+		
D2	LNA IN CH7+		
V1	LNA IN CH0-		LNA Inverting Input
T2	LNA IN CH1-		
P2	LNA IN CH2-		
M2	LNA IN CH3-		
K2	LNA IN CH4-		
H2	LNA IN CH5-		
F2	LNA IN CH6-		
D1	LNA IN CH7-		
V2	LNA OUT CH0-	Output	LNA Inverting Output
T1	LNA OUT CH1-		
P1	LNA OUT CH2-		
M1	LNA OUT CH3-		
K1	LNA OUT CH4-		
H1	LNA OUT CH5 -		
F1	LNA OUT CH6-		
D4	LNA OUT CH7-		
V8	DVGA BYP CH0	Bypass	Decoupling Capacitor to Analog Ground
T17	DVGA BYP CH1		
R16	DVGA BYP CH2		
L15	DVGA BYP CH3		
J17	DVGA BYP CH4		
D16	DVGA BYP CH5		
C15	DVGA BYP CH6		
B9	DVGA BYP CH7		
J14	CW CLK+	Input	CW DOPPLER Differential Input Clock +
J15	CW CLK-		CW DOPPLER Differential Input Clock -
V10	CW I CH0	Output	CW DOPPLER In-Phase output current
V14	CW I CH1		
P15	CW I CH2		
M16	CW I CH3		
G16	CW I CH4		
E15	CW I CH5		
B16	CW I CH6		
A11	CW I CH7		

Ball Id. (Row_Column)	Pin Name	Function	Description
U10	CW Q CH0	Output	CW DOPPLER Quadrature-Phase output current
V17	CW Q CH1		
P17	CW Q CH2		
N14	CW Q CH3		
G14	CW Q CH4		
F14	CW Q CH5		
A17	CW Q CH6		
B11	CW Q CH7		
Amplifier Controls			
K14	DVGA CLK	Input	DVGA GAIN Clock
L17	DVGA UP		1 = Increment DVGA gain 0 = Decrement DVGA gain
A6	DVGA INIT MSB		DVGA Initial Gain Control. Sets the initial DVGA gain. See application section.
B5	DVGA INIT LSB		
K15	CW/DVGA RST		1 = CW DOPPLER Phase and DVGA Gain Reset
K16	AMP CW/DVGA		0 = B-mode 1 = CW DOPPLER mode
A1	LNA PD		1 = LNA Power-down
A2	DVGA PD		1 = DVGA Power-down
A3	AMP RST		1 = Reset all Amplifier SPI™ Registers
B1	DVGA PA HI		Post Amplifier Gain: 1= 38 dB 0= 31 dB
ADC Signals			
B22 A22	ADC CLK+ ADC CLK-	Input	Differential Input Clock. The input clock must lie in the range of 40 MHz to 50 MHz. It is used by the PLL to generate the internal sampling clocks .
V31	ADC DOUT CH0+	Output	Differential Serial Outputs for channels 0 to 7. Each pair of outputs provides the serial output for the specific channel. The default output is LVDS format, but programming the appropriate control registers, the output format can be changed to SLVS . By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors.
U32	ADC DOUT CH1+		
P32	ADC DOUT CH2+		
L32	ADC DOUT CH3+		
J32	ADC DOUT CH4+		
G32	ADC DOUT CH5+		
E32	ADC DOUT CH6+		
C32	ADC DOUT CH7+		
V32	ADC DOUT CH0-		
T32	ADC DOUT CH1-		
N32	ADC DOUT CH2-		
K32	ADC DOUT CH3-		
H32	ADC DOUT CH4-		
F32	ADC DOUT CH5-		
D32	ADC DOUT CH6-		
B32	ADC DOUT CH7-		

Ball Id. (Row_Column)	Pin Name	Function	Description
A30 A29	ADC WCLK+ ADC WCLK-	Output	Word Clock. Differential output frame clock used to indicate the bit boundary of each data sample. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors.
A32 A31	ADC BCLK+ ADC BCLK-		Bit clock. Differential output clock used for sampling the serial outputs. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors.
ADC Controls			
U25	$\overline{\text{ADC RST}}$	Input	This pin is an active low reset for the entire ADC, both analog and digital components. The pin must be held low for 500 ns then returned to high in order to ensure that the chip is reset correctly.
V26	ADC CW/DVGA	Input	0 = B-mode 1 = CW DOPPLER mode, PLL and References are still active to minimize recovery time.
V22	ADC VREF		ADC Optional External Reference Voltage; Improves channel-to-channel and converter-to-converter matching.
V21	ADC VREF GND		If Internal Reference is used, connect to AGND.
U23	ADC RREF	Output	External 10k ±1% resistor to ADC Analog GND. Used to set internal bias currents. Required regardless of the type of reference used.
V23	ADC LPF BYP	Bypass	Capacitor required by the Modulator DAC's LP Filter. Must be at least 100 nF to ADC Analog GND. Can be increased to 10 µF to minimize close-in phase noise.
SPI™ Compatible Interface			
B3	SPI™ CLK	Input	SPI™ clock
B4	SPI™ DIO	Input/Output	SPI™ Data Input/Output
A5	$\overline{\text{ADC SPI™ CS}}$	Input	0 = ADC SPI™ Chip Select
A4	$\overline{\text{AMP SPI™ CS}}$		0 = Amplifier SPI™ Chip Select.

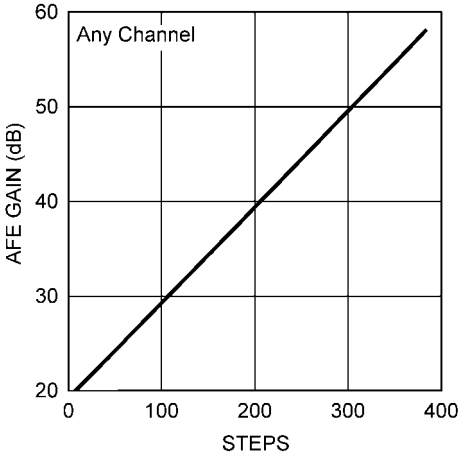
Ball Id. (Row_Column)	Pin Name	Function	Description
Power and Ground			
A10, B8, C16, C17, D14, D15, D17, E4, E14, G3, J3, J16, K17, L3, L16, M4, N4, R3, R14, R15, T4, T14, T15, U4, U7, U8, U13, V4, V6, V13	AMP AVCC A	Power	Amplifier Analog Power Nominally +3.3V.
B10, B14, B15, C14, E16, E17, H15, G15, M14, M15, P16, R17, T16, U9, U16, V9, B2, C2, E2, F4, G4, H4, J4, K4, L4, N2, P4, T3	CW AVCC		CW DOPPLER Analog Power Nominally +5.0V.
V5, A7, B7, H16, H17, U14, U15	AMP DVDD		DVGA Digital Power. Nominally +3.3V.
B6, L14	AMP IO DVDD		Amplifier IO Digital Power. Connect to ADC IO DVDD. Nominally +1.2V.
B30, G31, H31, U31	ADC IO DVDD		ADC IO Digital Power. Nominally +1.2V.
A19, C18, F18, J18, M19, R19, U19, U24, U26, U28, V27, V29	ADC AVDD		ADC Analog Power. Nominally +1.2V.
A26, B25, B26, U27, V28	ADC DVDD		ADC Digital Power. Nominally +1.2V .

Ball Id. (Row_Column)	Pin Name	Function	Description
A9, A12, A13, A16, A23, A24, A25, B17, B19, B20, B21, B23, B24, B29, B31, C3, C19, C31, D3, D18, D19, F3, F17, F19, F31, G17, G18, G19, H3, J19, J31, K3, K19, K31, L18, L31, M3, M17, M18, M32, N17, N18, P3, P14, P18, P31, R4, R18, R31, T18, T19, U3, U6, U12, U21, U22, U30, V3, V11, V12, V15, V19, V24, V25	AGND	Ground	Analog Ground
F7, F8, F9, F10, F11, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, M7, M8, M9, M10, M11, N7, N8, N9, N10, N11	AMP THRM GND		Thermal Ground (Connect to AGND)
F23, F24, F25, F26, F27, G23, G24, G25, G26, G27, H23, H24, H25, H26, H27, J23, J24, J25, J26, J27, K23, K24, K25, K26, K27, L23, L24, L25, L26, L27. M23, M24, M25, M26, M27, N23, N24, N25, N26, N27	ADC THRM GND		
A14, A15, B12, B13, F15, F16, N15, N16, U11, V16	CW DGND		Digital Ground
A8, H14, U5, U17	AMP DGND		
A27, A28, B27, B28, D31, E31, M31, N31, U29, V30	ADC IO DGND		
No Connect Important: “NC” pins should be left unconnected. Any connection to these pins could affect performance and functionality.			
A18, A20, A21, B18, C1, E3, E18, E19, G2, H18, H19, J2, K18, L2, L19, N3, N19, P19, R2, U2, U18, U20, V18, V20, R32, T31, V7, C4	NC		Do Not Connect

Typical Performance Characteristics

Unless otherwise noted, AMP AVCC A = AMP DVDD= 3.3V, CW AVCC = 5V; ADC AVDD = ADC DVDD = 1.2V, ADC IO DVDD = AMP IO DVDD = 1.2V, Full Scale RF Input at 5 MHz; CW CLK = 80 MHz;; FCLK = 40 MSPS ,TA =+25°C.

AFE Gain vs. Steps (DVGA PA HI = HI)



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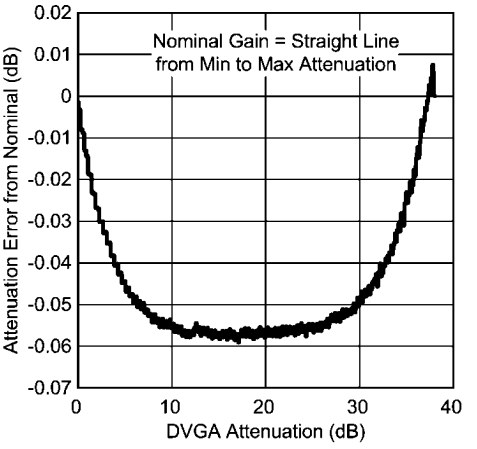
Attenuation Error from Nominal



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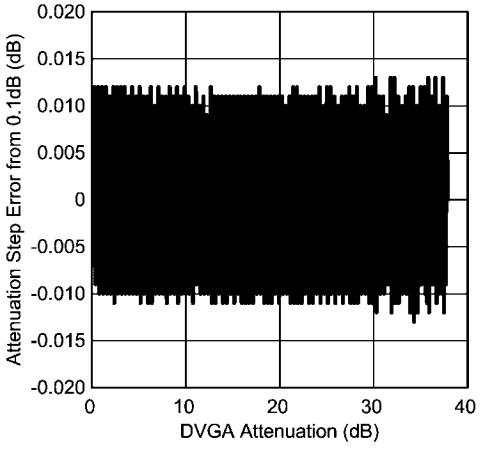
Attenuation Step Error from 0.1 dB



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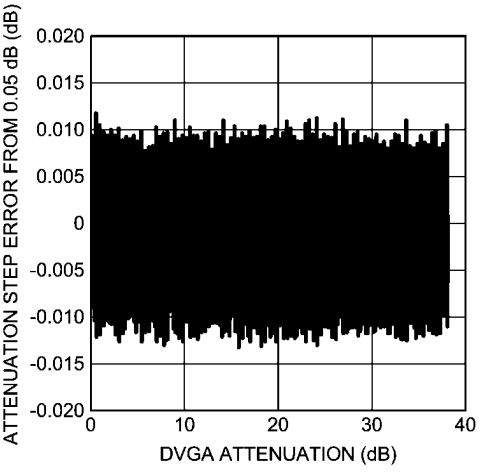
Attenuation Step Error from 0.05 dB



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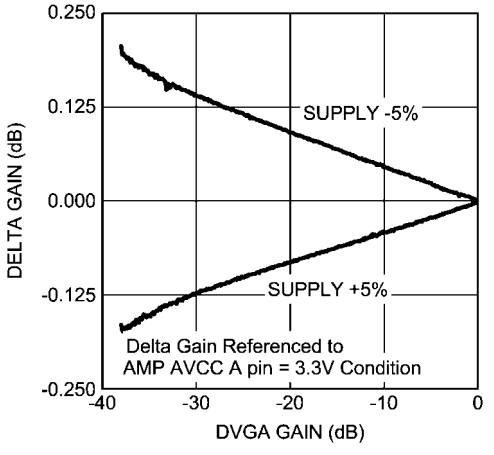
Gain Variation from Nominal vs Supply Voltage



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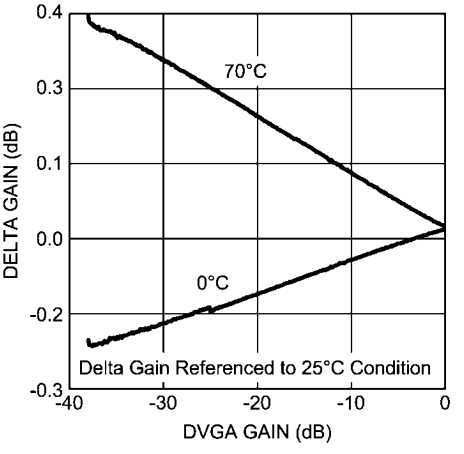
Gain Variation from Nominal vs Temperature



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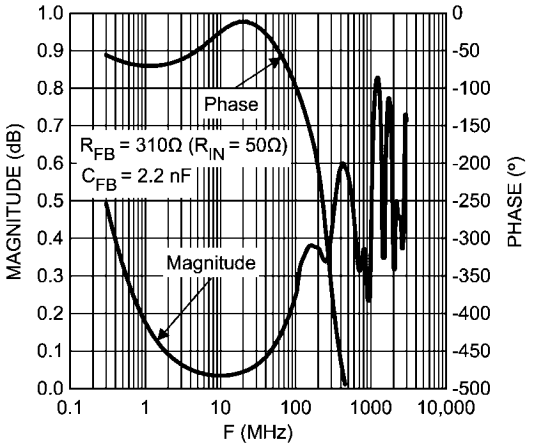
LNA S11 vs. Frequency



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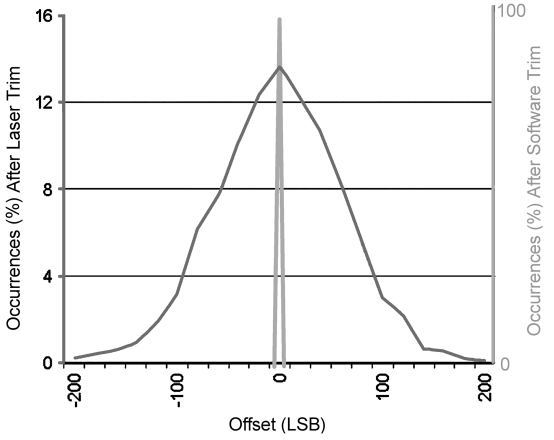
AFE Offset Distribution IOR On Mode, Minimum DVGA attenuation, DVGA PA HI pin = LO)



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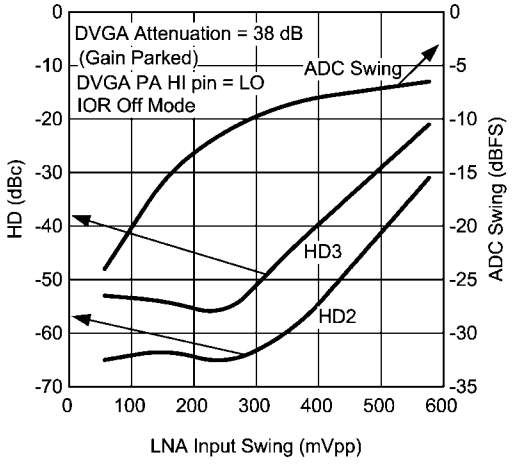
HD vs. LNA Input Swing (PA HI pin = LO)



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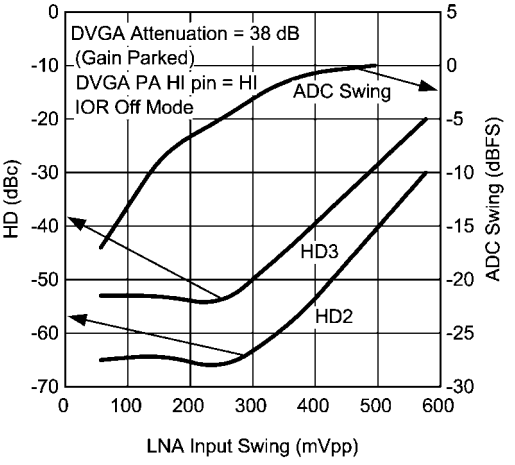
HD vs. LNA Input Swing (PA HI pin = HI)



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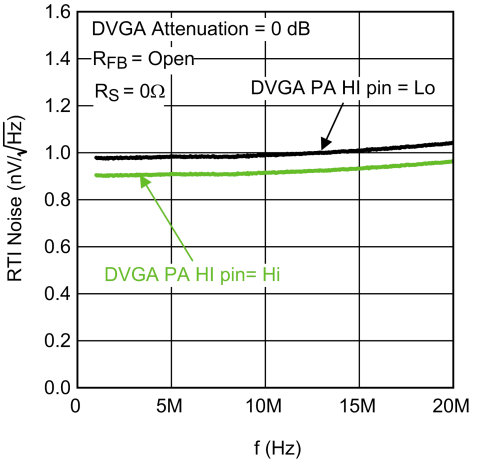
RTI Noise vs. Frequency (DVGA Attenuation = 0dB)



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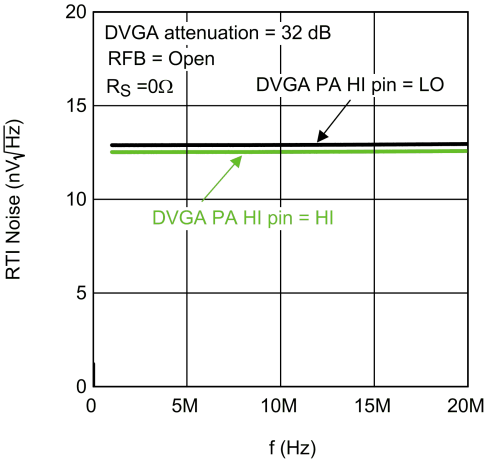
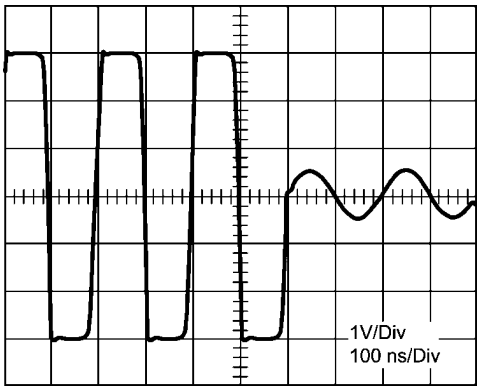
RTI Noise vs. Frequency (DVGA Attenuation = 32dB)



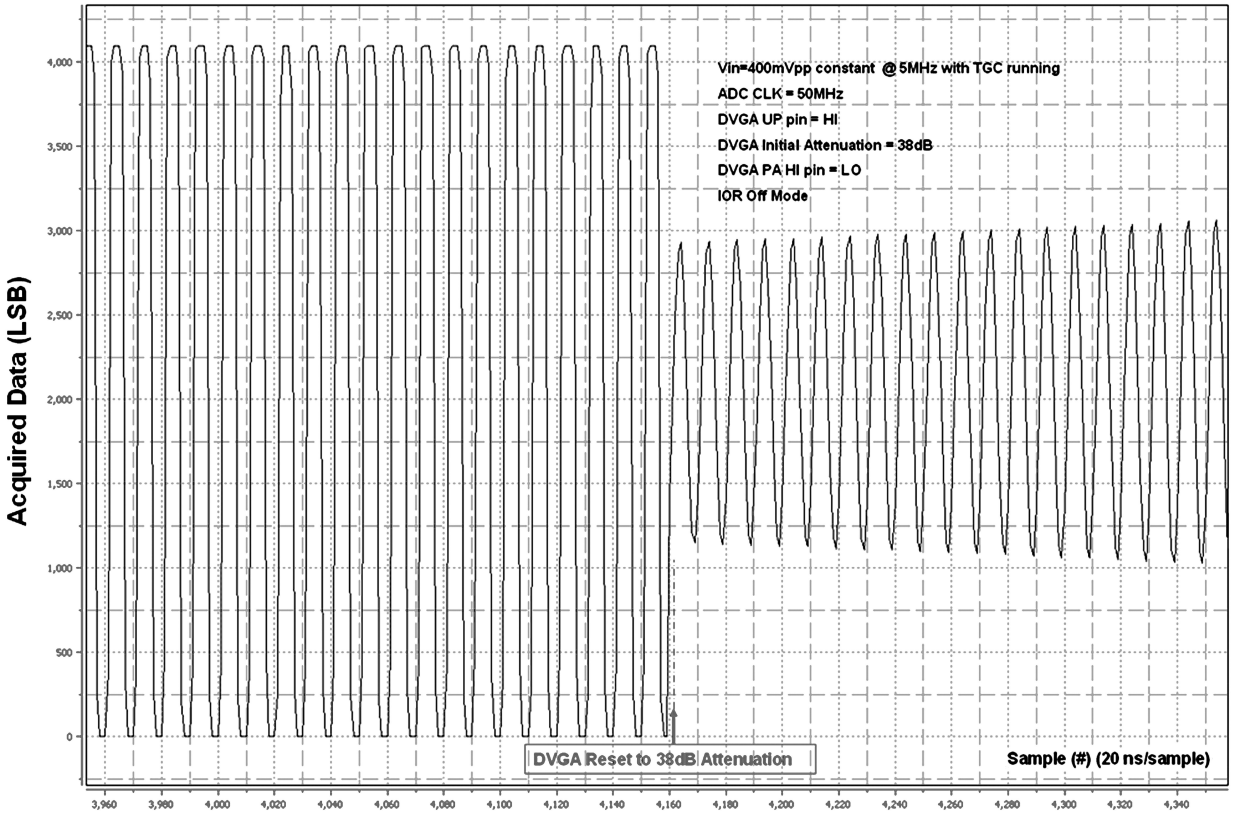
30087082

Far-Field Overload Recovery
@ Post Amp Output (No User Access)



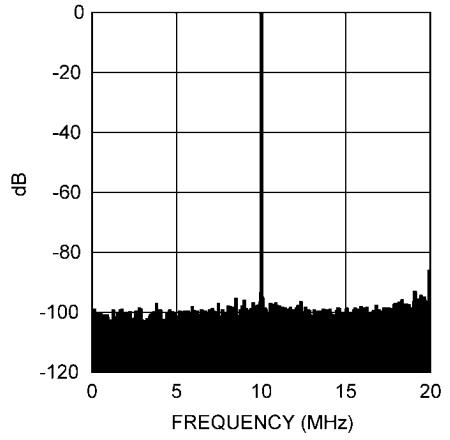
30087073

AFE (B-Mode) Overload Recovery



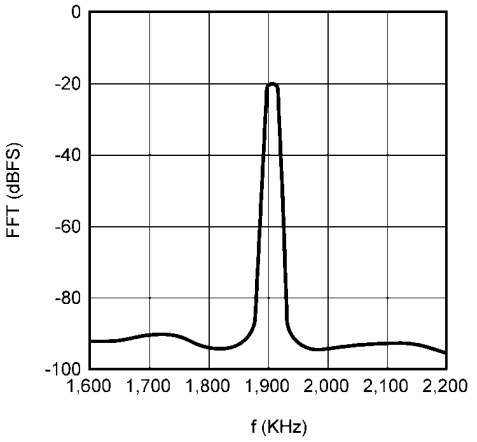
30087094

Spectral Response @ f_{IN}=10 MHz, ADC CLK = 400 mHz, IOR On



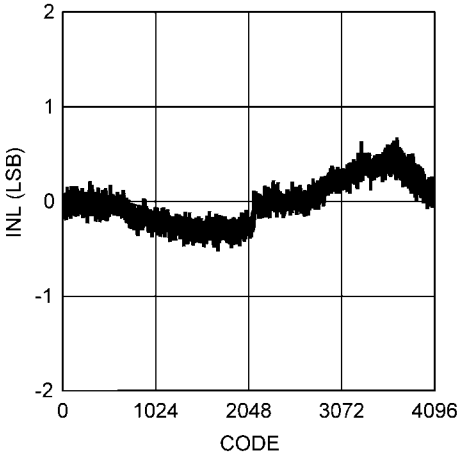
30087077

Close-In Spectral Response @ fIN=1.9 MHz, TGC Running, Cosine 6 Term Window



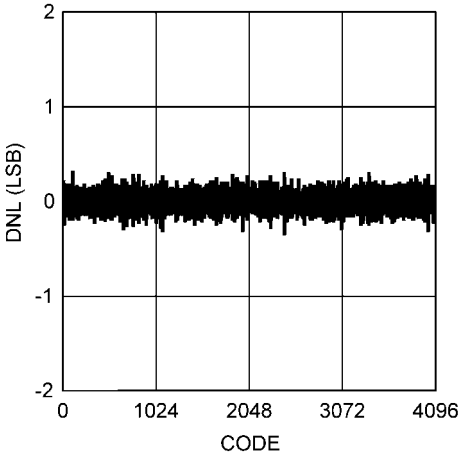
30087095

ADC INL



30087076

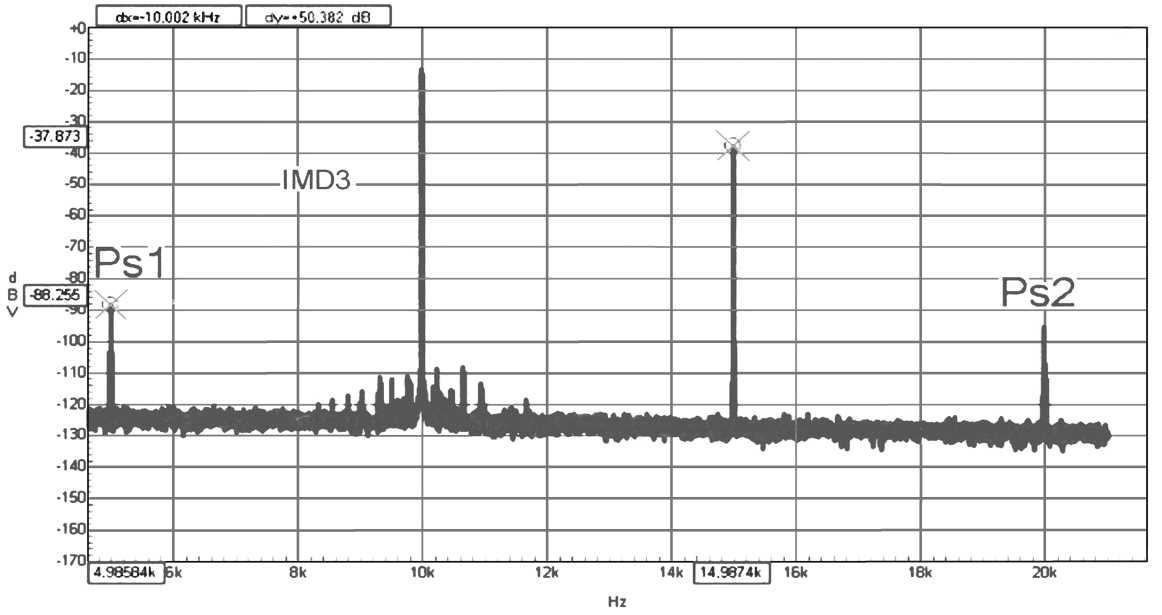
ADC DNL



30087075

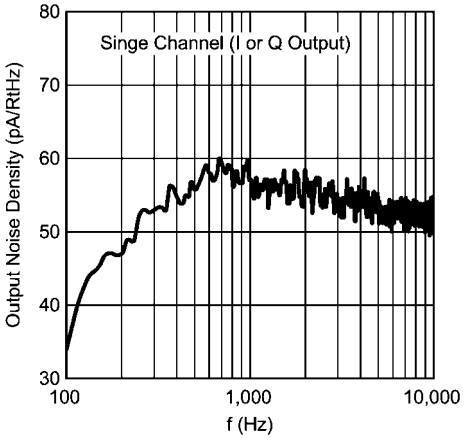
CW Doppler Plots

**CW Doppler IMD3, Unequal Tones
10kHz & 15kHz Offset,
25 dB Separation**



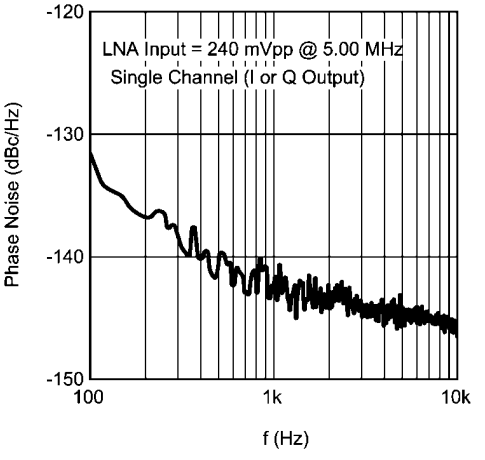
30087030

CW Doppler Output Noise (CWDIFF CLK = 80.0MHz)



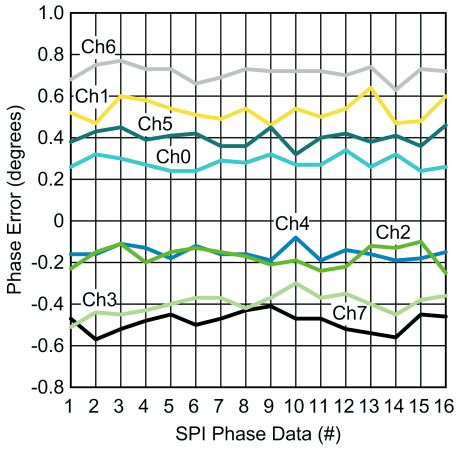
30087080

CW Doppler Phase Noise



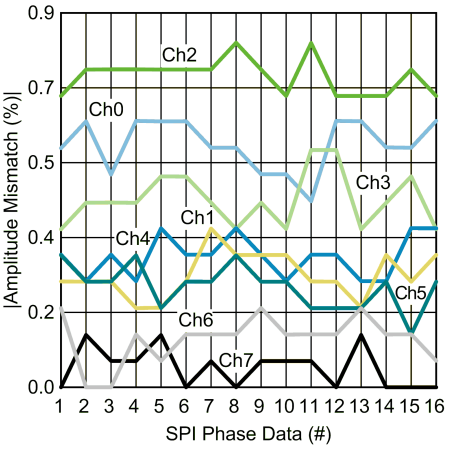
30087081

I-Q Quadrature Phase Error (Within Channel)



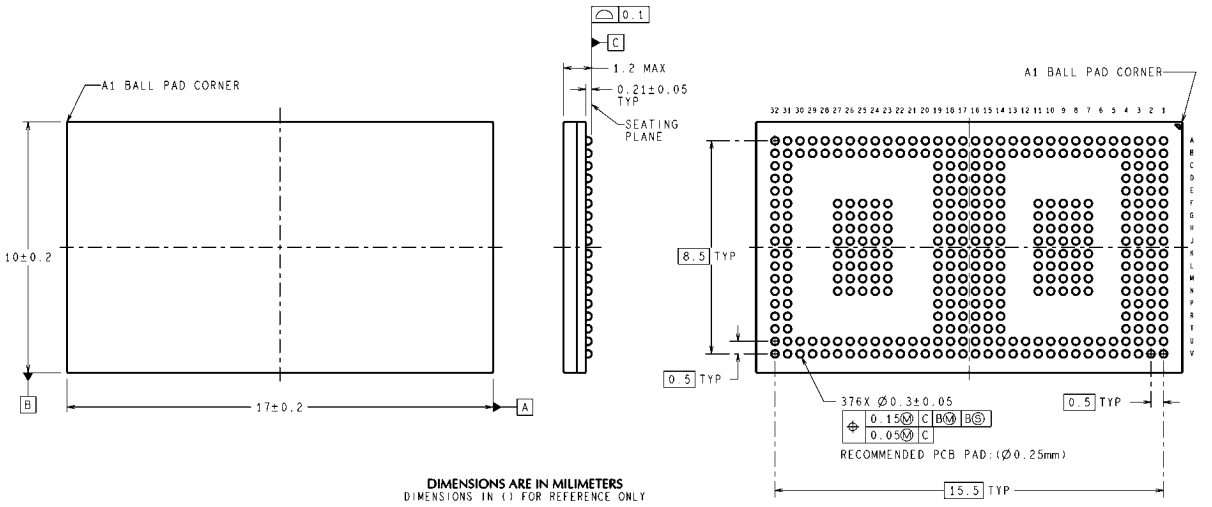
30087068

I-Q Output Amplitude Match (Within Channel)



30087069

Physical Dimensions inches (millimeters) unless otherwise noted



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