National Semiconductor

LM96570 PRODUCT BRIEF

PRELIMINARY
September 3, 2010

Ultrasound Configurable Transmit Beamformer

General Description

The LM96570 is an eight-channel monolithic beamformer for pulse generators in multi-channel medical ultrasound applications. It is well-suited for use with National's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96570 offers eight P and N output channels with individual delays of up to 102.4 µs operating at pulse rates of up to 80 MHz. A pulse sequence is launched on all channels simultaneously through a single firing signal. Advanced features include delay resolution down to 1/1280 µs and programmable patterns of up to 64 pulses. Pulse patterns and delay settings are pre-programmed through a serial interface, thereby simplifying the timing requirements on the driving circuitry.

The LM96570 is packaged in a 32-pin LLP.

Applications

- Ultrasound Imaging

Features

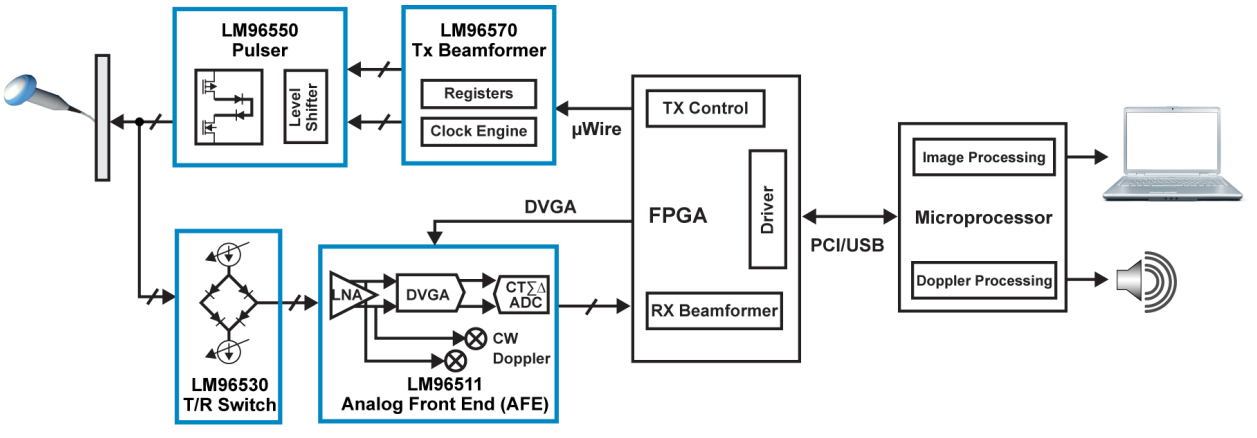
- Full control over selecting beam directions and pulse patterns by programming individual channel parameters
- Outputs interface seamlessly with positive and negative inputs on octal high-voltage pulser ICs
- Beamformer timing provides:
  - — Delay resolution of 1/1280 µs
  - — Delay range of up to 100 µs
- Pulse patterns are locally generated with:
  - — Sequences of up to 64 pulses
  - — Pulse width modulation at 80 MHz
- 2.5V to 3.3V CMOS logic interface

Key Specifications

I/O voltage	2.5 to 3.3	V
Core supply voltage	1.8	V
Output pulse rate	80	MHz
Reference frequency	40 (±5%)	MHz
1δ Output Jitter (@ 5MHz)	25	ps
Output Phase Noise (@ 5MHz, 1kHz offset)	–116	dBc/Hz
Delay resolution	1/1280	µs
Delay range	102.4	µs
Max. pattern length	64	pulses
Serial interface speed	2	Mbps
Total Power	0.063	Watts
Operating Temp.	0 to +70	°C

Typical Application

8-Channel Transmit/Receive Chipset



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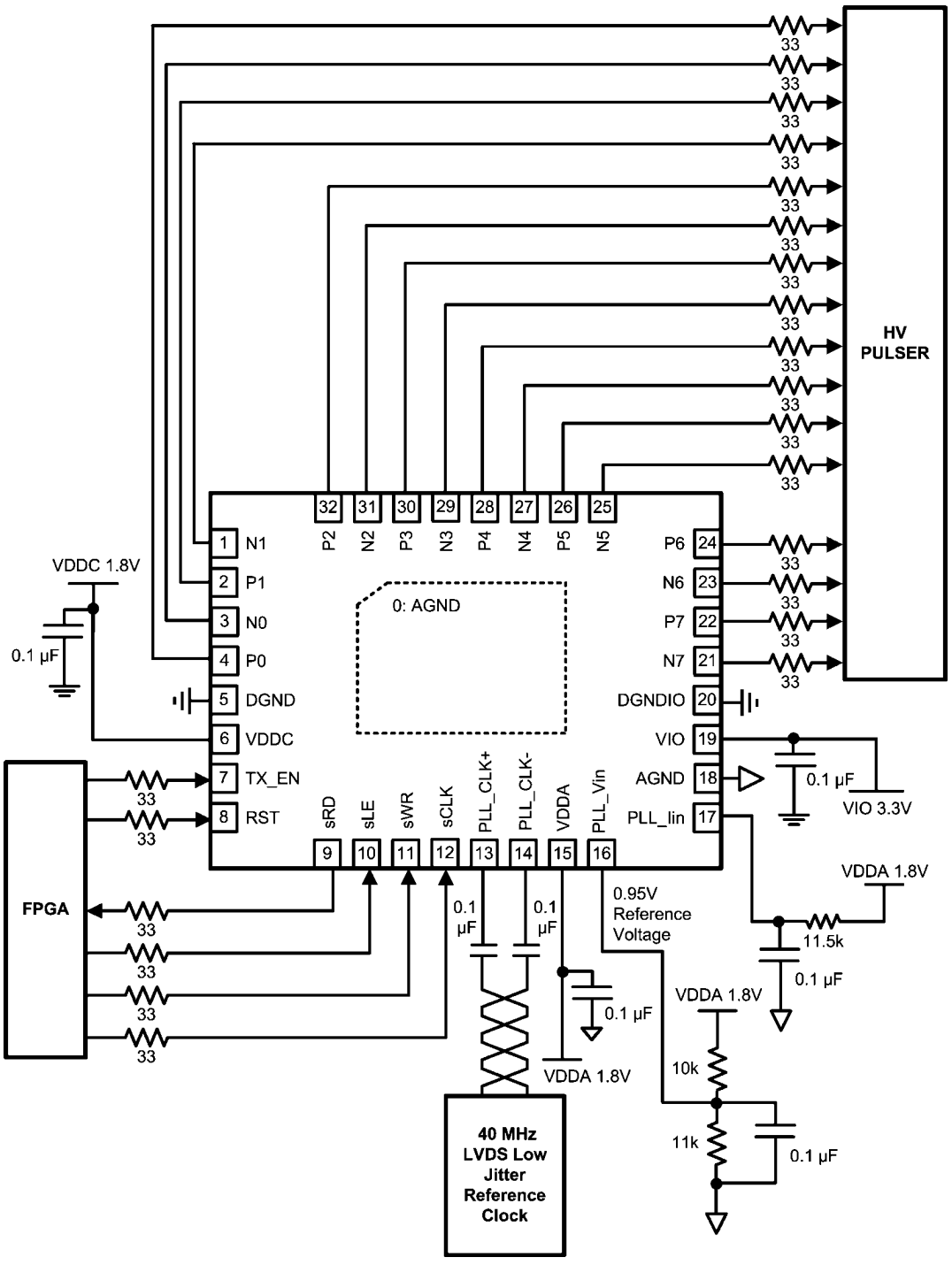
Block Diagram



Connection Diagram

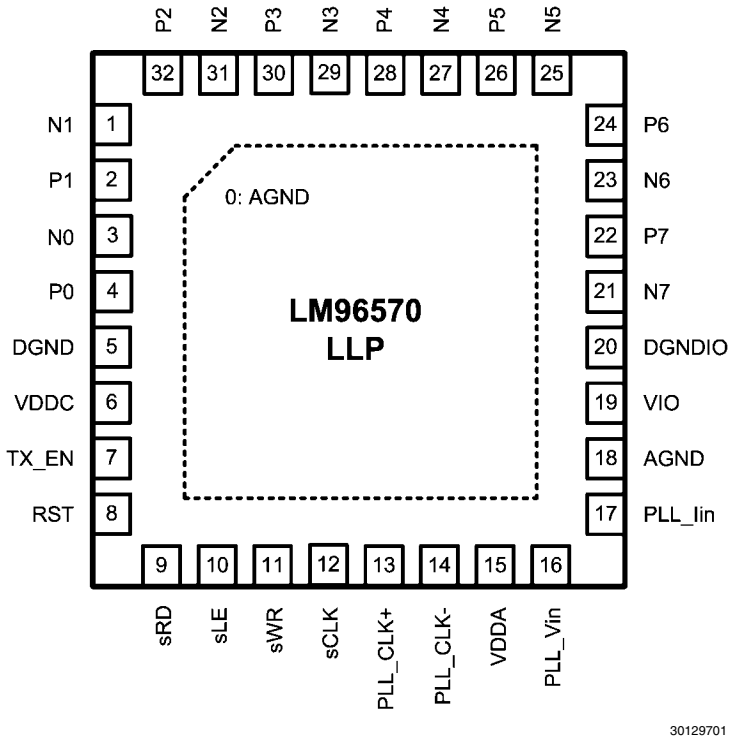
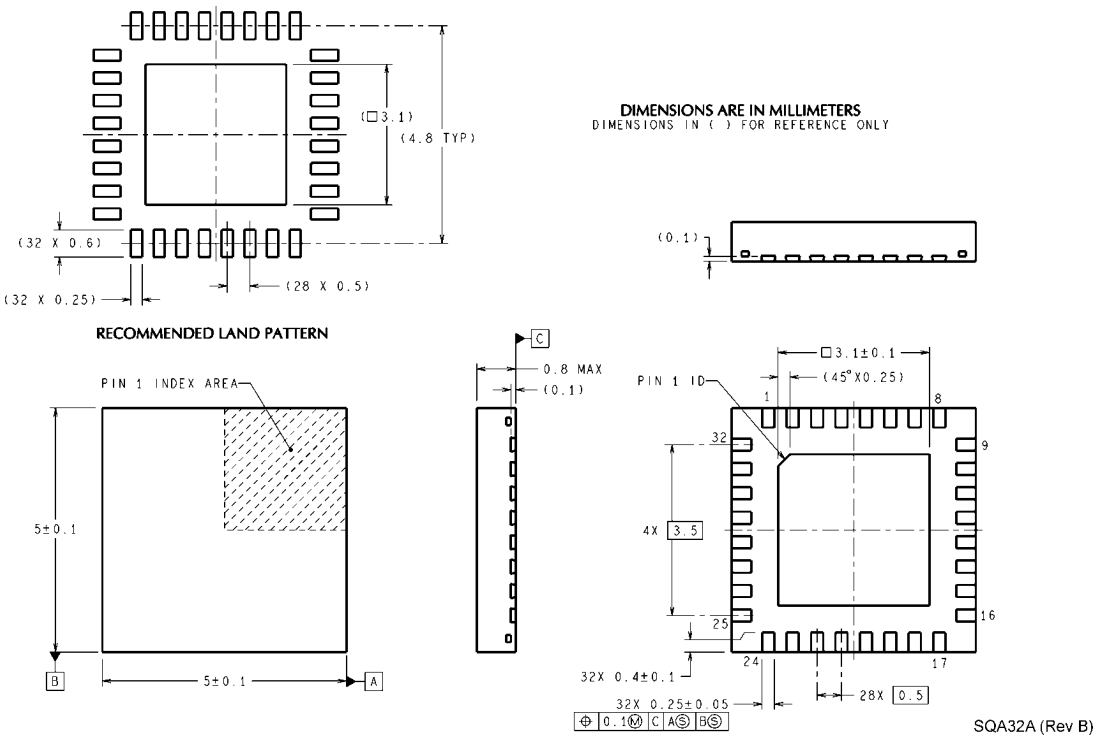


FIGURE 1. Pin Diagram of LM96570

Pin Descriptions

Pin No.	Name	Type	Function and Connection
1 – 4, 21 – 32	P0-7, N0-7	Output	Control signals for pulser. P outputs control positive pulses and N outputs control negative pulses.
13	PLL_CLK+	Input	PLL Reference Clock PLUS Input, LVDS compatible or Single-Ended LV CMOS input, programmable through 4-Wire Serial Interface (Register 0x1Bh[0])
14	PLL_CLK-	Input	PLL Reference Clock MINUS input, LVDS compatible. For Single-Ended PLL Reference Clock operation, tie this pin to AGND or VDDA.
7	TX_EN	Input	1 = Beamformer starts firing 0 = Beamformer ceases firing
16	PLL_Vin	Input	Voltage range 0.8-1.2V for tuning internal PLL noise performance. Under normal conditions, 0.94V is recommended.
17	PLL_Iin	Input	100 µA current input
8	RST	Input	Asynchronous Chip Reset 1 = Reset 0 = No Reset
12	sCLK	Input	4-Wire Serial Interface Clock
10	sLE	Input	4-Wire Serial Interface Latch Enable
11	sWR	Input	4-Wire Serial Interface Data Input for writing data registers
9	sRD	Output	4-Wire Serial Interface Data Output for reading data registers
15	VDDA	Power	Analog supply voltage (1.8V)
6	VDDC	Power	Digital core supply voltage (1.8V)
19	VIO	Power	Digital I/O supply voltage (2.5 to 3.3V)
0, 18	AGND	Ground	PLL Analog ground
5	DGND	Ground	Digital core ground
20	DGNDIO	Ground	Digital I/O ground

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead LLP Package
NS Package Number SQA32A

Notes

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