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National Semiconductor™

LM9812 30-Bit Color Linear CCD Sensor Processor

General Description

The LM9812 is a high performance integrated signal processor/digitizer for color linear CCD image scanners. The LM9812 performs all the signal processing (correlated double sampling, pixel rate offset and shading correction, color balance control, and 10-bit analog-to-digital conversion) necessary to maximize the performance of a wide range of linear CCD sensors.

The LM9812 can be digitally programmed to work with a wide variety of CCDs from different manufacturers, including both 3 output RGB and 2 output GRGB CCDs. An internal Configuration Register sets CCD and sampling timing to maximize performance, simplifying the design and manufacturing processes. For complementary voltage reference see the LM4041-ADJ.

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Scanners
- Multifunction Imaging Products
- Digital Copiers
- General Purpose Linear CCD Imaging

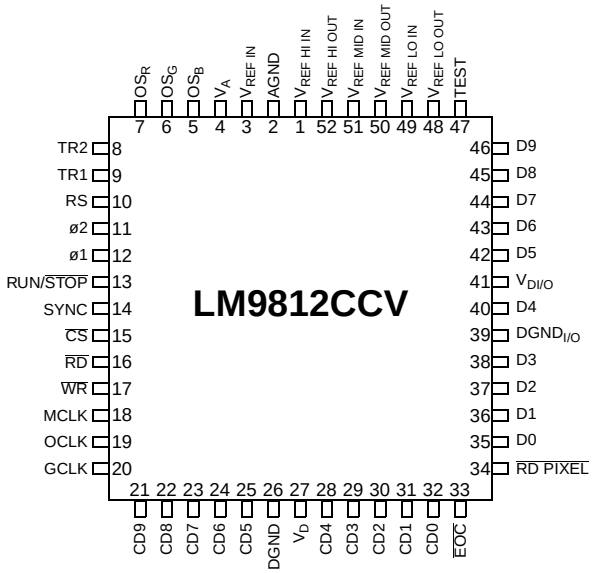
Features

- 6 million pixels/s conversion rate (2MHz/channel x 3)
- Pixel rate shading (gain) correction for individual pixels eliminates errors from PRNU, illumination, etc.
- Digitally programmed color balance controls
- Pixel rate offset correction for highest quality in dark regions
- Correlated Double Sampling for lowest noise
- Reference and signal sampling points digitally controlled in 20ns increments
- 2x and 4x analog fast preview/low resolution modes
- Digital control of CCD integration time
- Generates all necessary CCD clock signals
- Compatible with a wide range of color linear CCDs and Contact Image Sensors (CIS)
- TTL/CMOS input/output compatible

Key Specifications

• Output Data Resolution	10 Bits
• Pixel Conversion Rate (total)	6MHz
• Supply Voltage	+5V±5%
• Supply Voltage (Digital I/O)	+3.3V±10% or +5V±5%
• Power Dissipation (typical)	390mW

Connection Diagrams



Ordering Information

Commercial ($0°C \le T_A \le +70°C$)	Package
LM9812CCV	V52A 52 Pin Plastic Leaded Chip Carrier

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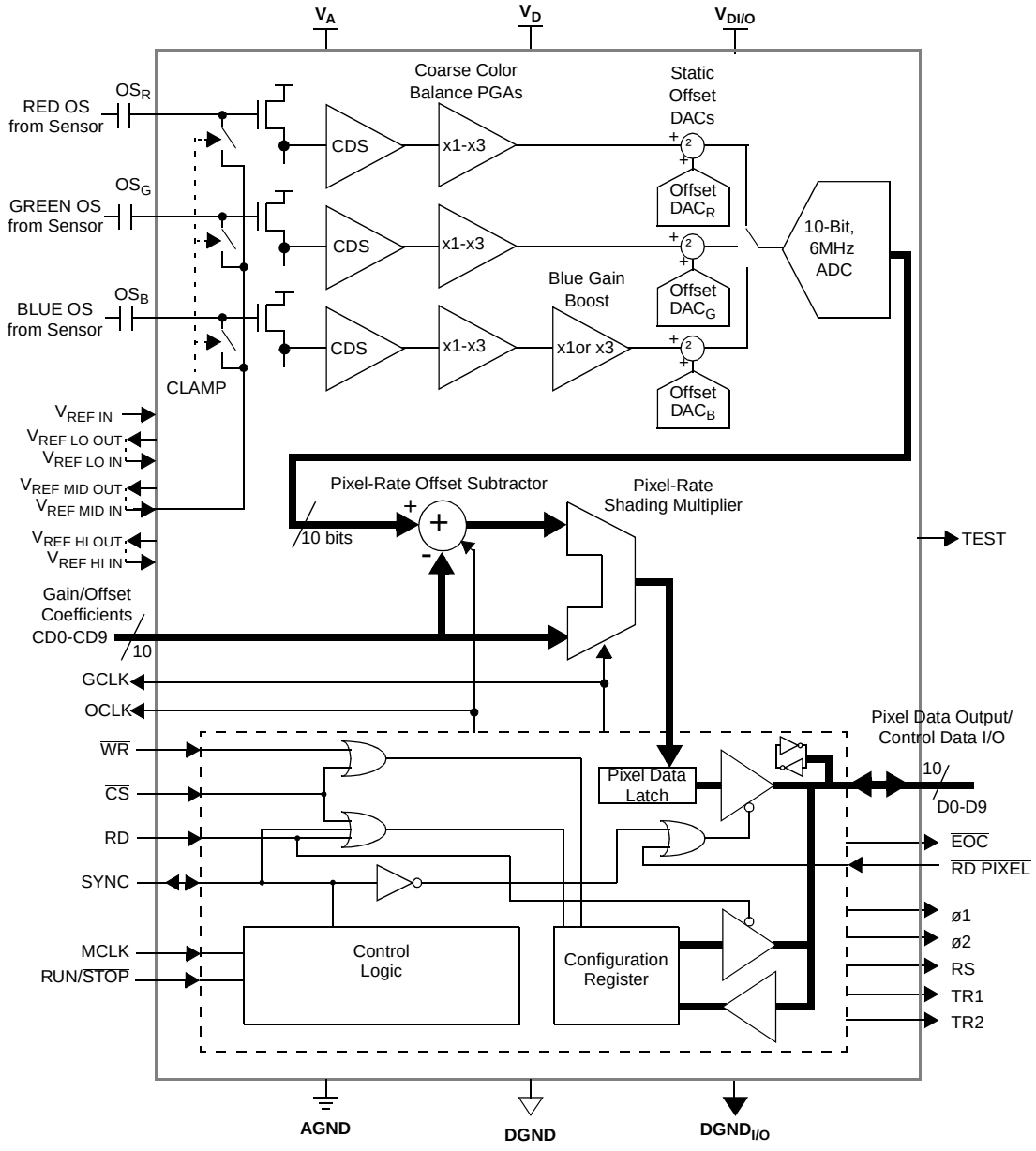
Block Diagram



Absolute Maximum Ratings (Notes 1 & 2)

Positive Supply Voltage (V^+=V_A=V_D=$V_{DI/O}$)	
With Respect to GND=AGND=DGND=$DGND_{I/O}$	6.5V
Voltage On Any Input or Output Pin	0.3V to V^++0.3V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C (Note 4)	
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Soldering Information	
Infrared, 10 seconds (Note 6)	300°C
Storage Temperature	-65°C to +150°

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	T_{MIN}≤T_A≤T_{MAX}
LM9812CCV	0°C≤T_A≤+70°C
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+4.75V to +5.25V
$V_{DI/O}$ Supply Voltage	+3.0V to +5.25V
$\|V_A-V_D\|$	≤ 100mV
$V_A-V_{DI/O}$	< -100mV
OS_R, OS_G, OS_B, $V_{REF\ IN}$	
Input Voltage Range	-0.05V to V_A + 0.05V
CD0-CD9, D0-D9, MCLK, SYNC, RUN/$\overline{STOP}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{RD\ PIXEL}$	
Input Voltage Range	-0.05V to $V_{DI/O}$ + 0.05V

Electrical Characteristics

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=+5.0V_{DC}, $V_{DI/O}$**=+5.0 or +3.3V_{DC}, $V_{REF\ IN}$ = +2.0V_{DC}, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7, 8, & 12)

CCD/CIS Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
$V_{OS\ PEAK}$	Sensor's Maximum Peak Differential Signal Range	Color Balance PGA gain = 0.933 Color Balance PGA gain = 3.0 Color Balance PGA gain = 9.0 (Blue Channel, BOOST on)		**1.0** **0.33** **0.11**	V (min) V (min) V (min)
	Sensor's Maximum Correctable Range of Pixel-to-Pixel V_{WHITE} Variation/Color	Range 0 Range 1 Range 2		**67 (1:3)** **50 (1:2)** **33 (1:1.5)**	% % %
Coarse Color Balance PGA Characteristics					
	Monotonicity			**5**	bits (min)
	G_0 (Minimum PGA Gain)	PGA Setting = 0	0.93	**0.90** **0.97**	V/V (max) V/V (min)
	G_{31} (Maximum PGA Gain)	PGA Setting = 31	3.00	**2.85** **3.20**	V/V (max) V/V (min)
	$G_{BLUE\ BOOST}$	Blue PGA Boost Setting = x3	3.00	**2.72** **3.27**	V/V (max) V/V (min)
	Gain Error at any gain (Note 14)		±1.0	**±4.0**	% (min) % (max)
Static Offset DAC Characteristics					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	In units of ADC LSBs	4.2	**1.3** **7.2**	LSB (min) LSB (max)
	Offset DAC Adjustment Range	In units of ADC LSBs	±130	**±118**	LSB (min)
ADC Characteristics					
	Resolution with No Missing Codes			**10**	Bits (min)
ILE	Integral Linearity Error (Note 11)		±0.4	**±1.5**	LSB (max)
DNL	Differential Non-Linearity		-0.14 +0.32	**-0.5** **+1.0**	LSB (min) LSB (max)
System Characteristics					
C	Analog Channel Gain Constant		2.00	**1.83** **2.17**	(min) (max)

Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=+5.0V_{DC}, $V_{DI/O}$**=+5.0 or +3.3V_{DC}, **$V_{REF\ IN}$** = +2.0V_{DC}, **f_{MCLK}**=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7, 8, & 12)

V_{OS1}	Pre-PGA Analog Channel Offset Error CCD Mode	In units of ADC LSBs	+5	**-40** **+40**	LSB (min) LSB (max)
V_{OS1}	Pre-PGA Analog Channel Offset Error CIS Mode	In units of ADC LSBs	+32	**-65** **+135**	LSB (min) LSB (max)
V_{OS2}	Post-PGA Analog Channel Offset Error	In units of ADC LSBs	-5	**-40** **+30**	LSB (min) LSB (max)
Reference and Analog Input Characteristics					
	OS_R, OS_G, OS_B Input Capacitance		5		pF
	OS_R, OS_G, OS_B Input Leakage Current	Measured with OS = 2.5V_{DC}	2	**20**	nA (max)
	$V_{REF\ IN}$ Input Leakage Current	Measured with $V_{REF\ IN}$ = 2.0V_{DC}	4	**20**	nA (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=+5.0V_{DC}, $V_{DI/O}$**=+5.0 or +3.3V_{DC}, **$V_{REF\ IN}$** = +2.0V_{DC}, **f_{MCLK}**=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
D0-D9, CD0-CD9, MCLK, RUN/$\overline{\text{STOP}}$, SYNC, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{RD PIXEL}}$ Digital Input Characteristics					
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{DI/O}$=5.25V $V_{DI/O}$=3.6V		**2.0** **2.0**	V (min) V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{DI/O}$=4.75V $V_{DI/O}$=3.0V		**0.8** **0.7**	V (max) V (max)
I_{IN}	Input Leakage Current	V_{IN}=V_D V_{IN}=DGND	0.1 -0.1		µA µA
C_{IN}	Input Capacitance		5		pF
D0-D9, $\overline{\text{EOC}}$, GCLK, OCLK, SYNC Digital Output Characteristics					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{DI/O}$=4.75V, I_{OUT}=-360µA $V_{DI/O}$=4.75V, I_{OUT}=-10µA $V_{DI/O}$=3.0V, I_{OUT}=-360µA $V_{DI/O}$=3.0V, I_{OUT}=-10µA		**2.4** **4.4** **2.1** **2.5**	V (min) V (min) V (min) V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{DI/O}$=5.25V, I_{OUT}=1.6mA $V_{DI/O}$=3.6V, I_{OUT}=1.6mA		**0.4** **0.4**	V (max) V (max)
I_{OUT}	TRI-STATE® Output Current (D0-D9 only)	V_{OUT}=DGND V_{OUT}=V_D	0.1 -0.1		µA µA
Ø1, Ø2, RS, TR1, TR2 Digital Output Characteristics					
$V_{OUT(1)}$	Logical “1” Output Voltage	V_D=4.75V, I_{OUT}=-360µA V_D=4.75V, I_{OUT}=-10µA		**2.4** **4.4**	V (min) V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_D=5.25V, I_{OUT}=1.6mA		**0.4**	V (max)
Power Supply Characteristics					
I_A	Analog Supply Current	Operating Standby	60 7	**85** **10**	mA (max) mA (max)
I_D	Digital Supply Current	Operating Standby	4.7 0.1	**10** **1.0**	mA (max) mA (max)

DC and Logic Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=+5.0V_{DC}, $V_{DI/O}$**=+5.0 or +3.3V_{DC}, **$V_{REF\ IN}$** = +2.0V_{DC}, **f_{MCLK}**=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
$I_{DI/O}$	Digital I/O Supply Current	Operating, $V_{DI/O}$=5.0V	12	**30**	mA (max)
		Standby, $V_{DI/O}$= 5.0V	5	**20**	mA (max)
		Operating, $V_{DI/O}$=3.3V	2	**10**	mA (max)
		Standby, $V_{DI/O}$= 3.3V	0.3	**3**	mA (max)

AC Electrical Characteristics, MCLK Independent

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=$V_{DI/O}$=+5.0V_{DC}**, **$V_{REF\ IN}$** = +2.0V_{DC}, **f_{MCLK}**=24MHz, **t_{MCLK}**=1/**f_{MCLK}**, **t_r=t_f=5ns**, R_s=25¾, C_L (databus loading) = 50pF/pin.
Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
f_{MCLK}	Maximum MCLK Frequency			**24**	MHz (min)
	Minimum MCLK Frequency			**4**	MHz (max)
	MCLK Duty Cycle			**40**	% (min)
				60	% (max)
$t_{SETUP\ (OUT)}$	Coefficient Data valid before latching edge of OCLK or GCLK	GCLK and OCLK as outputs	12	**20**	ns (min)
$t_{HOLD\ (OUT)}$	Coefficient Data held after latching edge of OCLK or GCLK	GCLK and OCLK as outputs	-10	**0**	ns (min)
$t_{SETUP\ (IN)}$	Coefficient Data Valid before latching edge of OCLK or GCLK	GCLK and OCLK as inputs	0	**5**	ns (min)
$t_{HOLD\ (IN)}$	Coefficient Data held after latching edge of OCLK or GCLK	GCLK and OCLK as inputs	0	**5**	ns (min)
$t_{GCLK\text{-}\overline{EOC}}$	Rising edge of GLCK to falling edge of $\overline{EOC}$ (GCLK as output)		2		ns
$t_{GCLK\text{-}OCLK}$	Rising edge of GLCK to falling edge of OCLK (GCLK and OCLK as outputs)	2 bus / 2 clock mode	1		ns
$t_{\overline{EOC}\text{-}OCLK}$	Rising edge of $\overline{EOC}$ to rising edge of OLCK (OCLK as output)	2 clock mode	1		ns
$t_{OCLK\text{-}GCLK}$	Rising edge of OLCK to falling edge of GLCK (GCLK and OCLK as outputs)	2 clock mode	3		ns
$t_{\overline{EOC}\text{-}GCLK}$	Rising edge of $\overline{EOC}$ to falling edge of GLCK (GCLK as output)	2 bus mode	2		ns
t_{DACC}	$\overline{RD}$ or $\overline{RD\_PIXEL}$ low to D0-D9 data valid		15	**41**	ns (max)
$t_{D1H,\ D0H}$	$\overline{RD}$ or $\overline{RD\_PIXEL}$ high to D0-D9 data tri-state		13	**20**	ns (max)
$t_{\overline{CS}\ SETUP}$	$\overline{CS}$ setup of $\overline{RD}$ or $\overline{WR}$			**0**	ns (min)
$t_{\overline{CS}\ HOLD}$	$\overline{CS}$ hold after $\overline{RD}$ or $\overline{WR}$			**0**	ns (min)
$t_{\overline{WR}\ SETUP}$	D0-D9 data valid before rising edge of $\overline{WR}$ (setup time)			**5**	ns (min)

AC Electrical Characteristics, MCLK Independent (Continued)

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=$V_{DI/O}$=+5.0**V_{DC}, $V_{REF\ IN}$ = +2.0V_{DC}, f_{MCLK}=24MHz, **t_{MCLK}**=1/f_{MCLK}, **t_r=t_f=5ns**, R_s=25¾, C_L (databus loading) = 50pF/pin.
Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
$t_{\overline{WR}\ HOLD}$	D0-D9 data valid after rising edge of $\overline{WR}$ (hold time)			**0**	ns (min)

AC Electrical Characteristics, MCLK Dependent

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=$V_{DI/O}$=+5.0**V_{DC}, $V_{REF\ IN}$ = +2.0V_{DC}, f_{MCLK}=24MHz, **t_{MCLK}**=1/f_{MCLK}, **t_r=t_f=5ns**, R_s=25Ω, C_L (databus loading) = 50pF/pin. Refer to Table 2: Configuration Register Parameters for limits labeled C.R. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
$t_{R/\overline{S}\ START}$	Rising edge of RUN/$\overline{STOP}$ to Rising edge of SYNC	SYNC OUT mode		**16**	MCLKs (max)
t_{START}	Rising edge of SYNC to rising edge of TR1	SYNC IN mode SYNC IN mode SYNC OUT mode	1+$t_{GUARDBAND}$ 13+$t_{GUARDBAND}$ $t_{GUARDBAND}$	**$t_{GUARDBAND}$** **14+$t_{GUARDBAND}$** **$t_{GUARDBAND}$**	MCLKs (min) MCLKs (max) MCLKs
$t_{SYNC\ END}$	Falling edge of SYNC to last rising edge of $\overline{EOC}$	SYNC IN mode SYNC OUT mode	8 0	**9** **0**	MCLKs (max) MCLKs (max)
$t_{SYNC\ LOW}$	SYNC low time	SYNC IN mode SYNC OUT mode		**8** **# of EOL PIxels - 4**	MCLKs (min) Pixel periods
$t_{TR1\ WIDTH}$, $t_{TR2\ WIDTH}$	TR1, TR2 Transfer Pulse Width			**C.R.**	MCLKs
t_{GUARD}	TR1, TR2 Transfer Pulse Guardband			**C.R.**	MCLKs
$t_{RS\ WIDTH}$	Reset Pulse Width			**C.R.**	MCLKs
$t_{CLAMP\ ON}$	Start of Optical Black clamping period			**C.R.**	MCLKs
$t_{CLAMP\ OFF}$	End of Optical Black clamping period			**C.R.**	MCLKs
$t_{Ø}$	Ø1, Ø2 clock period	Standard Mode Even/Odd Mode		**12** **24**	MCLKs MCLKs
t_{RS}	RS pulse position from Ø1 edge			**C.R.**	MCLKs
$t_{HOLD\ REF}$	Reference hold (sample) position from RS edge			**C.R.**	MCLKs
$t_{HOLD\ SIG}$	Signal hold (sample) position from RS edge			**C.R.**	MCLKs
$t_{OCLK\ LOW}$	OCLK low time (OCLK as Output)	2 bus mode 1bus mode		**2*t_{MCLK}** **1*t_{MCLK}**	ns
$t_{OCLK\ HIGH}$	OCLK high time (OCLK as Output)	2 bus mode 1 bus mode		**2*t_{MCLK}** **3*t_{MCLK}**	ns
$t_{GCLK\ LOW}$	GCLK low time (GCLK as Output)	2 bus mode 1 bus mode		**2*t_{MCLK}** **1*t_{MCLK}**	ns
$t_{GCLK\ HIGH}$	GCLK high time (GCLK as Output)	2 bus mode 1 bus mode		**2*t_{MCLK}** **3*t_{MCLK}**	ns

AC Electrical Characteristics, MCLK Dependent (Continued)

The following specifications apply for AGND=DGND=$DGND_{I/O}$=0V, **V_A=V_D=$V_{DI/O}$=+5.0V_{DC}**, $V_{REF\ IN}$ = +2.0V_{DC}, f_{MCLK}=24MHz, **t_{MCLK}=1/f_{MCLK}, t_r=t_f=5ns**, R_s=25Ω, C_L (databus loading) = 50pF/pin. Refer to Table 2: Configuration Register Parameters for limits labeled C.R. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
$t_{\overline{EOC}\ LOW}$	$\overline{EOC}$ low time			**2*t_{MCLK}**	ns
$t_{\overline{EOC}\ HIGH}$	$\overline{EOC}$ high time			**2*t_{MCLK}**	ns
$t_{DATA\ VALID}$	D0-D9 data valid from falling (Data Read Phase = 0°) or rising (Data Read Phase = 180°) edge of $\overline{EOC}$			**4*t_{MCLK}-20ns**	ns (min)
$t_{OCLK\text{-}\overline{EOC}\ 1}$ (OCLK IN)	OCLK rising edge to EOC falling edge (Gain Coefficient Write Phase = 0°), OCLK falling edge to EOC falling edge (Gain Coefficient Write Phase = 180°)	1 bus mode w/ext OCLK		**t_{MCLK} + 40ns** **4*t_{MCLK}**	ns (min) ns (max)
$t_{OCLK\text{-}\overline{EOC}\ 2}$ (OCLK IN)	OCLK rising edge to EOC rising edge (Gain Coefficient Write Phase = 0°), OCLK falling edge to EOC rising edge (Gain Coefficient Write Phase = 180°)	2 bus mode w/ext OCLK		**40ns** **3*t_{MCLK}**	ns (min) ns (max)
$t_{GCLK\text{-}\overline{EOC}}$ (GCLK IN)	GCLK rising edge to EOC falling edge (Gain Coefficient Write Phase = 0°), GCLK falling edge to EOC falling edge (Gain Coefficient Write Phase = 180°)	w/ext GCLK		**40ns** **3*t_{MCLK}**	ns (min) ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND=AGND=DGND=$DGND_{I/O}$=0V, unless otherwise specified.

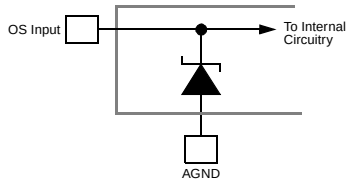
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}<GND or V_{IN}>V_A or V_D), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A) / \Theta_{JA}$. $T_J$max = 150°C for this device. The typical thermal resistance (Θ_{JA}) of this part when board mounted is 52°C/W for the V52A PLCC package.

Note 5: Human body model, 100pF capacitor discharged through a 1.5kΩ resistor.

Note 6: See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: A Zener diode clamps the OS analog inputs to AGND as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the sensor, prevents damage to the LM9812 from transients during power-up.



Note 8: To guarantee accuracy, it is required that V_A and V_D be connected together to the same power supply with separate bypass capacitors at each supply pin.

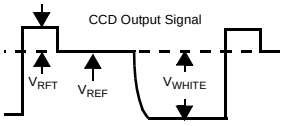
Note 9: Typicals are at T_J=T_A=25°C, f_{MCLK} = 24MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

Note 12: V_{REF} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{REF} . V_{RFT} is defined as the peak positive deviation above V_{REF} of the reset feedthrough pulse. The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the

LM9812 can correct for using its internal PGA.



Note 13: Reference voltages below 1.80V may decrease SNR. Reference voltages above 2.20V may cause linearity (headroom) errors inside the LM9812. The LM4041DIM3-ADJ (SOT-23 package) or the LM4041DIZ-ADJ (TO-92 package) bandgap voltage references are recommended for this application.

Note 14: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula $Gain_{PGA}\left(\frac{V}{V}\right) = G_0 + X\frac{\text{PGA code}}{32}$ where $X = (G_{31} - G_0)\frac{32}{31}$.

Pin Descriptions

Sensor Driver Signals	
ø1	Digital Output. Clock signal, phase 1.
ø2	Digital Output. Clock signal, phase 2.
RS	Digital Output. Reset pulse.
TR1, TR2	Digital Output. Transfer pulses.
Analog I/O	
OS_R, OS_G, OS_B,	Analog Inputs. These inputs (for Red, Green, and Blue) should be tied to the sensor's OS (Output Signal) through DC blocking capacitors.
$V_{REF\ IN}$	Analog Input. This is the system reference voltage input and should be connected to a 2.0V voltage source and bypassed to AGND with a 0.05µF monolithic capacitor.
$V_{REF\ LO\ OUT}$, $V_{REF\ LO\ IN}$	Analog Output/Input. $V_{REF\ LO\ OUT}$ is a voltage equal to $0.49V_A$ - $V_{REF\ IN}/2$ (1.45V for $V_{REF\ IN}$=2V) developed by the LM9812. It should be tied to $V_{REF\ LO\ IN}$ and bypassed to AGND with a 0.05µF monolithic capacitor.
$V_{REF\ MID\ OUT}$, $V_{REF\ MID\ IN}$	Analog Output/Input. $V_{REF\ MID\ OUT}$ is a voltage equal to $0.49V_A$ (2.45V for $V_{REF\ IN}$=2V) developed by the LM9812. It should be tied to $V_{REF\ MID\ IN}$ and bypassed to AGND with a 0.05µF monolithic capacitor.
$V_{REF\ HI\ OUT}$, $V_{REF\ HI\ IN}$	Analog Output/Input. $V_{REF\ HI\ OUT}$ is a voltage equal to $0.49V_A$ + $V_{REF\ IN}/2$ (3.45V for $V_{REF\ IN}$=2V) developed by the LM9812. It should be tied to $V_{REF\ HI\ IN}$ and bypassed to AGND with a 0.05µF monolithic capacitor.
Configuration Register I/O	
$\overline{CS}$	Digital Input. This is the Chip Select signal for reading or writing to the Configuration Register through the D0-D9 databus. This input must be low in order to enable writing to or reading from the Configuration Register.
$\overline{RD}$	Digital Input. A low signal on this input, when SYNC and $\overline{CS}$ are also low, places the data in the currently addressed Configuration Register on the D0-D9 databus. A $\overline{RD}$ cycle also resets the internal address latching state machine. NOTE: If this pin is taken low when CS is high, the D0-D9 databus will come out of tri-state and drive random data onto the bus.
$\overline{WR}$	Digital Input. This input, when simultaneously asserted along with $\overline{CS}$, transfers the data on the D0-D9 databus to the LM9812. If this is the first write in the cycle, this data is the address to be read or written to. If this is the second write in the cycle, this data is the data to be written to the Configuration Register at the currently latched address. Writing to the Configuration Register is independent of the state of SYNC.

General Digital I/O	
MCLK	Digital Input. This is the 24MHz (typical) master system clock.
SYNC	Digital Input (SYNC_IN mode) / Digital Output (SYNC_OUT mode). In the SYNC_IN mode, a low-to-high transition on this input begins a line scan operation. The line scan operation terminates when SYNC is taken low. In the SYNC_OUT mode, the rising edge of this output indicates the start of a line of data and the falling edge indicates the end of a line of data.
RUN/$\overline{STOP}$	Digital Input. In the SYNC_OUT mode, this input should be taken high to begin converting a series of lines, and taken low to stop converting a series of lines. In the SYNC_IN mode this input is ignored.
Digital Coefficient I/O	
CD0 (LSB) - CD9 (MSB)	Digital Inputs. This is the 10 bit data path for the pixel-rate gain coefficient and offset data.
OCLK	Digital Input/Output. This is the signal that is used to clock the Offset coefficients into the LM9812 through the CD0-CD9 databus. This can be either an output or an input depending on the state of bit 7 of Register 9. Data is latched on the rising edge of OCLK.
GCLK	Digital Input/Output. This is the signal that is used to clock the Shading (gain) coefficients into the LM9812 through the CD0-CD9 databus. This can be either an output or an input depending on the state of bit 7 of Register 9. Data is latched on the rising edge of GCLK.
Digital Output I/O	
D0 (LSB)- D9 (MSB)	Digital Inputs/Outputs. When SYNC is high and $\overline{RD\ PIXEL}$ is low, this data bus outputs the 10 bit digital output data during line scan. This databus is also used for reading or writing to the Configuration Register using the $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ signals. Writing to the Configuration Register can occur at any time. Reading from the Configuration Register can only occur when SYNC is low.
$\overline{EOC}$	Digital Output. This is the End Of Conversion signal from the LM9812 indicating that new pixel data is available on the D0-D9 databus.
$\overline{RD\ PIXEL}$	Digital Input. When SYNC is high, taking this input low places the digital pixel data stored in the output latch onto the D0-D9 bus. This input is ignored when SYNC is low.
Test	
TEST	Analog Output. This pin can be used to view the CDS and Clamp signals. See Register 27, bits 6 and 7.

Analog Power	
V_A	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
AGND	This is the ground return for the analog supply.
Digital Power	
V_D	This is the positive supply pin for the digital supply. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1µF monolithic capacitor.
DGND	This is the ground return for the digital supply.
$V_{DI/O}$	This is the positive supply pin for the digital supply for the LM9812's I/O. It should be connected to a voltage source of +3V to +5V and bypassed to $DGND_{I/O}$ with a 0.1µF monolithic capacitor. If the supply for this pin is different than the supply for V_A and V_D, it should also be bypassed with a 10µF tantalum capacitor.
$DGND_{I/O}$	This is the ground return for the digital supply for the LM9812's I/O.

Timing Diagrams

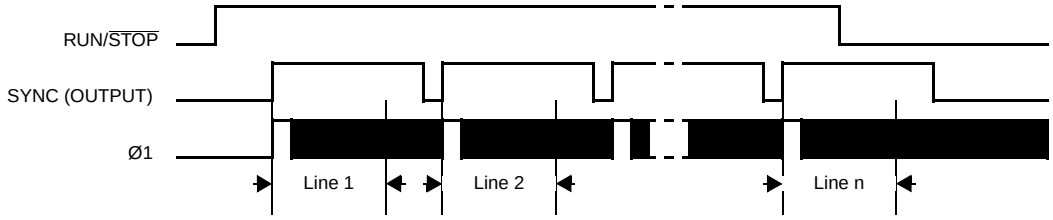


Diagram 1: SYNC OUT Mode Timing, Multiple Lines

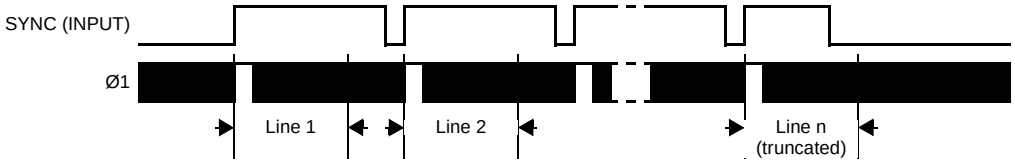


Diagram 2: SYNC IN Mode Timing, Multiple Lines

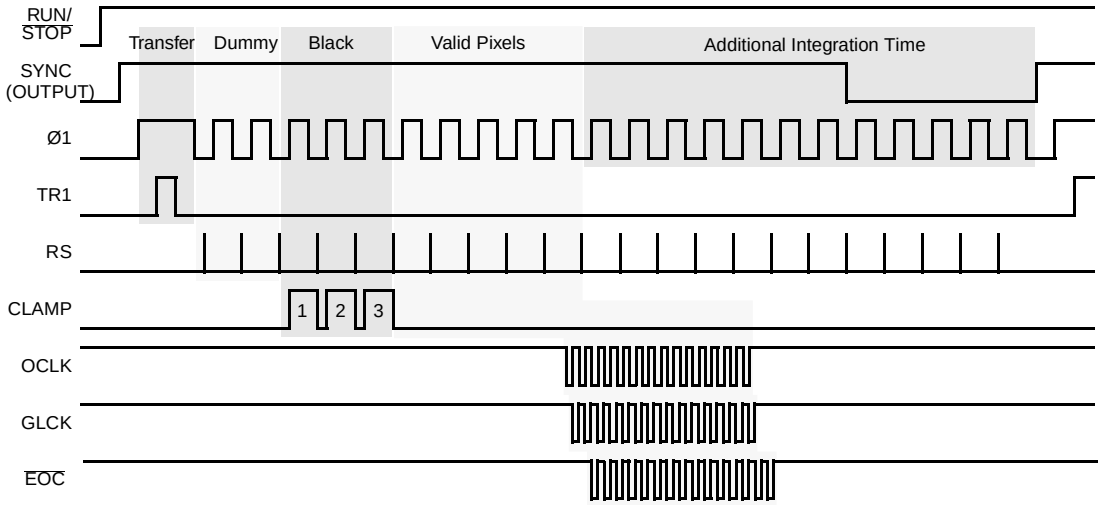


Diagram 3: SYNC OUT Mode Timing, One Line

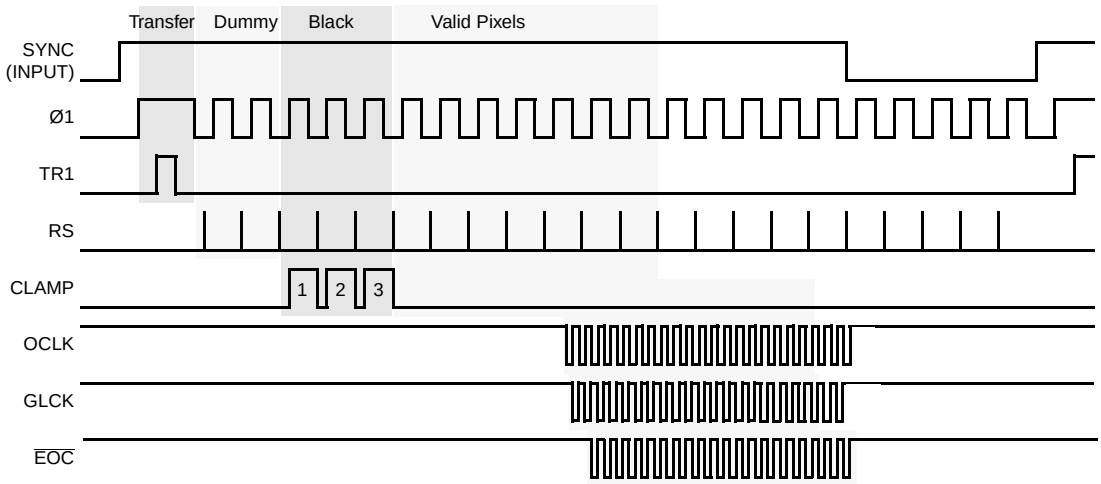


Diagram 4: SYNC In Mode Timing, One Line

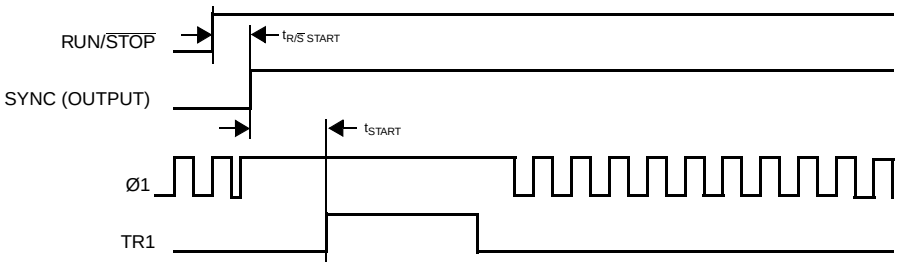


Diagram 5: Start of Line Scan, SYNC OUT Mode, One TR Pulse

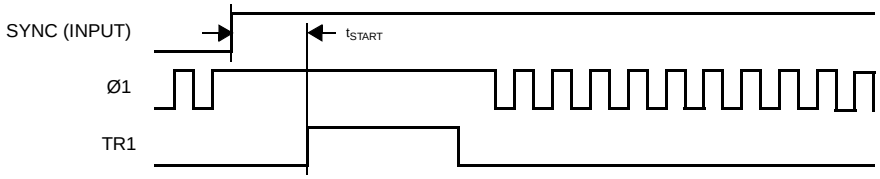


Diagram 6: Start of Line Scan, SYNC IN Mode, One TR Pulse

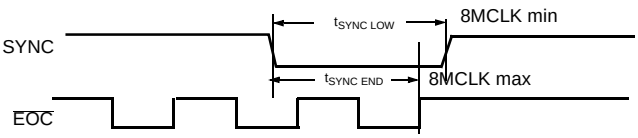


Diagram 7: Timing for End of Line/Start of Next Line

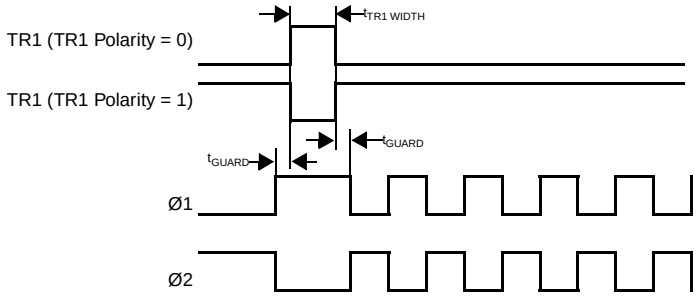


Diagram 8: TR Pulse Timing, One TR Pulse

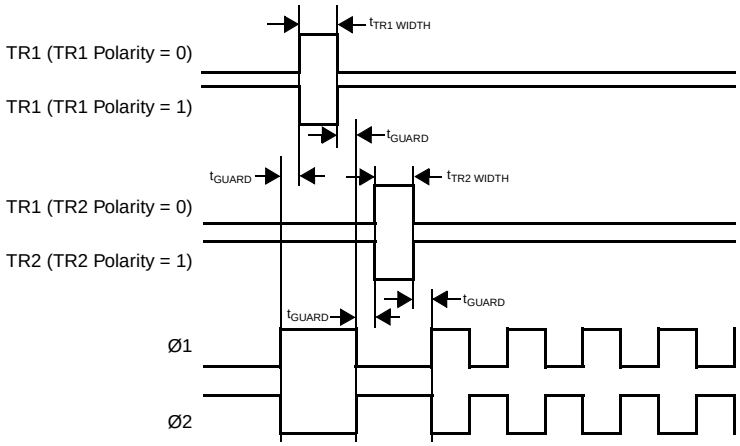


Diagram 9: TR Pulse Timing, Two TR Pulses

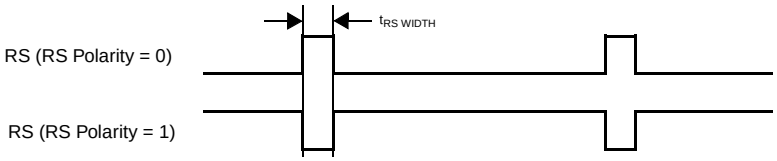


Diagram 10: RS Pulse Polarity

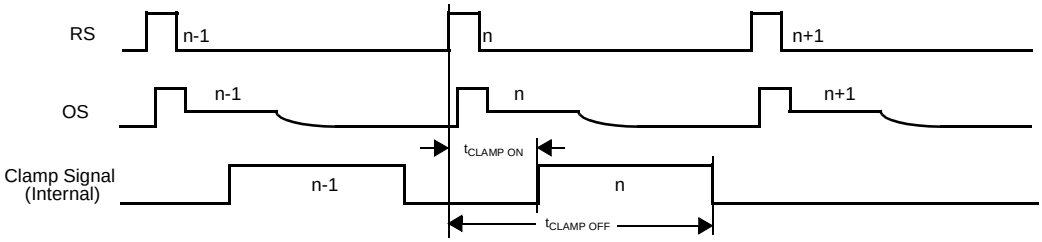


Diagram 11: CCD Clamping Timing

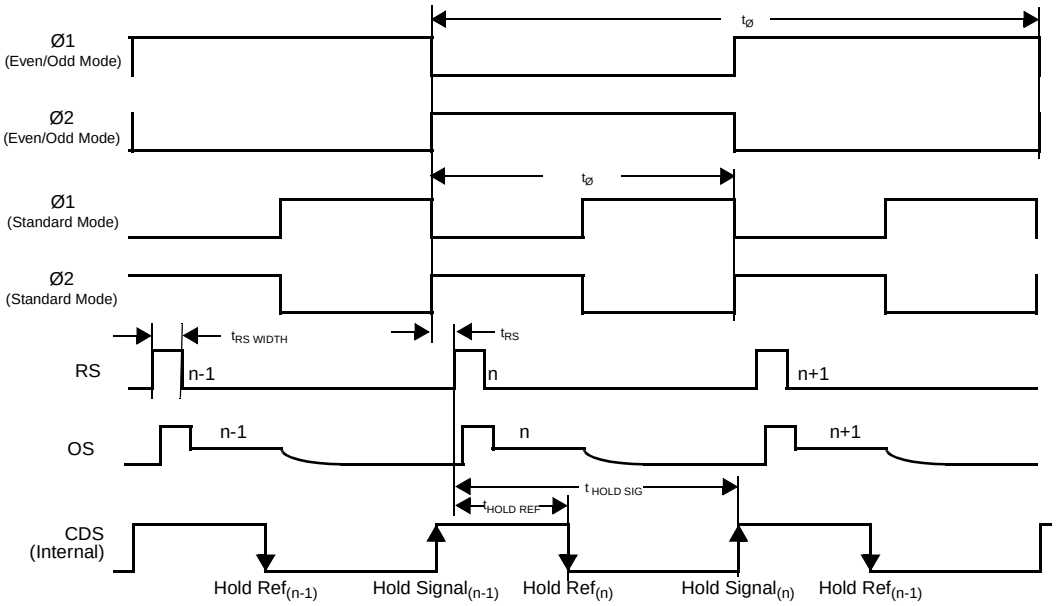
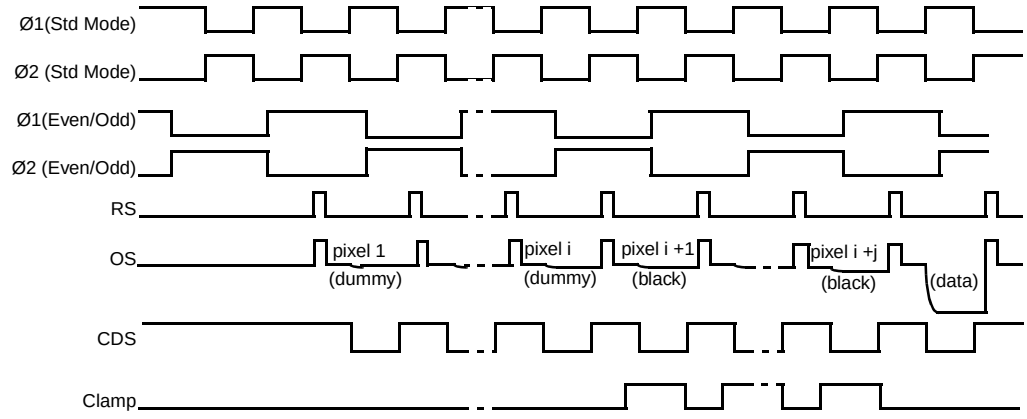


Diagram 12: CDS Timing



Note: i = value programmed in Dummy Pixel Register
j = value programmed in Optical Black Register

Diagram 13: Dummy Pixel and Optical Black Pixel Timing

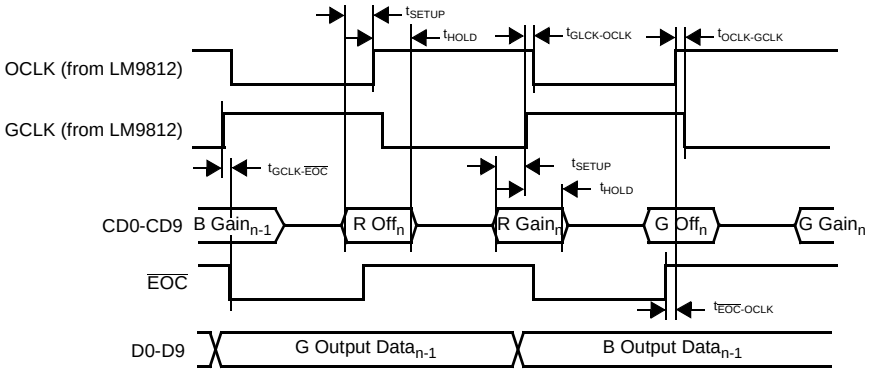


Diagram 14: Digital Data Timing, Output Data and Coefficient Data on separate buses, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK generated by LM9812, RD PIXEL held low.

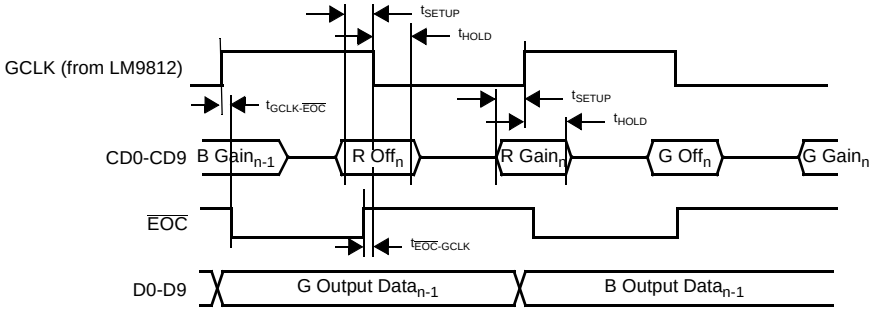


Diagram 15: Digital Data Timing, output data and coefficient data on separate buses, one clock (GCLK) for coefficient data, GCLK generated by LM9812, RD PIXEL held low.

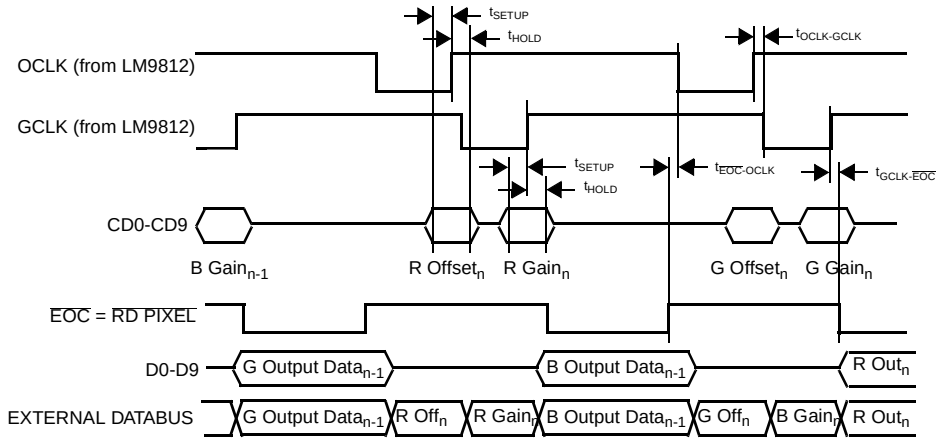


Diagram 16: Digital Data Timing, output data and coefficient data on same buses, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK generated by LM9812.

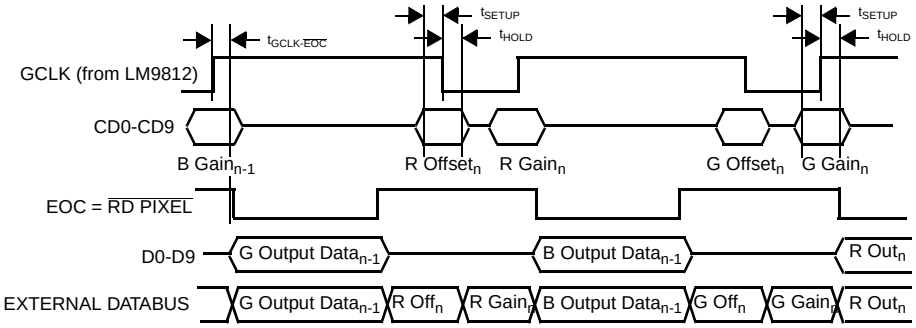


Diagram 17: Digital Data Timing, output data and coefficient data on same buses, one clock (GCLK) for coefficient data, GCLK generated by LM9812.

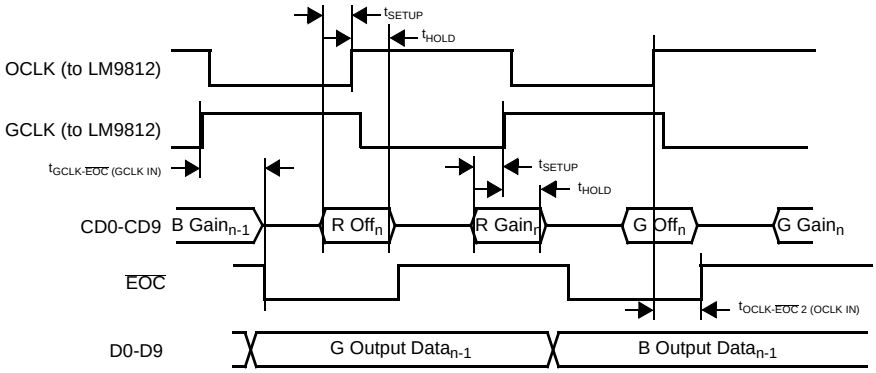


Diagram 18: Digital Data Timing, output data and coefficient data on separate buses, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK input to LM9812, OCLK and GLCK phase = 0°, RD PIXEL held low.

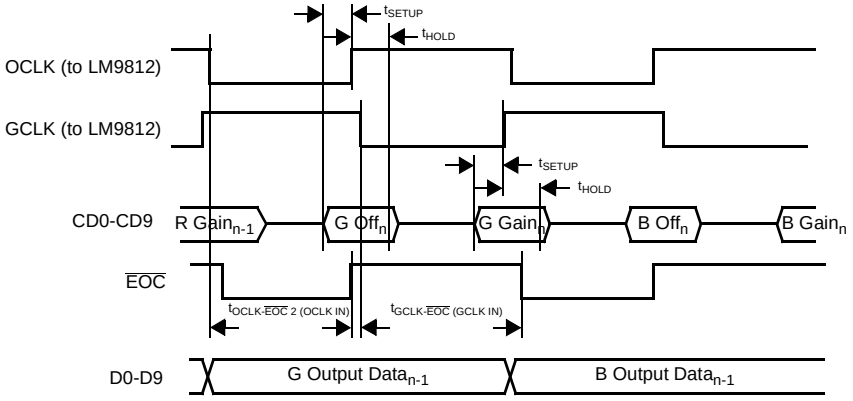


Diagram 19: Digital Data Timing, output data and coefficient data on separate buses, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK input to LM9812, OCLK and GLCK phase = 180°, RD PIXEL held low.

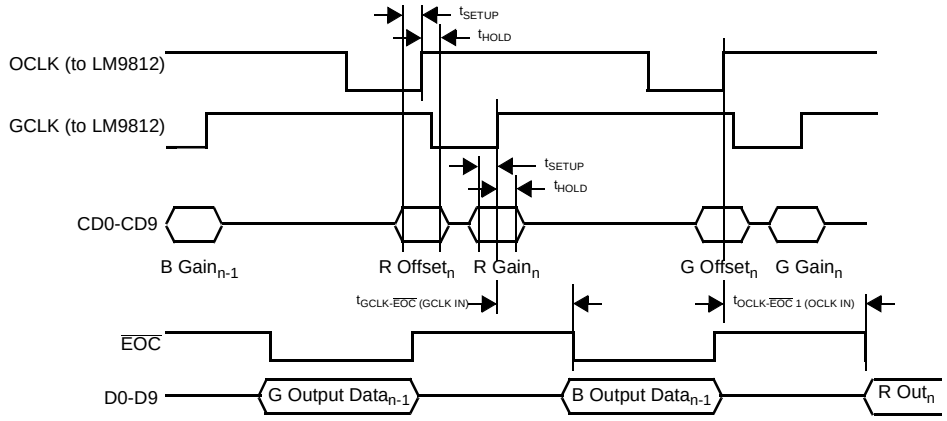


Diagram 20: Digital Data Timing, output data and coefficient data on same bus, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK input to LM9812, OCLK and GLCK phase = 0°.

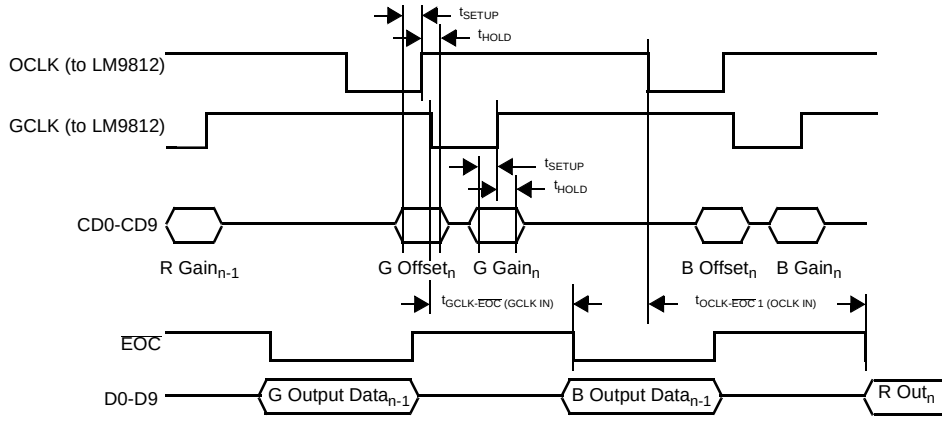


Diagram 21: Digital Data Timing, output data and coefficient data on same bus, two clocks (OCLK and GCLK) for coefficient data, OCLK and GCLK input to LM9812, OCLK and GLCK phase = 180°.

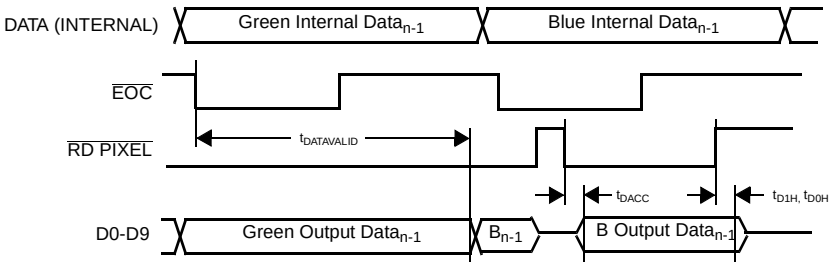


Diagram 22: $\overline{\text{RD PIXEL}}$ Output Timing (Data Read Phase = 0°)

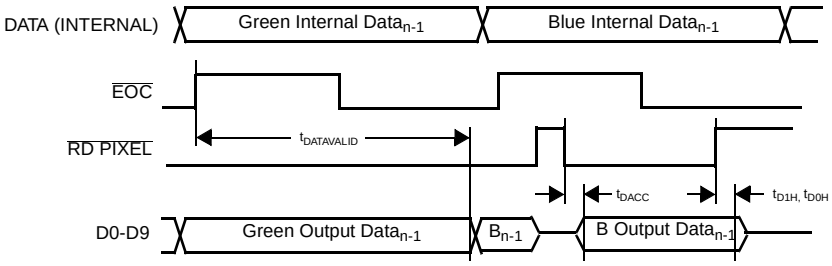
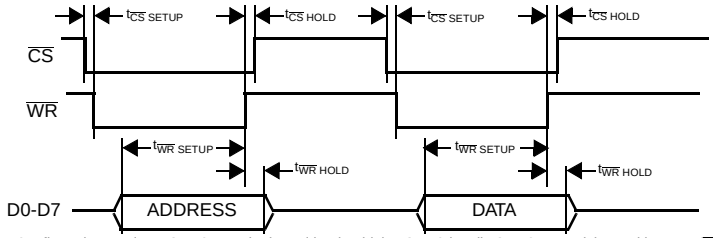
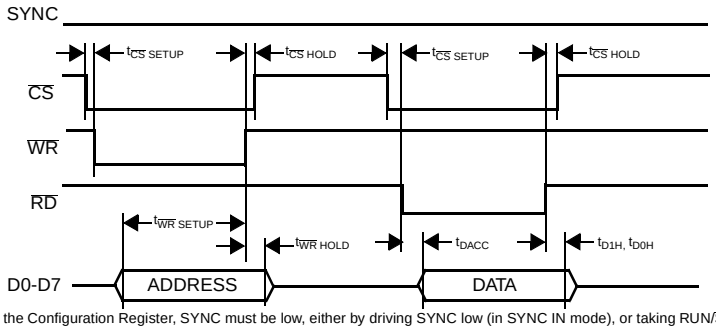


Diagram 23: $\overline{RD\ PIXEL}$ Output Timing (Data Read Phase = 180°)



Note: To read from the Configuration Register, SYNC must be low, either by driving SYNC low (in SYNC IN mode), or taking RUN/$\overline{STOP}$ low and waiting for SYNC to go low at the end of a line (in SYNC OUT mode). The Configuration Register can be written to independent of the state of SYNC.

Diagram 24: Writing to the Configuration Register, $\overline{RD}$ held high.



Note: To read from the Configuration Register, SYNC must be low, either by driving SYNC low (in SYNC IN mode), or taking RUN/$\overline{STOP}$ low and waiting for SYNC to go low at the end of a line (in SYNC OUT mode). The Configuration Register can be written to independent of the state of SYNC.

Diagram 25: Reading the Configuration Register

Table 1: Configuration Register Address Table

Address (Decimal)	Address (Binary)					Data Bits							
	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	Static Offset (Red)							
						-	-	Sign	MSB				LSB
1	0	0	0	0	1	Static Offset (Green)							
						-	-	Sign	MSB				LSB
2	0	0	0	1	0	Static Offset (Blue)							
						-	-	Sign	MSB				LSB
3	0	0	0	1	1	Coarse Color Balance PGA (Red)							
						-	-	-	MSB				LSB
4	0	0	1	0	0	Coarse Color Balance PGA (Green)							
						-	-	-	MSB				LSB
5	0	0	1	0	1	Coarse Color Balance PGA (Blue)							
						x3	-	-	MSB				LSB
6	0	0	1	1	0	Internal Offset Subtractor Coefficient							
						MSB							LSB
7	0	0	1	1	1	Internal Gain Multiplier Coefficient							
													LSB
8	0	1	0	0	0	Internal Gain Multiplier Coefficient (LM9812 only)							
						-	-	-	-	-	-	MSB	
9	0	1	0	0	1	Misc Group 1							
						Internal External Coefficient Clock	-	Number of Coefficient Clocks	Number of Databusses in System	Multiplier Gain Range 1	Multiplier Gain Range 0	Multiplier Coefficient Source	Offset Coefficient Source
10	0	1	0	1	0	Number of Dummy Pixels							
						MSB							LSB
11	0	1	0	1	1	Number of Optical Black Pixels							
						MSB							LSB
12	0	1	1	0	0	Number of Active Pixels (LSB)							
													LSB
13	0	1	1	0	1	Number of Active Pixels (MSB)							
						-	-	MSB					
14	0	1	1	1	0	Number of End of Line Integration Pixels (LSB)							
													LSB
15	0	1	1	1	1	Number of End of Line Integration Pixels (MSB)							
						-	-	MSB					
16	1	0	0	0	0	TR1 Pulse Duration							
						-	-	MSB					LSB
17	1	0	0	0	1	TR2 Pulse Duration							
						-	-	MSB					LSB
18	1	0	0	1	0	TR1/TR2 Guardbands							
						-	-	MSB					LSB
19	1	0	0	1	1	Optical Black Clamp Start							
						-	-	-	MSB				LSB
20	1	0	1	0	0	Optical Black Clamp End							
						-	-	-	MSB				LSB

Address (Decimal)	Address (Binary)					Data Bits							
	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
21	1	0	1	0	1	Reset Pulse Width			Reset Pulse Position				
						Bit 2		Bit 0	Bit 4				Bit 0
22	1	0	1	1	0	Reference Sample Position							
						-	-	-	Bit 4				Bit 0
23	1	0	1	1	1	Signal Sample Position							
						-	-	-	Bit 4				Bit 0
24	1	1	0	0	0	Misc Group 2							
						Signal Polarity	Preview 1	Preview 2	Internal/ External SYNC pulse	TR Pulse Mode (1 or 2 Pulses)	Red/Blue Order for 2 Output sensors	3 or 2 Output sensor	Standard or Odd/Even sensor
25	1	1	0	0	1	Misc Group 3							
						Power Down	8 or 10 bit Coefficient Bus	-	TR2 Enable	TR1 Enable	RS Enable	Ø2 Enable	Ø1 Enable
26	1	1	0	1	0	Misc Group 4							
						Gain Coefficient Write Phase	Offset Coefficient Write Phase	Data Read Phase	Ø1 Polarity During TR1	TR2 Pulse Polarity	TR1 Pulse Polarity	RS Pulse Polarity	Ø1/Ø2 Polarity
27	1	1	0	1	1	Test Mode 1							
						TB7	TB6	0	0	0	0	0	0
28	1	1	1	0	0	Test Mode 2							
						0	0	0	0	0	0	0	0

Table 2: Configuration Register Parameters

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits							Result
	D5 (SIGN)	**D4 (MSB)**	**D3**	**D2**	**D1**	**D0 (LSB)**		**Typical Offset (in ADC LSBs)**
	0	0	0	0	0	0		0.00
Red	0	0	0	0	0	1		+4.2
Offset DAC (0)	0	0	0	0	1	0		+8.4
	• • •	• • •	• • •	• • •	• • •	• • •		• • •
Green	0	1	1	1	1	0		+126.0
Offset DAC (1)	0	1	1	1	1	1		+130.2
	1	0	0	0	0	0		0.00
Blue	1	0	0	0	0	1		-4.2
Offset DAC (2)	1	0	0	0	1	0		-8.4
	• • •	• • •	• • •	• • •	• • •	• • •		• • •
	1	1	1	1	1	0		-126.0
	1	1	1	1	1	1		-130.2

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits								Result
Red PGA (3)	**D7**			**D4 (MSB)**	**D3**	**D2**	**D1**	**D0 (LSB)**	**Typical Gain (V/V)**
	0			0	0	0	0	0	0.93
Green PGA	0			0	0	0	0	1	1.00
(4)	0			0	0	0	1	0	
	• • •			• • •	• • •	• • •	• • •	• • •	• • •
Blue PGA	0			1	1	1	0	1	
(5)	0			1	1	1	1	0	
	0			1	1	1	1	1	3.00
	D7			**D4 (MSB)**	**D3**	**D2**	**D1**	**D0 (LSB)**	**Typical Gain (V/V)**
Coarse Color	1			0	0	0	0	0	2.79
Balance PGA	1			0	0	0	0	1	3.00
(Blue with x3	1			0	0	0	1	0	
multiplier bit set)	• • •			• • •	• • •	• • •	• • •	• • •	• • •
(5)	1			1	1	1	0	1	
	1			1	1	1	1	0	
	1			1	1	1	1	1	9.00
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**	**Offset (in ADC LSBs)**
Internal	0	0	0	0	0	0	0	0	0
Offset	0	0	0	0	0	0	0	1	1
Subtractor	0	0	0	0	0	0	1	0	2
Coefficient	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
(6)	1	1	1	1	1	1	0	1	253
	1	1	1	1	1	1	1	0	254
	1	1	1	1	1	1	1	1	255
	D9 (MSB)	**D8**	**D7**	• • •	• • •	**D2**	**D1**	**D0 (LSB)**	**Gain (V/V)**
Internal	0	0	0			0	0	0	
Multiplier	0	0	0			0	0	1	
Gain	0	0	0			0	1	0	See
Coefficient	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	Equation 5
(7, 8)	1	1	1			1	0	1	
	1	1	1			1	1	0	
	1	1	1			1	1	1	
Internal/External Coefficient Clocks (9)	**D7**								
	0						External Coefficient Clock Source		
	1						Internal Coefficient Clock Source		
Number of Coefficient Clocks (9)	**D5**								
	0						GCLK and OCLK		
	1						GCLK only		
Number of Databuses in System (9)	**D4**								
	0						2 Databuses		
	1						1 Databus		

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits								Result
Multiplier Gain Range (9)	**D3** 0 0 1 1	**D2** 0 1 0 1							Range 0, 67% (1:3) Range 1, 50% (1:2) Range 2, 33% (1:1.5) Not Used
Multiplier Coefficient Source (9)	**D1** 0 1								External CD0-CD9 Bus Internal Register
Offset Coefficient Source (9)	**D0** 0 1								External CD0-CD9 Bus Internal Register
Dummy Pixels (Minimum Value is 0) **(10)**	**D7** 0 0 0 • • • 1 1 1	**D6** 0 0 0 • • • 1 1 1	**D5** 0 0 0 • • • 1 1 1	**D4** 0 0 0 • • • 1 1 1	**D3** 0 0 0 • • • 1 1 1	**D2** 0 0 0 • • • 1 1 1	**D1** 0 0 1 • • • 0 1 1	**D0** 0 1 0 • • • 1 0 1	 0 1 2 • • • 253 254 255
Optical Black Pixels (Minimum Value is 1) **(11)**	**D7** 0 0 0 • • • 1 1 1	**D6** 0 0 0 • • • 1 1 1	**D5** 0 0 0 • • • 1 1 1	**D4** 0 0 0 • • • 1 1 1	**D3** 0 0 0 • • • 1 1 1	**D2** 0 0 0 • • • 1 1 1	**D1** 0 1 1 • • • 0 1 1	**D0** 1 0 1 • • • 1 0 1	 1 2 3 • • • 253 254 255
Active Pixels (Minimum Value is 0) **(12, 13)**	**D13 (MSB)** 0 0 0 • • • 1 1 1	**D12** 0 0 0 • • • 1 1 1	**D11** 0 0 0 • • • 1 1 1	• • • • • • 	• • • • • • 	**D2** 0 0 0 • • • 1 1 1	**D1** 0 0 1 • • • 0 1 1	**D0 (LSB)** 0 1 0 • • • 1 0 1	**Active Pixels** 0 1 2 • • • 16381 16382 16383
End of Line Integration Pixels (Minimum Value is 5) **(14, 15)**	**D13 (MSB)** 0 0 0 • • • 1 1 1	**D12** 0 0 0 • • • 1 1 1	**D11** 0 0 0 • • • 1 1 1	• • • • • • 	• • • • • • 	**D2** 1 1 1 • • • 1 1 1	**D1** 0 1 1 • • • 0 1 1	**D0 (LSB)** 1 0 1 • • • 1 0 1	**End-of-Line Pixels** 5 6 7 • • • 16381 16382 16383

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits							Result
	D5 (MSB)	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**	= $(x/2)t_{pixel}$, where $t_{pixel} = 12t_{MCLK}$ for	**TR Pulse Width**
TR1 Pulse Duration (16)	0	0	0	0	0	0	3 channel mode,	0.5 t_{pixel}
	0	0	0	0	0	1	$t_{pixel} = 8t_{MCLK}$ for 2	0.5 t_{pixel}
	0	0	0	0	1	0	channel mode	1.0 t_{pixel}
TR2 Pulse Duration (17)	• • •	• • •	• • •	• • •	• • •	• • •	(except for x = 0:	• • •
	1	1	1	1	0	1	duration for x = 0 is	30.5 t_{pixel}
	1	1	1	1	1	0	0.5tpixel, same as	31.0 t_{pixel}
	1	1	1	1	1	1	for x = 1)	31.5 t_{pixel}
	D5 (MSB)	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**	= $(x/2)t_{pixel}$, where $t_{pixel} = 12t_{MCLK}$ for	**TR Guardband**
	0	0	0	0	0	0	3 channel mode,	0.5 t_{pixel}
	0	0	0	0	0	1	$t_{pixel} = 8t_{MCLK}$ for 2	0.5 t_{pixel}
TR1/TR2 - Ø1 Guardband (18)	0	0	0	0	1	0	channel mode	1.0 t_{pixel}
	• • •	• • •	• • •	• • •	• • •	• • •	(except for x = 0:	• • •
	1	1	1	1	0	1	guardband for x = 0	30.5 t_{pixel}
	1	1	1	1	1	0	is 0.5tpixel, same	31.0 t_{pixel}
	1	1	1	1	1	1	as for x = 1)	31.5 t_{pixel}
	D4 (MSB)	**D3**	**D2**	**D1**	**D0 (LSB)**			**Clamp Start (1/(2*f_{MCLK}))**
	0	0	0	0	0			0
	0	0	0	0	1			1
Optical Black Clamp Start Position (Must be Š RS Pulse Width) **(19)**	0	0	0	1	0			2
	• • •	• • •	• • •	• • •	• • •			• • •
	1	1	1	0	1			29
	1	1	1	1	0			30
	1	1	1	1	1			31
	D4 (MSB)	**D3**	**D2**	**D1**	**D0 (LSB)**			**Clamp Stop (1/(2*f_{MCLK}))**
	0	0	0	0	0			0
	0	0	0	0	1			1
Optical Black Clamp Stop Position (20)	0	0	0	1	0			2
	• • •	• • •	• • •	• • •	• • •			• • •
	1	1	1	0	1			29
	1	1	1	1	0			30
	1	1	1	1	1			31
	D7 (MSB)	**D6**	**D5 (LSB)**					**RS Pulse Width (1/(2*f_{MCLK}))**
	0	0	1					1
	0	1	0					2
Reset Pulse Width (Minimum Value Is 1) **(21)**	0	1	1					3
	1	0	0					4
	1	0	1					5
	1	1	0					6
	1	1	1					7

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits						Result
Reset Pulse Position (21)	D4 (MSB)	D3	D2	D1	D0 (LSB)		Reset Position (1/(2*f_{MCLK}))
	0	0	0	0	0		0
	0	0	0	0	1		1
	0	0	0	1	0		2
	• • •	• • •	• • •	• • •	• • •		• • •
	1	1	1	0	1		29
	1	1	1	1	0		30
	1	1	1	1	1		31
Reference Sample Position (22)	D4 (MSB)	D3	D2	D1	D0 (LSB)		Reference Position (1/(2*f_{MCLK}))
	0	0	0	0	0		0
	0	0	0	0	1		1
	0	0	0	1	0		2
	• • •	• • •	• • •	• • •	• • •		• • •
	1	1	1	0	1		29
	1	1	1	1	0		30
	1	1	1	1	1		31
Signal Sample Position (23)	D4 (MSB)	D3	D2	D1	D0 (LSB)		Signal Position (1/(2*f_{MCLK}))
	0	0	0	0	0		0
	0	0	0	0	1		1
	0	0	0	1	0		2
	• • •	• • •	• • •	• • •	• • •		• • •
	1	1	1	0	1		29
	1	1	1	1	0		30
	1	1	1	1	1		31
Signal Polarity (24)	D7						
	0						Negative, CDS On (CCD)
	1						Positive, CDS Off (CIS)
Preview Mode (24)	D6	D5					
	0	0					Normal Operation
	0	1					Normal Operation
	1	0					2x Speed
	1	1					4x Speed
SYNC Pulse (24)	D4						
	0						Externally Supplied (SYNC is Input)
	1						Internally Generated (SYNC is Output)
TR Pulses (24)	D3						
	0						1 TR Pulse (TR1)
	1						2 TR Pulses (TR1 and TR2)
Red/Blue Order for GRGB CCDs (24)	D2						
	0						GR First
	1						GB First
Sensor Type (24)	D1						
	0						Dual Output (RG-BG)
	1						Triple Output (R-G-B)

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

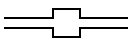
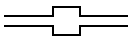
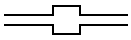
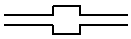
Parameter (Address)	Control Bits		Result
Sensor Type (24)	**D0** 0 1		 Standard Even/Odd
Power Down (25)	**D7** 0 1		 Operating Low Power Standby Mode
Coefficient Bus Width (25)	**D6** 0 1	In 8 bit mode, coefficient data is 8 bits wide, input through CD0-CD7.	 10 bit 8 bit
TR2 Enable (25)	**D4** 0 1		 TR2 Enabled TR2 Disabled
TR1 Enable (25)	**D3** 0 1		 TR1 Enabled TR1 Disabled
RS Enable (25)	**D2** 0 1		 RS Enabled RS Disabled
Ø2 Enable (25)	**D1** 0 1		 Ø2 Enabled Ø2 Disabled
Ø1 Enable (25)	**D0** 0 1		 Ø1 Enabled Ø1 Disabled
Gain Coefficient Write Phase (26)	**D7** 0 1		 0° 180°
Offset Coefficient Write Phase (26)	**D6** 0 1		 0° 180°
Data Read Phase (26)	**D5** 0 1		 0° 180°
Ø1 Polarity During TR1 (26)	**D4** 0 1		 High Low
TR2 Pulse Polarity (26)	**D3** 0 1		 High Low
TR1 Pulse Polarity (26)	**D2** 0 1		 High Low

Table 2: Configuration Register Parameters (Continued)

Note: $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 24MHz (t_{MCLK} = 41.66ns).

Parameter (Address)	Control Bits								Result
RS Pulse Polarity (26)	**D1** 0 1								High Low
Ø1/Ø2 Polarity (26)	**D0** 0 1								Ø1 High/Ø2 Low Ø1 Low/ Ø2 High
Test Mode (27)	**TB7** 0 0 1	**TB6** 0 1 1	Set bits D0-D5 to 0						Test Output Low Test Output Is CDS Signal Test Output is Clamp Signal
Test Mode (28)	0	0	0	0	0	0	0	0	Set all bits to 0

Applications Information

1.0 THEORY OF OPERATION

The LM9812 removes errors from and digitizes up to 3 channels of linear sensor pixel streams, while providing all the necessary clock signals to drive the sensor. Offset and gain errors are removed at the pixel rate, for individual pixels. Offset errors are removed through correlated double sampling (CDS), an analog offset DAC for large DC offsets, and finally a pixel-rate digital offset subtractor for individual pixel offsets. Gain errors (which may come from any combination of PRNU, uneven illumination, $\cos^4$ effect, RGB filter mismatch, etc.) are removed through the use of a 5 bit PGA in front of the ADC (for coarse gain correction) and a 10x10bit pixel-rate digital multiplier for individual pixel gain errors.

1.1 ANALOG SIGNAL PATH (See Functional Block Diagram)

1.1.1 Clamping and Buffering

The Output Signals (OS) from the image sensor are capacitively coupled to the three (OS_R, OS_G, OS_B) analog inputs of the LM9812. Inside the LM9812, a DC restore operation is performed by clamping the input signal to 2.5V when the input signal is known to be black (during the start of a new line of image data). To eliminate loading of the input signal, the signal is buffered through a source follower before being sent to the CDS section.

1.1.2 CDS

The LM9812 uses a high performance CDS (Correlated Double Sampling) circuit to remove many sources of noise and error from the CCD signal. It also supports CIS image sensors with a single sampling mode for positive-going signals.

Figure 1 shows the output stage of a typical CCD and the resulting output waveform:

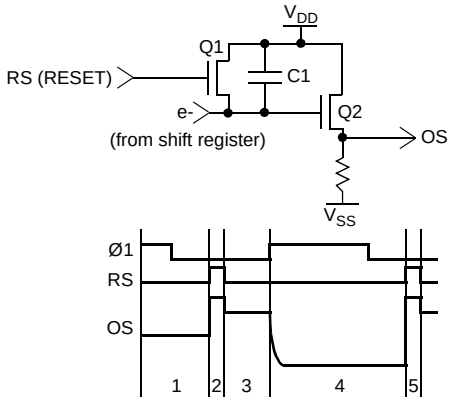


Figure 1: CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 in between every pixel at intervals 2 and 5. When Q1 is on, the output signal (OS) is at its most positive voltage. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ($V_{RESIDUAL}$). $V_{RESIDUAL}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock (Ø1) makes a low to high transition (period 4), the electrons from the next pixel flow into C1. The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{RESIDUAL}$, an error term. If OS is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $V_{RESIDUAL}$ term is canceled and the noise on the signal is reduced ($[V_{SIGNAL}+V_{RESIDUAL}]-V_{RESIDUAL} = V_{SIGNAL}$). This is the principal of Correlated Double Sampling.

The LM9812's CDS circuit acquires a signal within a 1 MCLK window which can be placed anywhere in the pixel period with 0.5 MCLK precision. See Diagram 12 for more detailed timing information.

1.2 CIS Mode

The LM9812 provides some support for CIS (Contact Image Sensor) devices by offering a sampling mode for capturing positive going signals, as opposed to the CCD's negative going signal. The output signal of a CIS sensor (Figure 2) differs from a CCD signal in two primary ways: its output increases with increasing signal strength, and it does not usually have a reference level as an integral part of the output waveform of every pixel.

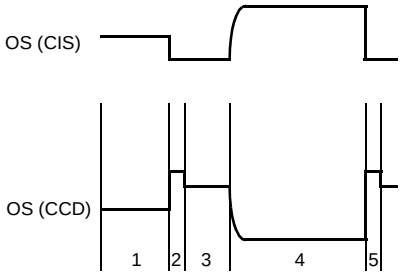


Figure 2: CIS vs. CCD Output signals

When the LM9812 is in CIS mode (Register 24, bit 7=1), it uses the $V_{REF\ MID}$ level as the reference (or black) voltage for each pixel. Since the LM9812 clamps the input signal to $V_{REF\ MID}$ at the black portion at the beginning of every line, the output of the sampler is an accurate and repeatable representation of the that pixel's brightness.

1.2.1 Static PGAs

The output of the CDS stage drives the PGAs (Programmable Gain Amplifiers). Each PGA provides 5 bits of fixed gain correction over a 0.93V/V to 3V/V (-0.6 to 9.5dB) range. The Blue channel has an optional x3 stage for a gain range of 2.8V/V to 9.0V/V (8.9 to 19dB). The gain of each PGA should be set during calibration to bring the maximum amplitude of the strongest pixel to a level just below the desired maximum output from the ADC. The gain is determined by the following equation:

$$\text{Gain}\left(\frac{V}{V}\right) = 0.93 + \frac{\text{PGA code}}{32}2.137$$

Equation 1: PGA Gain

The Blue Channel has an additional gain stage with a gain of 3V/V that may be switched on to compensate for the low amplitude blue output of some sensors. With the x3 bit set (Register 2, bit 7=1), the blue gain is:

$$\text{Gain}\left(\frac{V}{V}\right) = 02.79 + \frac{\text{PGA code}}{32}6.411$$

Equation 2: Blue Channel PGA Gain with x3 Bit Set

This PGA is static - it does not change at the pixel rate. The Pixel-Rate Shading Multiplier is used to eliminate pixel-to-pixel gain errors (typically sensor PRNU and shading errors).

1.2.2 Static Offset DACs

The Static Offset DACs remove DC offsets generated by the sensor and the LM9812's analog signal chain. The DACs should be set during calibration to the lowest value that still results in an ADC output code > 0 for all the pixels. Each LSB of the offset DAC is typically 4.2 ADC LSBs, providing a total offset adjustment range of ±130 ADC LSBs. The equation for the offset DAC is:

$$\text{Offset(ADC LSBs)} = 4.2(\text{DAC Code})$$

Equation 3: Offset DAC

Like the PGA, the Offset DAC is static - it does not change at the pixel rate. The Pixel Rate Offset Subtractor is used to eliminate pixel-to-pixel offset errors.

1.2.3 ADC

The 10 bit ADC quantizes the output from the analog chain and passes the result to the digital section for pixel rate error correction. The ADC's input range is equal to $V_{REF\ IN}/C$, where C is the gain constant compensating for all sources of gain error throughout the entire analog signal path.

1.3 DIGITAL SIGNAL PATH

1.3.1 Pixel-Rate Offset Subtractor

The output of the ADC is fed to the Pixel-Rate Offset Subtractor. Each pixel of image data may have a different offset error. If bit 0 of Register 9 is set to a 0 and a byte representing the offset error code is fed to the Pixel-Rate Offset Subtractor through the CD0-CD9 databus, the offset for each pixel can be subtracted from the ADC output code at the pixel conversion rate. If this feature is not desired, the Offset Subtractor can be set to a fixed value by writing the desired value to Register 6 and setting bit 0 of Register 9 to a 1.

$$\text{Offset Subtractor Out} = \text{ADC Output} - \text{Offset Error Code}$$

Equation 4: Offset Subtractor

The offset subtractor input is 8 bits wide, input on CD0-CD7, for a correction range of 0 to 255. Information on bits CD8 and CD9 is ignored.

1.3.2 Pixel-Rate Shading Multiplier

The Pixel Rate Shading Multiplier follows the Offset Subtractor. This stage compensates for nonuniformities between individual pixels (shading error). Each pixel of image data may have a different gain error. If bit 1 of Register 9 is set to a 0 and a word representing the gain correction coefficient is fed to the Pixel-Rate Shading Multiplier through the CD0-CD9 databus, the gain for each pixel is changed at the pixel rate to eliminate pixel-to-pixel gain errors. If this feature is not desired, the Shading Multiplier can be set to a fixed value by writing the desired gain value to Registers 7 and 8 and setting bit 1 of Register 9 to a 1.

The equation for calculating the gain of the multiplier is given in Equation 5. The Pixel Rate Shading Multiplier has three different gain ranges as shown in **Table 1**. For systems where the ratio of the strongest pixel to the weakest pixel is less than 1.5, the multiplier gain range setting of 1:1.5 provides very accurate control of the gain of each pixel. Systems with larger variation can use gain ranges of 1:2 or 1:3.

$$\text{Multiplier Gain(V/V)} = 1 + \frac{\text{Gain Correction Coefficient}}{N}$$

Equation 5: Shading Multiplier Gain

Multiplier Gain Range	1:1.5 (33%)	1:2.0 (50%)	1:3.0 (67%)
Minimum Gain (V/V, Multiplier Input = 0)	1	1	1
Maximum Gain (V/V, Multiplier Input = 1024)	1.5	2.0	3.0
N (used in Equation 5)	2048	1024	512
Bits D3, D2 of Register 9	1, 0	0, 1	0,0

Table 1:Shading Multiplier: 10 bit Coefficient Bus Width

When the 8 bit Coefficient Bus Width is selected (Register 25, bit 6=1), the coefficient data is only 8 bits wide, supplied on CD0-CD7. This reduces the accuracy of the gain correction, but allows the use of an 8 bit path to store coefficient data, instead of a 10 or 16 bit wide path.

Multiplier Gain Range	1:1.5 (33%)	1:2.0 (50%)	1:3.0 (67%)
Minimum Gain (V/V, Multiplier Input = 0)	1	1	1
Maximum Gain (V/V, Multiplier Input = 256)	1.5	2.0	3.0
N (used in Equation 5)	512	256	128
Bits D3, D2 of Register 9	1, 0	0, 1	0,0

Table 2:Shading Multiplier: 8 bit Coefficient Bus Width

1.4 SENSOR CLOCK GENERATION

The LM9812 generates all of the clock signals required to directly drive most commercial linear CCDs and some CIS - no external clock buffers are necessary. Most linear CCDs designed for scanner applications require 0 to 5V signal swings into 20 to 500pF input loading. Series resistors are typically inserted between the driver and the CCD to control slew rate and isolate the driver from the large load capacitances. The values of these resistors are given in the CCD's datasheet.

1.4.1 TR1 and TR2

The LM9812 supports one or two TR (transfer, or shift) pulses as shown in Diagrams 8 and 9. This pulse is used to transfer the contents of each pixel's photodiode to the CCD's serial shift register for clocking out of the CCD. Configuration Registers 16, 17, and 18 control the TR1, TR2, and TR guardband pulse widths, while Register 24, bit 3 determines whether the LM9812 generates TR1 only or both TR1 and TR2 at the beginning of a line. The polarities of the TR pulses are determined by Register 26, bits 2 and 3. If not needed, one or both TR pulses can be disabled by setting Register 25, bits 3 and 4 to the appropriate value.

1.4.2 RS

The LM9812 also generates the RS (reset) pulse required to clear the CCD's output capacitor of the previous pixel's charge. The RS pulse's width and position (relative to the edge of the ø1 pulse) is determined by the value in Configuration Register 21. See Diagrams 10 and 12. The polarity of the RS pulse is determined by Register 26, bit 1. If not needed, this pulse can be disabled by setting Register 25, bit 2 to a 1.

1.4.3 ø1 and ø2

ø1 and ø2 are the two phase clock for the CCD shift register. ø2 is always the inverse of ø1. For "standard" CCDs, the ø1 and ø2 frequency is equal to the pixel rate, the same frequency as the RS pulse. In Standard Mode, the RS pulse position and Sample Reference/Sample Signal edges are set with respect to the falling edge of ø1. For "even/odd" CCDs, the ø1 and ø2 frequency is equal to one half the pixel rate, a pixels is sampled after both the rising and falling edges of the ø clock. In Even/Odd Mode, the RS pulse position and Sample Reference/Sample Signal edges are set with respect to the either edge of ø1. Standard or Even/Odd mode is selected by setting bit 0 of Register 24. The absolute polarity of the ø pulses is determined by Register 26, bits 0 and 4 (both bits perform the same function). If not needed, one or both ø pulses can be disabled by setting Register 25, bits 0 and 1 to the appropriate value.

1.5 DIGITAL INTERFACE

There are three main sections to the digital interface of the LM9812: the Configuration Register interface (through which all device programming is done), the Correction Coefficient Data interface (the 10 bit-wide input databus for gain and offset correction coefficients), and the 10 bit-wide Pixel Data output databus (where the corrected digital output data appears).

1.5.1 Configuration Register I/O

The Configuration Register is written to and read from through the D0-D9 databus, using the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals. To write to the Configuration Register, follow the timing shown in Diagram 24. The first byte is the address of the Configuration Register to be written to, the second byte is the data to be stored at that address. Configuration Register writes can occur at any time, independent of the state of the SYNC pin.

To read from the Configuration Register, follow the timing shown in Diagram 25. The first byte is the address of the Configuration Register to be written to, the second byte is the data stored at that address. The SYNC pin must be low in order to read from the Configuration Register. To ensure that SYNC is low when in the SYNC out mode, RUN/$\overline{STOP}$ must be low until the end of the active pixels.

If the LM9812's $\overline{RD}$ pin is taken low, *even if the $\overline{CS}$ pin is high*, the D0-D9 databus will be driven. Never take the $\overline{RD}$ pin low unless you are actually doing a Configuration Register read.

1.5.2 Pixel Data I/O

The output of the multiplier is available on the D0-D9 databus. If the Data Read Phase bit (bit 5 of Register 26) is set to a 0, Data changes shortly before the falling edge of $\overline{EOC}$ and remains valid for $t_{DATAVALID}$. If the Data Read Phase bit is set to a 1, Data changes shortly before the rising edge of $\overline{EOC}$ and remains valid for $t_{DATAVALID}$. The D0-D9 databus comes out of tri-state when SYNC is high and $\overline{RD\ PIXEL}$ is low. If SYNC is low, $\overline{RD\ PIXEL}$ will have no effect.

When reading pixel data, $\overline{RD\ PIXEL}$ may be driven by $\overline{EOC}$, putting the data on the bus only when EOC is low, and allowing other data on the bus (such as CD0-CD9 correction data) at other times. In this way the output data and correction coefficient data can share the same databus (See Diagrams 16, 17, 20, and 21).

1.5.3 Correction Coefficient Data I/O

Coefficient data for the pixel rate Offset Subtractor and Shading Multiplier enters the LM9812 through the CD0-CD9 databus. To maximize flexibility for the system designer, there are several clocking options available in this mode: separate or combined buses for the CD0-CD9 and the D0-D9 data, one (GLCK) or two (GLCK and OCLK) clock signals to latch the Correction Coefficient data, and the option to have the LM9812 generate the clock signals or have them supplied to the LM9812. Timing for these different options is shown in Diagrams 14 through 21, and described below.

	CD0-CD9 tied to D0-D9 (1 bus)	CD0-CD9 separate from D0-D9 (2 bus)
GLCK, OCLK are outputs (2 Clock)	Diagram 16	Diagram 14
GLCK is output (1 Clock)	Diagram 17	Diagram 15
GLCK, OCLK are inputs	Diagrams 20, 21	Diagrams 18, 19

Table 3:Correction Databus Options

Diagram 14 shows the case where the correction data (CD0-CD9) is on a separate bus from the output data (D0-D9) (Register 9, bit 4=0). The GLCK and OCLK signals are generated by the LM9812 (Register 9, bit 5=0, bit 7=1). Gain correction data is latched on the rising edge of GCLK, and offset correction data is latched on the rising edge of OCLK. There is a one $\overline{EOC}$ clock latency between the latching of the gain coefficient for a particular pixel and the output of that pixel on the D0-D9 databus.

Diagram 15 shows the case where the correction data (CD0-CD9) is on a separate bus from the output data (D0-D9) (Register 9, bit 4=0). The LM9812 generates the GCLK signal only (Register 9, bit 5=1, bit 7=1). Gain correction data is latched on the rising edge of GCLK, and offset correction data is latched on the falling edge of GCLK. There is a one $\overline{EOC}$ clock latency between the latching of the gain coefficient for a particular pixel and the output of that pixel on the D0-D9 databus.

Diagram 16 shows the case where the correction data (CD0-CD9) is on the same bus as the output data (D0-D9) (Register 9, bit 4=1). The GLCK and OCLK signals are generated by the LM9812 (Register 9, bit 5=0, bit 7=1). Gain correction data is latched on the rising edge of GCLK, and offset correction data is latched on the rising edge of OCLK. Using the $\overline{EOC}$ output to control the $\overline{RD\ PIXEL}$ input allows the CD0-CD9 and the D0-D9 data to exist on the same bus with no contention. There is a one

$\overline{EOC}$ clock latency between the latching of the gain coefficient for a particular pixel and the output of that pixel on the D0-D9 databus.

Diagram 17 shows the case where the correction data (CD0-CD9) is on the same bus as the output data (D0-D9) (Register 9, bit 4=1). The LM9812 generates the GCLK signal only (Register 9, bit 5=1, bit 7=1). Gain correction data is latched on the rising edge of GCLK, and offset correction data is latched on the falling edge of GCLK. Using the $\overline{EOC}$ output to control the $\overline{RD}$ PIXEL input allows the CD0-CD9 and the D0-D9 data to exist on the same bus with no contention. There is a one $\overline{EOC}$ clock latency between the latching of the gain coefficient for a particular pixel and the output of that pixel on the D0-D9 databus.

In the previous modes of operation, the offset correction clock (OCLK) and the gain (shading) correction clock (GCLK) are generated by the LM9812 and used to generate the $\overline{RD}$ pulses to coefficient RAM. These clocks can also be configured as inputs to allow compatibility with some existing ASICs or designs where it is preferred to let the ASIC generate all the timing. The offset data is always latched on the rising edge of OCLK. The gain data is always latched on the rising edge of GCLK.

To operate the LM9812 with an externally supplied OCLK and GCLK, set bit D7 of register 9 to a 0 and set the phase bit for each clock. The procedure to determine the state of the phase bit is described at the end of this section.

DIagrams 18 through 21 show the timing required when GCLK and OCLK are configured as inputs to the LM9812 (Register 9, bit 5=0, bit 7=0). This option exists to allow the LM9812 to work with ASICs designed for earlier systems, where the ASIC generates the SRAM timing (instead of the LM9812). Diagrams 18 and 19 show the 2 bus mode (Register 9, bit 4=0), diagrams 20 and 21 show the 1 bus mode (Register 9, bit 4=1).

In these modes, GLCK and OCLK come from an external source that may be asynchronous to the internally generated OCLK and GCLK. While these clocks may be asynchronous, they will be the same frequency, the ADC conversion rate (since offset and gain coefficients are needed for every pixel, and the pixel data rate is fixed by the ADC conversion rate).

The circuit shown in Figure 3 is implemented inside the LM9812 to synchronize (by delaying) the external coefficient clocks and CD0-9 data with the internal LM9812 clocks.

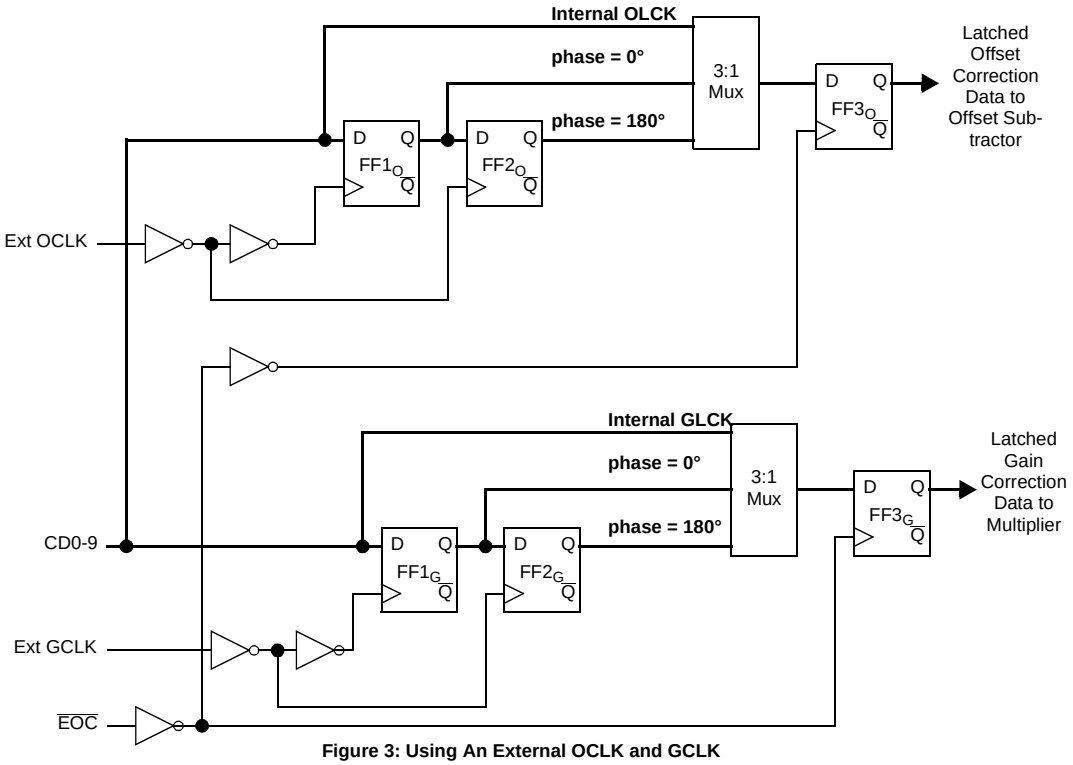


Figure 3: Using An External OCLK and GCLK

CD0-9 data is always latched into register FF1 on the rising edge of the external clock. The output of FF1 is then latched by FF2 on the *falling* edge of the external clock. So the latched data is available at the output of FF1 between the rising edges of the external clock, and is valid at the output of FF2 between the falling edges of the external clock. If the phase difference between the external clock and $\overline{EOC}$ (the LM9812's internal coefficient clock) is known, then by selecting Q1 or Q2 as the input to FF3, the designer can guarantee that the data will be valid on the rising edge of $GCLK_{INT}$, where it is latched into FF3 and synchronized to the LM9812.

$GCLK_{INT}$ is not externally available to the user but it is basically

the inverse of $\overline{EOC}$, plus or minus a few ns of gate delay. To use an external GLCK and OCLK, determine the phase of the external OCLK and GLCK with respect to $\overline{EOC}$. Then look at Diagrams 18 and 19 (2 bus mode) or 20 and 21 (1 bus mode). Choose a phase setting (0° or 180°, register 26 bits 6 and 7) for OCLK and GCLK that provides the most margin with respect to the $t_{OCLK\text{-}\overline{EOC}1\ (OCLK\ IN)}$, $t_{OCLK\text{-}\overline{EOC}2\ (OCLK\ IN)}$, and $t_{GCLK\text{-}\overline{EOC}\ (GCLK\ IN)}$ specifications.

It is entirely possible that either setting (0° or 180°) will work equally well. The condition that must be avoided is when FF3 is clocked (falling edge of EOC) at the same time the input data to FF3 is changing (rising edge of OCLK/GCLK for 0° phase, or falling edge of OCLK/GCLK for 180° phase). As long as this does not occur simultaneously, the data will be correctly latched.

Note that the coefficient data must appear sooner (relative to the pixel output data) for the Clock In modes, to account for the extra latency through FF1 and FF2. This additional time is shown in Diagrams 18 through 21.

This mode of operation may seem confusing at first, but it is necessary to allow the synchronous LM9812 to phase lock to external coefficient data of unknown phase.

1.5.4 MCLK

This is the master clock input for the LM9812. The ADC conversion rate is fixed at 1/4 of this frequency. The pixel rate in 3 channel mode is 1/12 of the MCLK frequency. Many of the timing parameters are also relative to the frequency of this clock.

1.5.5 SYNC

This input signals the beginning of a line. When SYNC goes high, the LM9812 generates a TR pulse, then begins converting pixels until the SYNC line is brought low again. If SYNC is externally applied, the LM9812 will work with sensors with any number of pixels. If SYNC is internally generated (in combination with the RUN/$\overline{STOP}$ input), sensors with up to 3 channels of 16383 pixels/channel can be used.

1.5.6 RUN/$\overline{STOP}$

The LM9812 has a “SYNC OUT” mode (Register 24, bit 4=1) that automatically generates a SYNC pulse stream based on the number of active pixels and the number of additional end-of-line integration pixels programmed into registers 12-15. When the RUN/$\overline{STOP}$ pin is brought high, the LM9812 begins generating the periodic SYNC pulse. When RUN/$\overline{STOP}$ goes low, the LM9812 will continue converting the remaining active pixels, then SYNC will go low and the part will “idle” until the next rising edge of RUN/$\overline{STOP}$.

Using the SYNC OUT mode provides a simple way to clock the sensor continuously with a repeatable, user-programmed integration period. By varying the number of end-of-line integration pixels (in registers 14 and 15), the integration time (and thus the amplitude of the output signal from the sensor) can be adjusted with very high accuracy (about 1 part in 5400, or 0.02%, for a 600dpi sensor).

2.0 PREVIEW MODE OPERATION

The LM9812 supports two “preview” or low resolution modes for CCD sensors (this mode will not work for CIS sensors). In these modes, adjacent pixels are averaged together in the analog domain and converted at the maximum ADC conversion rate. This allows the CCD data to be clocked out and digitized 2 or 4 times faster (corresponding to a 2 to 4 times faster image scan). The image will be 1/2 or 1/4 the resolution. For example, a 600dpi sensor will look like a 300dpi sensor in the x2 preview mode, or a 150dpi sensor in the x4 preview mode. This is useful because it allows faster scans for lower resolution images and scan preview images. The quality of the lower resolution image is also significantly improved because this technique *averages* pixels to reduce the resolution instead of discarding pixels (which often results in a loss of image information).

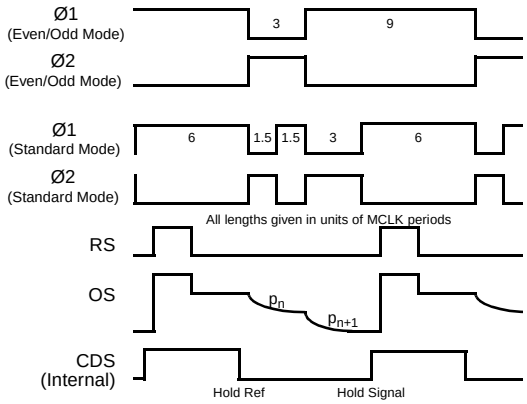


Diagram 4: x2 Preview Mode Timing

In the x2 preview mode, the Ø clock is clocked at 2 times the normal Ø clock frequency, while the RS pulse stays at the ADC’s conversion rate. By skipping every other RS pulse, the charge for pixel n+1 will be added to the charge for pixel n on the CCD itself. Since the CCD is being clocked at 2 times the normal rate, the period between lines (and therefore the integration time) will be half as long, causing the amplitude of each pixel to be half as large. Since the output of the CCD is the sum of two pixels, the final amplitude seen by the LM9812 is very similar to what it is in normal mode. The final pixel amplitude will be equal to $(p_n/2 + p_{n+1}/2) = (p_n + p_{n+1})/2$ = the average of p_n and p_{n+1}.

The same principle applies in the x4 preview mode. Here the Ø clock is clocked at 4 times the normal Ø clock frequency, while the RS pulse stays at the ADC’s conversion rate. By skipping 3 out of 4 RS pulses, the charge for pixels n, n+1, n+2, and n+3 will be averaged in the CCD’s output stage. Since the CCD is being clocked at 4 times the normal rate, the period between lines (and therefore the integration time) will be one quarter as long. The final pixel amplitude will be equal to $(p_n + p_{n+1} + p_{n+2} + p_{n+3})/4$ = the average of p_n, p_{n+1}, p_{n+2}, and p_{n+3}.

Getting the optimum performance out of the preview modes with a particular CCD may require adjusting the RS pulse width, RS pulse position, Sample Reference, and Sample Signal timing (Registers 21, 22, and 23).

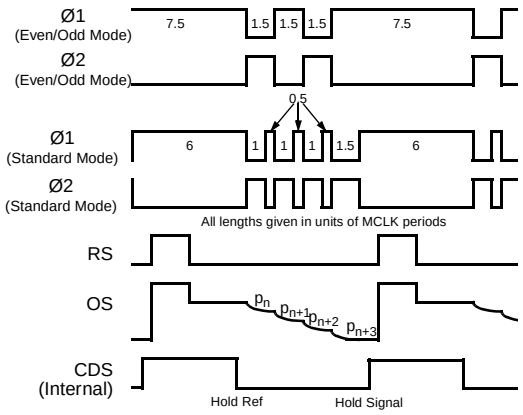


Diagram 5: x4 Preview Mode Timing

3.0 ANALOG INTERFACE

3.1 Voltage Reference

The $V_{REF\ IN}$ pin should be connected to a 2V±5% reference voltage. The LM4041-ADJ adjustable bandgap reference is recommended for this application, as shown in Figure 6. The inexpensive "D" grade meets all the requirements of the application and is available in a TO-92 (LM4041DIZ-ADJ) package as well as a SOT-23 package (LM4041DIM3-ADJ) to minimize board space. To reduce noise, the $V_{REF\ IN}$ pin should be bypassed to

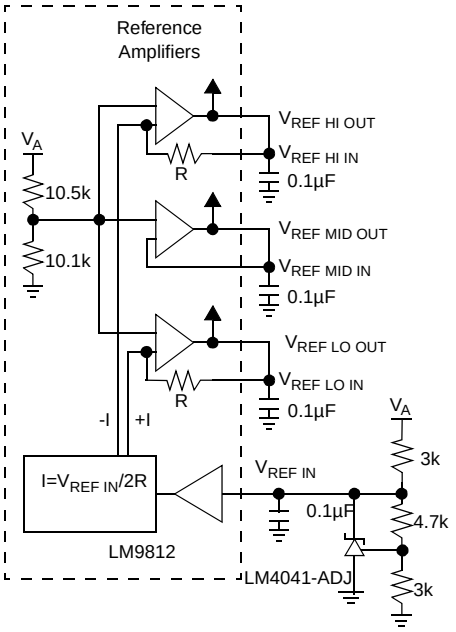


Figure 6: Voltage Reference Generation

AGND with a 0.1µF monolithic capacitor.

The LM9812 generates three internal reference voltages for its analog front end: $V_{REF\ MID}$, $V_{REF\ HI}$, and $V_{REF\ LO}$. $V_{REF\ MID}$ is equal to 0.49*V_A, or 2.45V with a nominal 5V supply. $V_{REF\ IN}$ drives a transconductance amplifier with two output currents, -$V_{REF\ IN}$/2 and +$V_{REF\ IN}$/2. These currents go into the $V_{REF\ HI}$ and $V_{REF\ LO}$ reference voltage buffers, which generate a nominal 3.45V ($V_{REF\ HI}$ = $V_{REF\ MID}$ + $V_{REF\ IN}$/2), and 1.45V ($V_{REF\ LO}$ = $V_{REF\ MID}$ - $V_{REF\ IN}$/2). To minimize noise, the reference amplifiers sense (IN) inputs are brought out to the chip for bypassing. Each buffer's output and input should be tied together and decoupled to AGND through a 0.1µF monolithic capacitor.

3.2 Clamp Capacitor Selection

This section is very long because it is relatively complicated to explain, but the answer is short and simple: A clamp capacitor value of 0.01µF should work in almost all applications. The rest of this section describes exactly how this value is selected.

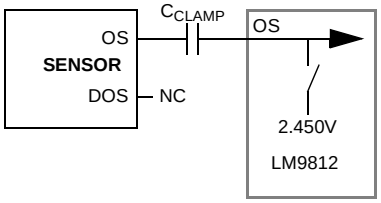


Figure 7: OS Clamp Capacitor and Internal Clamp

The output signal of many sensors rides on a DC offset (greater than 5V for many CCDs) which is incompatible with the LM9812's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output of the sensor is AC coupled to the LM9812 through a DC blocking capacitor, C_{CLAMP} (the CCD's DOS output, if available, is not used). The value of this capacitor is determined by the leakage current of the LM9812's OS input and the output impedance of the sensor. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of $V_{REF\ MID}$, which then determines how many pixels can be processed before the droop causes errors in the conversion (±0.1V is the recommended limit). The output impedance of the sensor determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.

The minimum clamp capacitor value is determined by the maximum droop the LM9812 can tolerate while converting one sensor line. The following equation takes the maximum leakage current into the OS input, the maximum allowable droop (100mV), the number of pixels on the sensor, and the pixel conversion rate (f_{MCLK}/12 for triple output sensors or f_{MCLK}/8 for dual output sensors) and provides the minimum clamp capacitor value:

$$C_{CLAMP\ MIN} = \frac{i}{dV}dt = \frac{\text{leakage current (A)}}{\text{max droop(V)}}\frac{\text{number of pixels}}{\text{conversion rate (Hz)}}$$

Equation 6: $C_{CLAMP\ MIN}$ Calculation

For example, if the OS input leakage current is 20nA worst-case, the sensor has 2700 active pixels, the conversion rate is 2MHz (f_{MCLK} = 24MHz, triple output sensor), and the max droop desired is 0.1V, the minimum clamp capacitor value is:

$$C_{CLAMP\ MIN} = \frac{20nA}{0.1V}\frac{2700}{2MHz} = 270pF$$

Equation 7: $C_{CLAMP\ MIN}$ Example

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the sensor output. The internal clamp is on for each pixel for the time specified in Registers 19 and 20 (see Diagram 11). This time can be calculated using this equation:

$$t_{DARK}(s) = \frac{\text{Start-Stop}}{2\, f_{MCLK}(Hz)}$$

Equation 8: t_{DARK} Calculation

Where Start is the Optical Black Clamp Start Position (Register 19), Stop is the Optical Black Clamp Stop Position (Register 20), f_{MCLK} is the MCLK frequency, and t_{DARK} is the amount of time (per pixel) that the clamp is on.

The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the sensor's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value that allows the clamp capacitor to settle to the desired accuracy within a single line:

$$C_{CLAMP\ MAX} = \frac{t}{R}\frac{1}{\ln(accuracy)} = \frac{n}{R_{OUT}}\frac{t_{DARK}(s)}{\ln(accuracy)}$$

Equation 9: $C_{CLAMP\ MAX}$ Calculation

Where n = the number of optical black pixels, t_{DARK} is the amount of time (per pixel) that the clamp is on, R_{OUT} is the output impedance of the CCD, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. For example, if a sensor has 18 black reference pixels, the output impedance of the sensor is 1500Ω, the LM9812 is configured to clamp for 375ns, the worst case initial voltage across the capacitor is 10V, and the desired voltage after clamping is 0.1V (accuracy = 10/0.1 = 100), then:

$$C_{CLAMP\ MAX} = \frac{18}{1500}\frac{375ns}{\ln(100)} = 977pF$$

Equation 10: $C_{CLAMP\ MAX}$ Example

The final value for C_{CLAMP} should be less than or equal to $C_{CLAMP\ MAX}$, but no less than $C_{CLAMP\ MIN}$. A value of 470pF will work in this example.

In some cases, depending primarily on the choice of sensor, $C_{CLAMP\ MAX}$ may actually be *less* than $C_{CLAMP\ MIN}$, meaning that the capacitor can not be charged to its final voltage during the black pixels at the beginning of a line and hold it's voltage without drooping for the duration of that line. This is usually not a problem because in most applications the sensor is clocked continuously as soon as power is applied. In this case, a larger capacitor can be used (guaranteeing that the $C_{CLAMP\ MIN}$ requirement is met), and the final clamp voltage is forced across the capacitor over multiple lines. This equation calculates how many lines are required before the capacitor settles to the desired accuracy:

$$lines = \left(\frac{R_{OUT}}{n}\frac{C_{CLAMP}}{t_{DARK}}\right)\ln\left(\frac{\text{Initial Voltage}}{\text{Final Voltage}}\right)$$

Equation 11: Line Settling Formula

Using the values shown before and a clamp capacitor value of 0.01µF, this works out to be:

$$lines = \left(\frac{1500}{18}\frac{0.01\mu F}{375ns}\right)\ln\left(\frac{10V}{0.1V}\right) = 10.2\ lines$$

Equation 12: Line Settling Example

At a 2MHz conversion rate, this is about 14ms.

In this example a 0.01µF capacitor takes 14ms after power-up to charge to its final value, but its droop across all subsequent lines is now less than 3mV (using the previous example's values). This wide margin is the reason a C_{CLAMP} value of 0.01µF will work in most applications.

4.0 CALIBRATION

System calibration is required to correct the many sources of error in a scanner and optimize image quality. There are many different ways to calibrate a system, some take a long time but produce better results, others are faster with potentially lower quality images. The method described below should produce very good results, but it is by no means the only way to approach scanner calibration. Some calibration steps could be eliminated to speed up the calibration procedure. Other steps could be improved by iteratively repeating them, verifying that the previous calculation achieved the desired result. Every scanner system is different, so every system may benefit from optimization of the calibration routine.

4.0.1 LM9812 Configuration Sequence After Power-On

The power-on reset circuit of the LM9812 may take several hundred microseconds. Wait 1ms after power-on before writing to the Configuration Registers.

Make sure the SYNC and RUN/$\overline{\text{STOP}}$ inputs are low before writing to the Configuration Registers. When SYNC is high, you can not read the configuration register (but you can still write to it).

The LM9812 configuration sequence:

- Set bit 2 of Test Register 28 to 0 (to allow writing of configuration data). This register is reset to 0 by the power-on reset, but this step is still recommended to ensure that writes will work even if this register was corrupted.
- Program bit 4 of register 24 to determine if the LM9812 will be used in the SYNC OUT or SYNC IN mode.
- Cycle the Powerdown bit to reset the LM9812's state machines. (Take bit 7 of register 25 to a 1, then back to a 0).

This procedure will completely reset the part. At this time the LM9812 is ready for data to be written to all 28 configuration registers. Data can also be read back from all 28 registers if write confirmation is desired.

After all 28 configuration registers have been programmed, scanning can begin by taking SYNC high (in the SYNC IN mode) or RUN/STOP high (in the SYNC OUT mode).

4.1 Calibration Initialization

- Set the Offset DACs to their maximum positive value (Offset DAC registers 0, 1, and 2 =31)
- Set the PGA gains to 1V/V (PGA gain registers 3, 4, and 5 =1)
- Set the Pixel Rate Offset Adder Source to internal (register 9, bit 0=1)
- Set the Pixel Rate Multiplier Source to internal (register 9, bit 1=1)
- Set the Internal Pixel Rate Offset Adder value to 0 (register 6=0)
- Set the Internal Pixel Rate Multiplier value for a gain of 1 (registers 7 and 8 = 0)

- Set the Multiplier Gain Range to 1:3 (register 9, bits 2 and 3 = 00)

4.2 Setting the Static Offset DACs

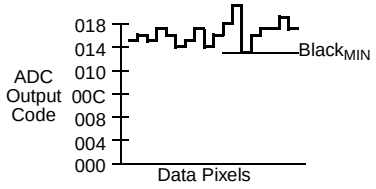


Figure 8: Finding Black$_{MIN}$

- Scan one line of a pure black test pattern, or scan one line with the light source turned off. (Caution: turning the light source on and off may cause thermal drift in light intensity as the light source warms up and cools down.) Scanning multiple black lines and averaging each pixel from each line will reduce noise and increase the accuracy of this step.
- Find the minimum pixel value of the scanned black image (Black$_{MIN}$) for each color (Figure 8).
- Reduce the Offset DAC value for each color so that the minimum black pixel is close to 0, but still greater than 0 (Figure 9). One offset DAC code = ~4.2 ADC LSBs, so change the DAC code to (31 - Black$_{MIN}$/4.2).

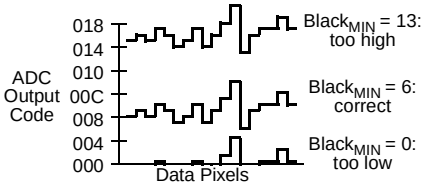


Figure 9: Setting the Static Offset DACs

- Because the above equation is based on typical LM9812 performance, the new DAC settings should be verified. Scan another black line(s) with the new DAC values and verify that all the pixels are still above 0. If any pixels are equal to 0, increment the DAC value by 1. If the minimum pixel is above 8, consider decrementing the DAC value by 1. Repeat this step until the minimum pixel value of the scanned black image (Black$_{MIN}$) for each color is greater than 0 but less than 9. Black$_{MIN}$ values greater than 9 are acceptable (they will be removed by the Pixel Rate Offset Subtractor), but will reduce the dynamic range of the system.

4.3 Setting the Static PGAs

- Decide on the Target Code for your scanner. This is the maximum output code from the ADC for a pure white image. This code may be as large as 1023, but this value could cause clipping if the light source drifts and becomes brighter after calibration. A value of 1000 allows for moderate light source drift between calibration and image scan.
- Scan one line of a pure white test pattern. Scanning multiple white lines and averaging each pixel from each line will reduce noise and increase the accuracy of this step.
- Find the maximum white pixel value of the image data (White$_{MAX}$) for each color (Figure 10).
- Program the PGA value for each color so that the maximum white pixel is close to, but still less than the Target Code (Figure 11). The PGA gain required to meet this condition is equal to the Target Code divided by White$_{MAX}$. Using the PGA

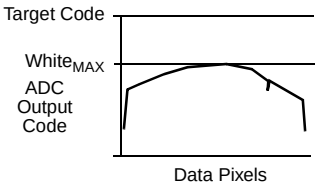


Figure 10: Finding White$_{MAX}$

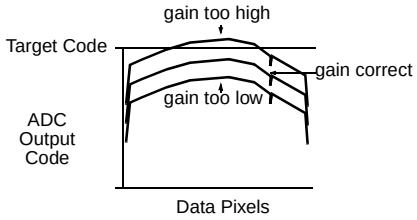


Figure 11: CCD Input Signal In Range

gain equation (Equation 1), the PGA code required is:

$$\text{PGA code} = \text{Integer}\left(\left(\frac{\text{Target Code}}{\text{White}_{MAX}} - 0.94\right)\frac{32}{2.137}\right)$$

Equation 13: PGA Code Calculation

If the Blue channel requires a gain greater than 3 (Target Code/White$_{MAX}$ is >3), then set register 2, bit 7=1 and use Equation 14:

$$\text{PGA code} = \text{Integer}\left(\left(\frac{\text{Target Code}}{\text{White}_{MAX}} - 2.82\right)\frac{32}{6.411}\right)$$

Equation 14: Blue PGA Code Calculation, x3 Bit Set

- Program the calculated PGA values for each color into configuration registers 3, 4, and 5.
- Because the above equations are based on typical LM9812 performance, the new PGA settings should be verified. Scan another white line(s) with the new PGA values and recalculate White$_{MAX}$ and White$_{MIN}$ (the minimum ADC output code for the white image) for each color. Verify that White$_{MAX}$ is near but still below the Target Code. If White$_{MAX}$ is greater than or equal to the target code, decrement that PGA value by 1.
-

4.4 Determining the Multiplier Correction Range Setting

- For best performance, repeat Steps 4.2 and 4.3 before proceeding. This will maximize the available dynamic range of the ADC and ensure that all the pixels are in range.
- Digitize another white line (or multiple lines) and calculate the minimum and maximum pixels from that line (White$_{MIN}$ and White$_{MAX}$). Verify that White$_{MAX}$ is less than the Target Code.

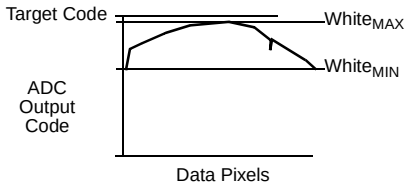


Figure 12: Determining Correction Range Setting

- The correction range required (Range) = White$_{MAX}$/White$_{MIN}$
- If Range < 1.5, then set the Multiplier Range bits (register 9, bits 3 and 2) to 10 (33%).

- If 1.5 < Range < 2.0, then set the Multiplier Range bits (register 9, bits 3 and 2) to 01 (50%).
- If 2.0 < Range < 3.0, then set the Multiplier Range bits (register 9, bits 3 and 2) to 00 (66%).
- If Range > 3.0, then set the range is too large and the system can not be calibrated.

4.5 Calculating the Pixel Rate Offset Coefficients

- Scan one line of a pure black test pattern, or scan one line with the light source turned off. (Caution: turning the light source on and off may cause thermal drift in light intensity as the light source warms up and cools down.) Scanning multiple black lines and averaging each pixel from each line will reduce noise and increase the accuracy of this step.
- The value of each pixel is the offset error for that pixel. Store each pixel value into that pixel's offset correction RAM location.
- Set the Pixel Rate Offset Adder Source to external (register 9, bit 0 = 0)

4.6 Calculating the Pixel Rate Multiplier Coefficients

- Scan one line of a pure white test pattern. Scanning multiple white lines and averaging each pixel from each line will reduce noise and increase the accuracy of this step.
- The equation for the multiplier gain is:

$$\text{Multiplier Gain} = 1 + \frac{x}{N}$$

Equation 15: Multiplier Gain Equation

where:
x is the 10 bit multiplier gain coefficient (0 to 1023),
N = 2048 (Multiplier range = 1:1.5),
N = 1024 (Multiplier range = 1:2),
N = 512 (Multiplier range = 1:3).

- Determine the multiplier gain for each pixel n so the result is the Target Code:

$$\text{Gain(n)} = \frac{\text{Target Code}}{\text{pixel data}_n}$$

Equation 16: Gain Calculation for Each Pixel

- The multiplier coefficient required is therefore:

$$\text{Multiplier Coefficent (n)} = \text{Integer}(N(\text{Gain(n)} - 1))$$
$$= \text{Integer}\left(N\left(\frac{\text{Target Code}}{\text{pixel data}_n} - 1\right)\right)$$

Equation 17: Multiplier Coefficient Calculation for Each Pixel

- Store the Multiplier Gain Coefficients for each pixel into that pixel's offset correction RAM location.
- Set the Pixel Rate Multiplier Source to external (register 9, bit 1=0)

CALIBRATION COMPLETE

4.7 Additional Calibration Information

The procedure detailed in sections 4.1 through 4.6 is only one of many approaches to scanner calibration. In some approaches it may be useful to use a model for the analog front end and actually measure V_{OS1} and V_{OS2}.

Figure 13 is a mathematical model of the analog front end of one channel of the LM9812. The constant C (typically 2, given in the Electrical Characteristics table) represents the total gain error from Vin through D_{OUT} with G = 1V/V (PGA register setting = 1). To further simplify the model, the signal is always assumed to be 0V for black and increasing in the positive direction as pixel brightness increases. In reality, black may be offset from ground, and white may be negative (CCD) or positive (CIS) with respect to black, but this is all taken care of by the CDS function and the correct setting of the Signal Polarity bit (Register 24, bit 7).

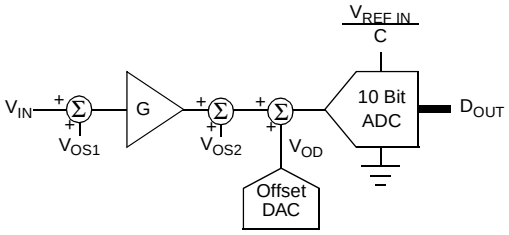


Figure 13: Simplified Model of One Channel of the Analog Front End

The analog front end's transfer function is shown in Equation 18.

$$D_{OUT} = 1024\,C\frac{(V_{IN} + V_{OS1})G + V_{OS2} + V_{OD}}{V_{REFIN}}$$

Equation 18: AFE Transfer Equation

The typical values of C (2) and V_{REFIN} (2V) cancel each other out. It is also useful to convert all the voltages to ADC codes, since that is the domain in which they will be seen by the calibration software. V_{IN} (in ADC codes) = V_{IN} (in V)*1024. Calibration can be more easily accomplished using the simplified model of Equation 19.

$$D_{OUT} = (V_{IN} + V_{OS1})G + V_{OS2} + V_{OD}$$

Equation 19: AFE Transfer Equation (units of ADC LSBs)

Measurement of the two offset voltages (V_{OS1} and V_{OS2}) is done by measuring the ADC output, with a black image on the sensor (if a black reference image is not available, it may be created simply by turning off the scanner's illumination). In this example, V_{IN} is considered to be 0V, and any offsets from the sensor are lumped in with the LM9812's V_{OS1}. If the ADC output is measured with a PGA gain of 1V/V and 3V/V, then the offset errors (V_{OS1} and V_{OS2}) can be determined from the following two equations:

$V_{ADC1} = 1V_{OS1} + V_{OS2} + V_{DAC2}$ *(PGA gain = 1V/V)*
$V_{ADC2} = 3V_{OS1} + V_{OS2} + V_{DAC2}$ *(PGA gain = 3V/V)*

Solving for V_{OS1} and V_{OS2}:

$V_{OS1} = (V_{ADC2} - V_{ADC1})/2$
$V_{OS2} = (3V_{ADC1} - V_{ADC2})/2$

5.0 POWER SUPPLY CONSIDERATIONS

5.1 General

The LM9812 should be powered by a single +5V source (unless 3V-compatible digital I/O is required-see Section *5.2*). The analog supplies (V_A) and the digital supplies (V_D and $V_{DI/O}$) are brought out individually to allow separate bypassing for each supply input. They should *not* be powered by two or more different supplies.

In systems with separate analog and digital +5V supplies, all the supply pins of the LM9812 should be powered by the analog +5V supply. Each supply input should be bypassed to its respective ground with a 0.1µF capacitor located as close as possible to the supply input pin. A single 10µF tantalum capacitor should be placed near the V_A supply pin to provide low frequency bypassing.

To minimize noise, keep the LM9812 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, reference inputs and outputs, V_A, AGND) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

5.2 3V Compatible Digital I/O

If 3V digital I/O operation is desired, the $V_{DI/O}$ pin may be powered by a separate 3V±10% or 3.3V±10% supply. In this case all the digital I/O pins (CD0-CD9, D0-D9, MCLK, SYNC, RUN/$\overline{\text{STOP}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{EOC}}$, GLCK, OCLK, and $\overline{\text{RD PIXELI}}$) will be 3V compatible. The CCD clock signals (Ø1, Ø2, RS, TR1 and TR2) remain 5V outputs, powered by V_D. In this case, the $V_{DI/O}$ input should be bypassed to $DGND_{I/O}$ with a parallel combination of a 0.1µF capacitor and a 10µF tantalum capacitor.

5.3 Power Down Mode

Setting the Power Down bit to a “1” puts the device in a low power standby mode. The CCD outputs (Ø1, Ø2, RS, TR1 and TR2) are pulled low and the analog sections are turned off to conserve power. The digital logic will continue to operate if MCLK continues and SYNC is held high, so for minimum power dissipation MCLK should be stopped when the LM9812 enters the Power Down mode. Recovery from Power Down typically takes 50µs (the time required for the reference voltages to settle to 0.5 LSB accuracy).

6.0 RULES, HINTS, AND COMMON DESIGN PROBLEMS

6.1 Ignore MCLK When Designing a System

While the MCLK input is the master clock for all the LM9812 timing, it should not be used to predict when other clocks or events will occur. To get the highest possible timing resolution, the LM9812 uses double-edged flip flops for many functions. CCD clock output signals, coefficient clocks, and internal clocks may change state on the rising or falling edge of MCLK, depending on the state of MCLK and some internal free running state machines when the RUN/$\overline{\text{STOP}}$ or SYNC input goes high. Normal process variations from part to part result in different delays between an MCLK edge and other events in the LM9812.

For a reliable design, synchronize your system to $\overline{\text{EOC}}$, GCLK, and OCLK. These signals are repeatable from device to device. Do not synchronize your system to MCLK: treat it only as a frequency that sets the pixel rate of the system. If you need to generate additional CCD timing signals, synchronize them to the LM9812’s TR and RS outputs.

6.2 Weak Latches On Databus

The D0-D9 databus has weak latches on its output pins to keep the databus from drifting through the input’s trip point when TRI-STATED. If the voltage on the input pin is at the threshold, large amounts of current can be drawn from the digital I/O supply because the N and the P channel of the input buffer are simultaneously on. These latches are very weak (sourcing and sinking about 50µA typically) and can be easily overdriven.

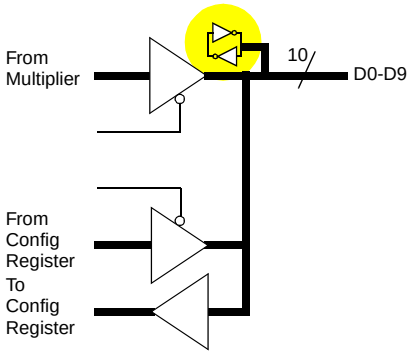


Figure 14: Weak Latches On Databus

6.3 Don’t Decrement the Reference Sample Position Register by 1

A write to the Reference Sample Position Register (Configuration Register 22) containing a value that is 1 less than the current value stored in the Reference Sample Position Register will sometimes make one of the LM9812’s internal state machines to fail, causing erratic and improper operation of the LM9812. For example, if the value currently stored in the Reference Sample Position Register is 12, then writing an 11 can cause this problem.

To avoid this condition, never decrement the existing value stored in the Reference Sample Position Register by 1. Incrementing by any amount or decrementing by 2 or greater or writing the same number over again will not cause any problems.

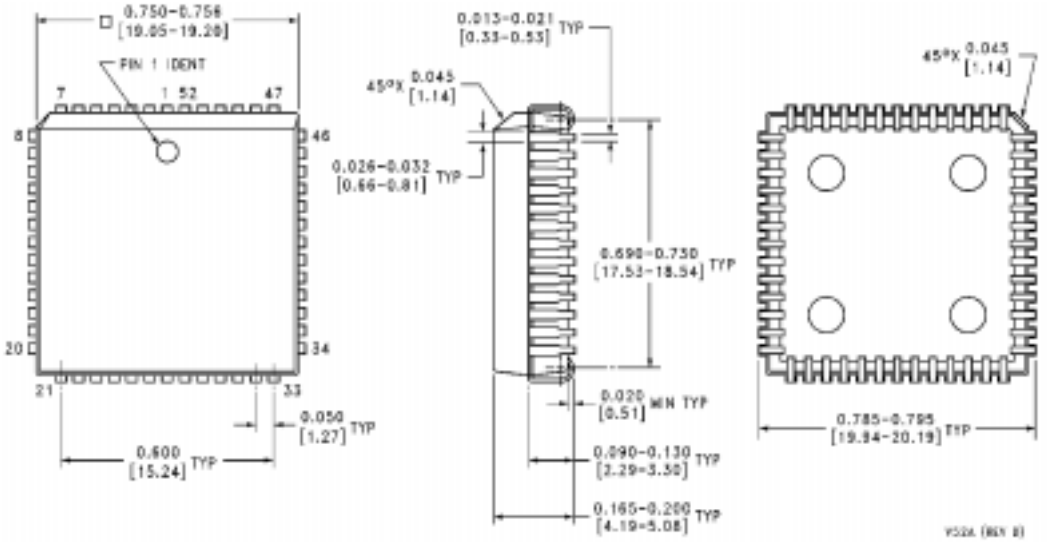
To get out of this mode, write a new number to the Reference Sample Position Register that is greater than the original number.

Since incrementing and decrementing this register should only be done during the development phase of the system until an ideal value for this register is chosen. This issue should cause absolutely no problems in production, since the value of this register will be fixed, so the firmware should never write more than the final ideal value to this register.

6.4 Taking $\overline{\text{RD}}$ Low With $\overline{\text{CS}}$ High Will Drive the Databus

In many digital systems, the $\overline{\text{RD}}$ signal is ignored when $\overline{\text{CS}}$ is held high. This is not the case with the The LM9812. Taking $\overline{\text{RD}}$ low with $\overline{\text{CS}}$ high will take the D0-D9 databus out of tristate and put random data on the databus. Do not assume that $\overline{\text{RD}}$ is ignored when $\overline{\text{CS}}$ is high.

Physical Dimensions inches (millimeters)



52-Pin Plastic Leaded Chip Carrier (PLCC)
Order Number LM9812CCV
NS Package Number V52A

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