National Semiconductor

October 2000

LM98503
10-Bit, 18 MSPS Camera Signal Processor

General Description

The LM98503 is a CCD signal processor for digital cameras. The processor provides a common interface to a number of different image sensors including CCD, CMOS, and CIS. Correlated double sampling reduces kTC noise from the image signal. A fast, temperature stable, 8-bit digitally programmable gain amplifier enables pixel-rate white-balancing. An auxiliary input is provided, allowing for the selection of an external signal, useful for sampling analog video signals. The 10-bit A/D converter preserves the image quality with excellent noise performance. The LM98503 also includes the supporting functions of digital black level clamp and power down, ideally suited for portable video applications. This low-power processor is a natural choice for the most demanding imaging systems.

Applications

- Digital still cameras
- Digital video camcorders
- Video conferencing
- Security cameras
- Plain paper copiers
- Flatbed or handheld color scanners
- Video processing for X-ray or infrared
- Barcode scanners

Features

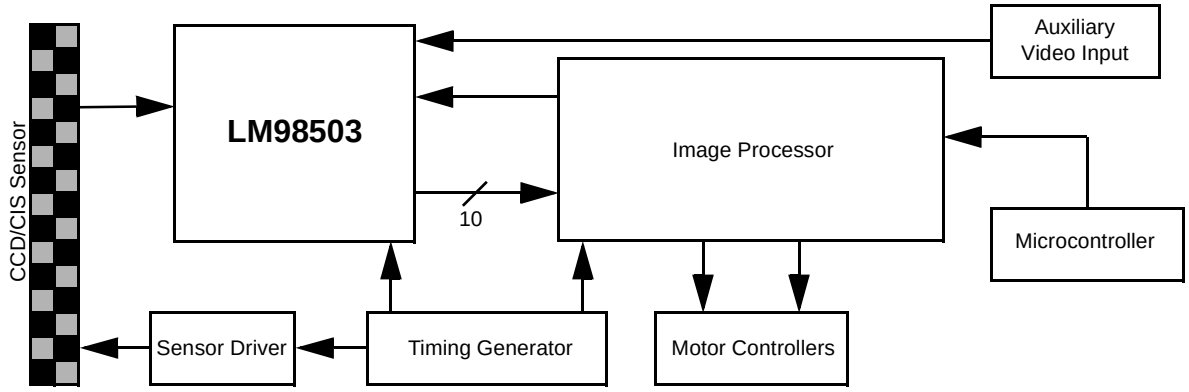
- +3 Volt single power supply
- Low power CMOS design
- 4-Wire serial interface
- 2.5V data output voltage swing
- AUX input with analog clamp and programmable gain
- Four color gain and offset registers
- Digital black level clamp
- Small 48-lead LQFP package
- Supports interlace and progressive scan CCDs.

Key Specifications

■Maximum Input Level	1.0 Volt peak-peak
■CDS Sampling Rate	18 MSPS
■PGA Gain Steps	256 Steps
■PGA Gain Range	0.0 - 32.0 dB
■ADC Resolution	10-Bit
■ADC Sampling Rate	18 MSPS
■*Signal-to-Noise Ratio	68dB @ 0dB Gain, 1.0V Input
■Power Dissipation *AV+ = DV+ = 2.7V*	86 mW (typical)
■Operating Temp	0^oC to 70^oC

* Note: $20 \log_{10} (V_{IN} / \text{RMS Output Noise})$

Typical Digital Camera Block Diagram



Block Diagram

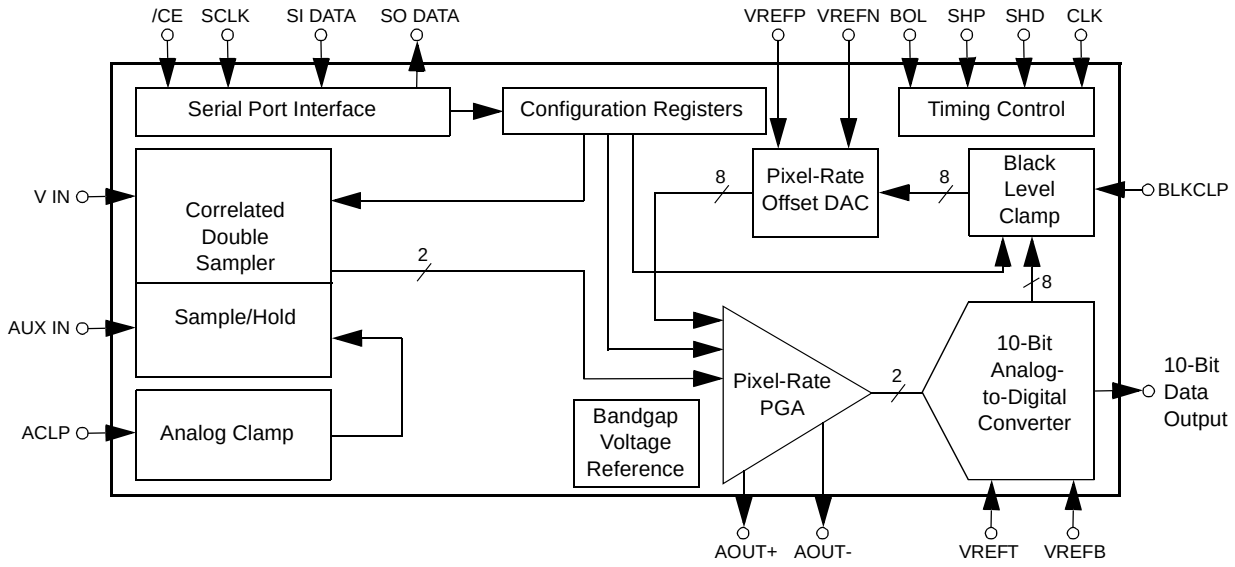


Figure 1: Chip Block Diagram

Pin Out

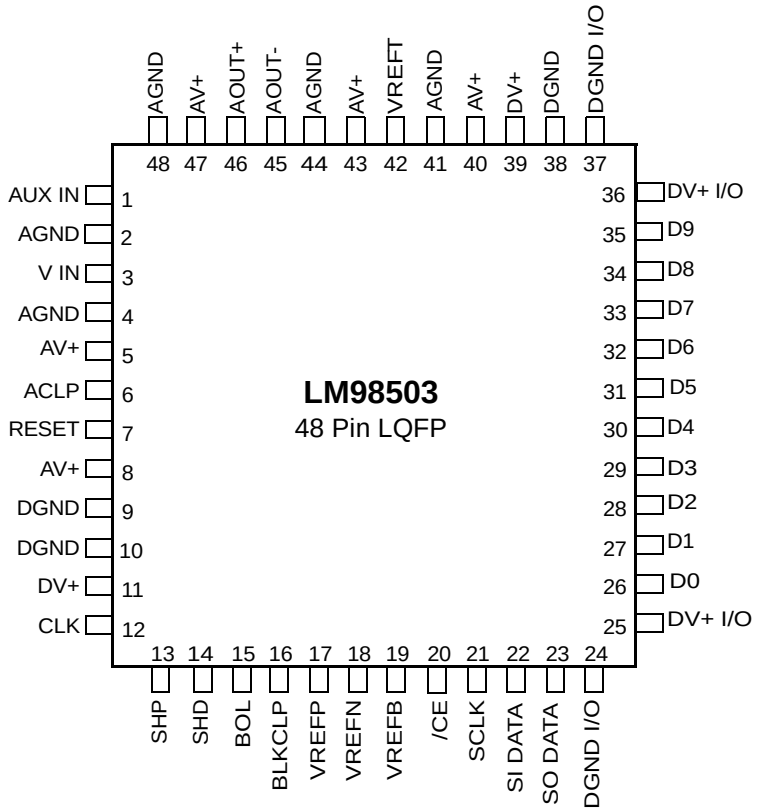


Figure 2: Pin Out Diagram

Ordering Information

Commercial ($0°C \leq T_A \leq 70°C$)	NS Package
LM98503CCVV	LQFP

Typical Application Circuit

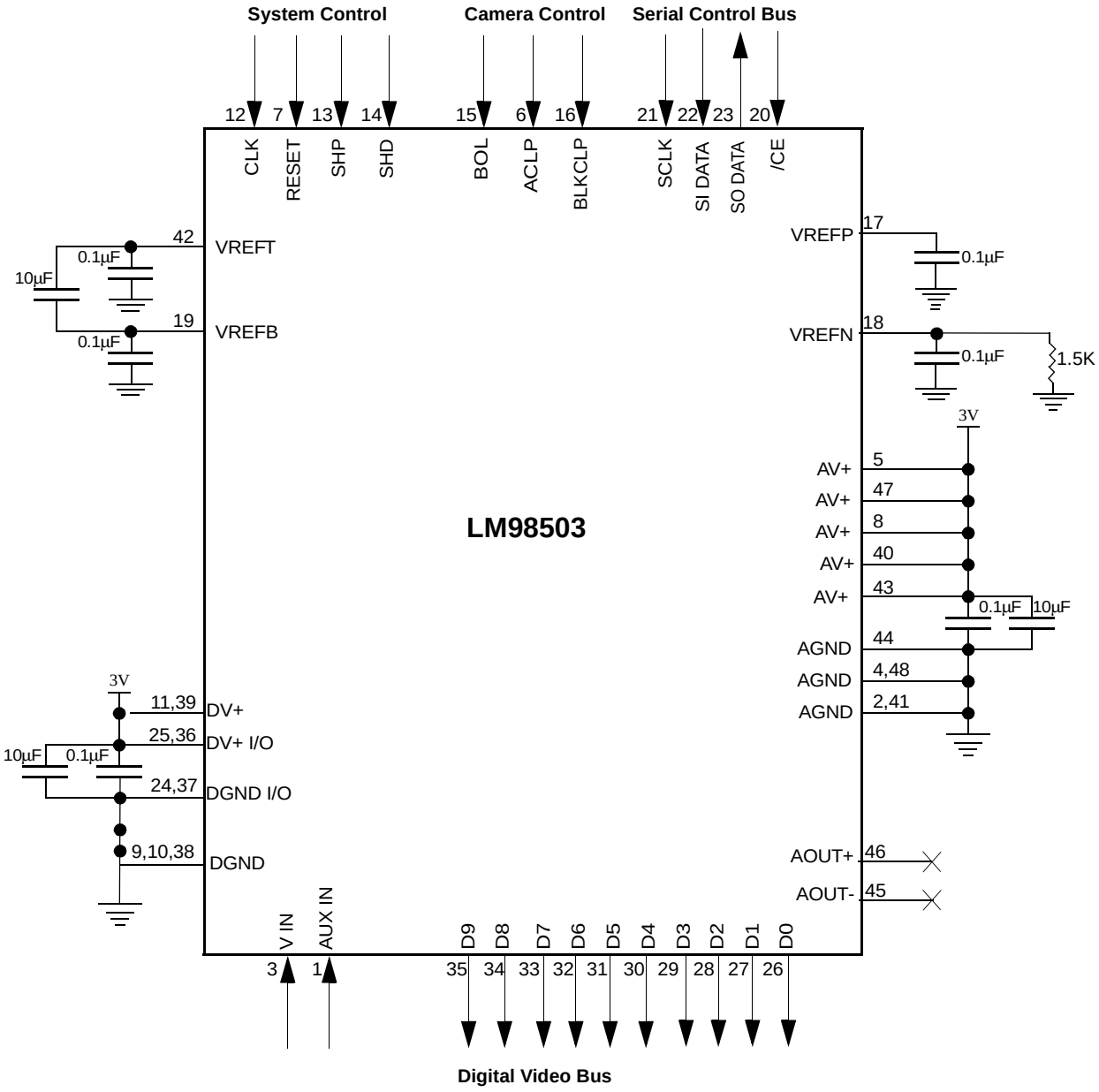


Figure 3: Typical Application Circuit Diagram

Pin Descriptions

Pin	Name	I/O	Typ	Description
1	AUX IN	I	A	Auxiliary analog input.
2	AGND		P	Analog ground return.
3	V IN	I	A	Analog input. AC-couple input signal through a 0.1µF capacitor.
4	AGND		P	Analog ground return.
5	AV+		P	+3 Volt power supply for the analog circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
6	ACLP	I	D	Analog clamp switch.
7	RESET	I	D	Active-high master reset. Float pin when function not being used.
8	AV+		P	+3 Volt power supply for the analog circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
9	DGND		P	Digital ground return.
10	DGND		P	Digital ground return.
11	DV+		P	+3 Volt power supply for the digital circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
12	CLK	I	D	18 MHz clock input.
13	SHP	I	D	Correlated double sampler reset voltage clamp override. Programmable active-high or active-low through serial interface. Connect to +3 Volt digital supply when function not being used (register values in default condition).
14	SHD	I	D	Correlated double sampler video signal voltage sample override. Programmable active-high or active-low through serial interface. Connect to +3 Volt digital supply when function not being used (register values in default condition).
15	BOL	I	D	Active-high beginning of line switch input. Hold high during entire line of effective pixels. Hold low during blanking period.
16	BLKCLP	I	D	Active-high black level clamp switch input. Pulse high during black pixels to set black pixel level to the value stored in Output Black Level register. (See page 15.)
17	VREFP	IO	A	Top of DAC reference ladder. Normally bypassed with a 0.1µF capacitor. An external DAC reference voltage may be applied to this pin.
18	VREFN	IO	A	Bottom of DAC reference ladder. Normally bypassed with a 0.1µF capacitor. An external DAC reference voltage may be applied to this pin. Alternately, an external pull-down resistor may be used to extend the DAC range. (See section 3.0).
19	VREFB	IO	A	Bottom of ADC reference ladder. Normally bypassed with a 0.1µF capacitor and 10µF capacitors in parallel. An external ADC reference voltage may be applied to this pin.
20	/CE	I	D	Active-low chip enable for the serial interface.
21	SCLK	I	D	Serial interface clock used to decode the serial input data.
22	SI DATA	I	D	Serial interface input port.
23	SO DATA	O	D	Serial interface output port.
24	DGND I/O		P	Digital output driver ground return.
25	DV+ I/O		P	+3 Volt power supply for the digital output driver circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
26	D0	O	D	Digital output. Bit 0 of 9 (LSB) of the digital video output bus.
27	D1	O	D	Digital output. Bit 1 of 9 of the digital video output bus.
28	D2	O	D	Digital output. Bit 2 of 9 of the digital video output bus.
29	D3	O	D	Digital output. Bit 3 of 9 of the digital video output bus.
30	D4	O	D	Digital output. Bit 4 of 9 of the digital video output bus.
31	D5	O	D	Digital output. Bit 5 of 9 of the digital video output bus.
32	D6	O	D	Digital output. Bit 6 of 9 of the digital video output bus.

Pin Descriptions (continued)

Pin	Name	I/O	Typ	Description
30	D4	O	D	Digital output. Bit 4 of 9 of the digital video output bus.
31	D5	O	D	Digital output. Bit 5 of 9 of the digital video output bus.
32	D6	O	D	Digital output. Bit 6 of 9 of the digital video output bus.
33	D7	O	D	Digital output. Bit 7 of 9 of the digital video output bus.
34	D8	O	D	Digital output. Bit 8 of 9 of the digital video output bus.
35	D9	O	D	Digital output. Bit 9 of 9 (MSB) of the digital video output bus.
36	DV+ I/O		P	+3 Volt power supply for the digital output driver circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
37	DGND I/O		P	Digital output driver ground return.
38	DGND		P	Digital ground return.
39	DV+		P	+3 Volt power supply for the digital circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
40	AV+		P	+3 Volt power supply for the analog circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
41	AGND		P	Analog ground return.
42	VREFT	IO	A	Top of ADC reference ladder. Normally bypassed with a 0.1µF capacitor and 10µF capacitors in parallel. An external ADC reference voltage may be applied to this pin.
43	AV+		P	+3 Volt power supply for the analog circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
44	AGND		P	Analog ground return.
45	AOUT-	O	A	Negative differential analog output from correlated double sampler or PGA (selectable through the serial interface).
46	AOUT+	O	A	Positive differential analog output from correlated double sampler or PGA (selectable through the serial interface).
47	AV+		P	+3 Volt power supply for the analog circuits. Bypass each supply pin with 0.1µF and 10µF capacitors in parallel.
48	AGND		P	Analog ground return.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog)

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	4.2V
Voltage On Any Input or Output Pin	-0.3V to 4.2V
Input Current at any pin (Note 3)	±35mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C (Note 4)	
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature	
Infrared, 10 seconds (Note 6)	260°C
Storage Temperature	-65°C to 150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	-0°C≤T_A≤+70°C
All Supply Voltages	+2.85V to +3.15V
V IN Voltage Range	0.0V to AV+
V_{REFT} Voltage Range	2.0V to 2.5V
V_{REFB} Voltage Range	0.4V to 0.9V
V_{REFP} Voltage Range	1.3V to 1.9V
V_{REFN} Voltage Range	1.3V to 1.9V
All Digital Inputs Voltage Range	-0.05V to 3.35V

DC and Logic Level Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7).

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
Digital Input Characteristics						
VIH	Logical “1” Input Voltage		**2.0**			V
VIL	Logical “0” Input Voltage				**1.0**	V
IIH	Logical “1” Input Current	VIH = DV+, Digital inputs except Reset		100		nA
		VIH = DV+, Reset (internal pull-down resistor)		400		µA
IIL	Logical “0” Input Current	VIL = DGND		-100		nA
Digital Output Characteristics						
VOH	Logical “1” Output Voltage	DV+ = 3.15V, Iout = -0.5mA DV+ = 2.85V, Iout = -0.5mA	**2.5** **2.3**			V
VOL	Logical “0” Output Voltage	DV+ = 3.15V, Iout = 1.6mA DV+ = 2.85V, Iout = 1.6mA			**0.4** **0.4**	V
IOS	Output Short Circuit Current			30		mA
Power Supply Characteristics						

Power Dissipation Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
PWR	Average Power Dissipation	AV+ = DV+ = DV+ I/O = 2.7V AV+ = DV+ = DV+ I/O = 3.0V AV+ = DV+ = DV+ I/O = 3.3		86 100 116		mW

Correlated Double Sampler Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
V_{IN}	Input Voltage Level			1.0		V_{p-p}
I_{IN}	Input Leakage Current			5		nA
C_{IN}	Input Capacitance			5		pF
R_{IN}	Input Resistance			10		kΩ
t_{AD}	Aperture Delay			2		ns
t_{SHP}	CLK falling edge to SHP falling edge			10		
t_{SHD}	CLK rising edge to SHD falling edge			14		

PGA Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
	Gain Resolution			8		Bits
	Step Size	(Gain / Resolution)		0.125		dB
	Maximum Gain			32.0		dB
	Minimum Gain			0.0		dB
	Gain Error @ 20MHz	Deviation from best-fit line after end-point correction		±5		%

Offset DAC and Black Level Clamp Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
R_{REF}	Reference Ladder Resistance			50		kΩ
	Resolution			±7		Bits
	Offset Adjustment Range	PGA Gain = 1.0		±54		mV
	Black Level Clamp Accuracy	PGA Gain = 0.0dB PGA Gain = 32.0dB		±.5 ±.5		LSB LSB
t_{BLKCLP}	Black Clamp Switch Pulse Width		20			T_{CLK}

Analog to Digital Converter Specifications

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18 MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
R_{REF}	Reference Ladder Resistance			1000		kΩ
V_{REFT}	Top of Reference Ladder	V_{REFT} not driven externally.		2.25		V
V_{REFB}	Bottom of Reference Ladder	V_{REFB} not driven externally.		0.75		V
V_{REFT} - V_{REFB}	Differential Reference Voltage	V_{REFT} and V_{REFB} not driven externally.		1.5		V
	Overrange Output Code	$V_{IN} > V_{REFT}$		1023		
	Underrange Output Code	$V_{IN} < V_{REFB}$		0		

AC Electrical Characteristics

The following specifications apply for DV+ = AV+ = DV+ I/O = +3.0V, C_L = 10pF, and f_{CLK} = 18 MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
f_{CLK}	Input Clock Frequency		1	18	20	MHz
T_{CLK}	Input Clock Period		50	55	1000	ns
t_{ch}	Clock High Time	@ CLK_{max}	27.5			ns
t_{cl}	Clock Low Time	@ CLK_{max}	22.5			ns
	Clock Duty Cycle	@ CLK_{max}		45/55		min/max
t_{rc}, t_{fc}	Clock Input Rise and Fall Time			5		ns
	Pipeline Delay (Latency)			7		T_{CLK}
t_{VALID}	Data valid time			40		ns
t_{OH}	Output Data Hold Time			27	**33**	ns
t_{OD}	Output Delay Time			20		ns

Full Channel Performance Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
DNL	Differential Non-Linearity			±0.5		LSB
INL	Integral Non-Linearity			+3.0/-1.5		LSB

* Note: 20 $\log_{10}$ (V_{IN} / RMS Output Noise)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Note 3: When the voltage at any pin exceeds the power supplies (VIN < GND or VIN > AV+ or DV+), the current at that pin should be limited to 35mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.

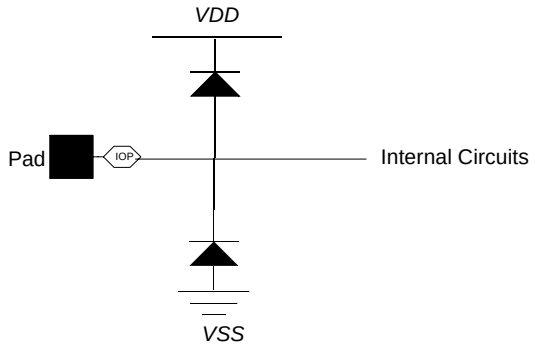
Full Channel Performance Specifications (continued)

Note 4: The absolute maximum junction temperature (TJmax) for this device is 150^{o}C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (*JA), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJmax - TA)/*JA. In the 48-pin LQFP, *JA is 69oC/W, so PDMAX = 1,811mW at 25oC and 1,159 mW at the maximum operating ambient temperature of 70oC. Note that the power dissipation of this device under normal operation will typically be about TBDmW. The values for maximum power dissipation listed above will be reached only when the LM98503 is operated in a severe fault condition.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above AV+ and below AGND.



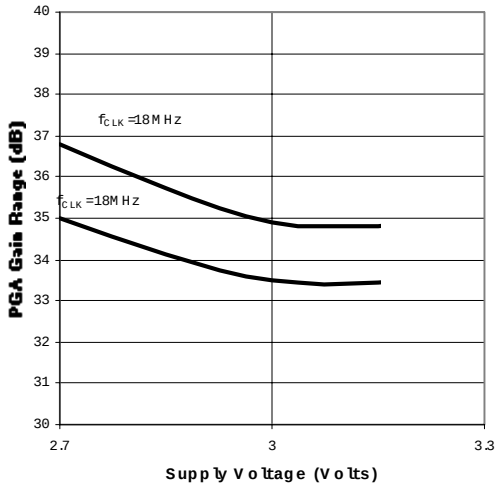
Note 8: Typical figures are at TJ = 25^{o}C, and represent most likely parametric norms

Note 9: Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

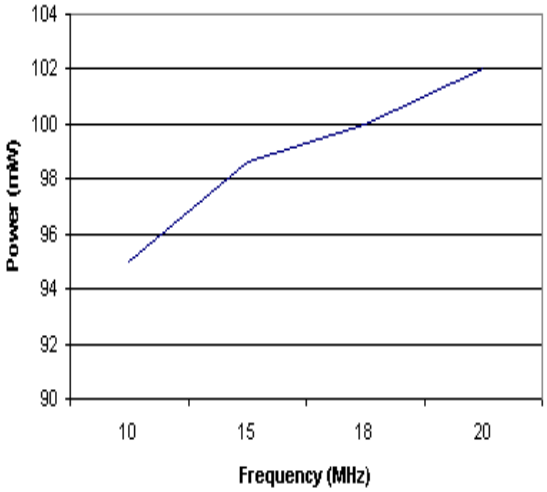
Typical Performance Characteristics

(Default conditions are f_S = 27MHz, T_A = 3.0V, and AV+ = DV+ = DV+ I/O = 3.0V, unless otherwise noted.)

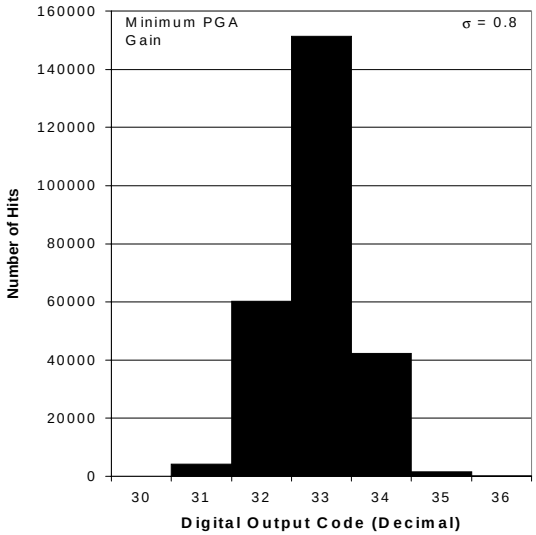
Gain variation part to part



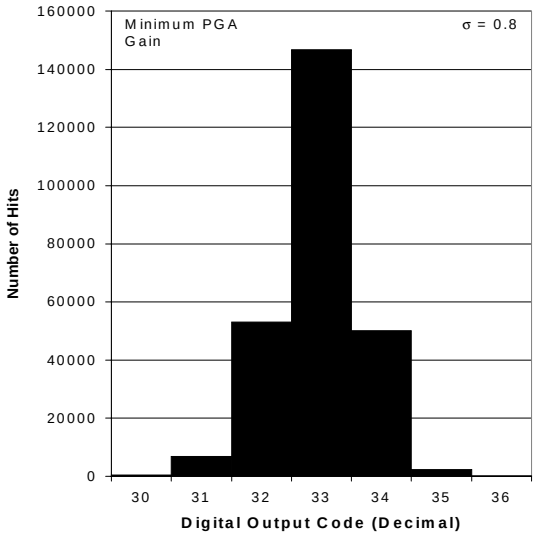
Power Dissipation vs. Clock Frequency



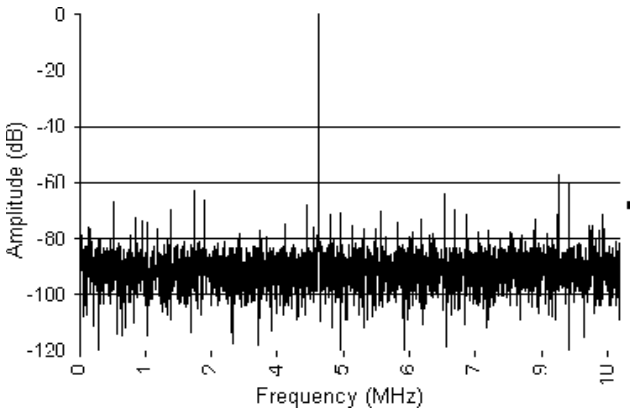
Grounded Input Noise @ 14MHz Clock Frequency



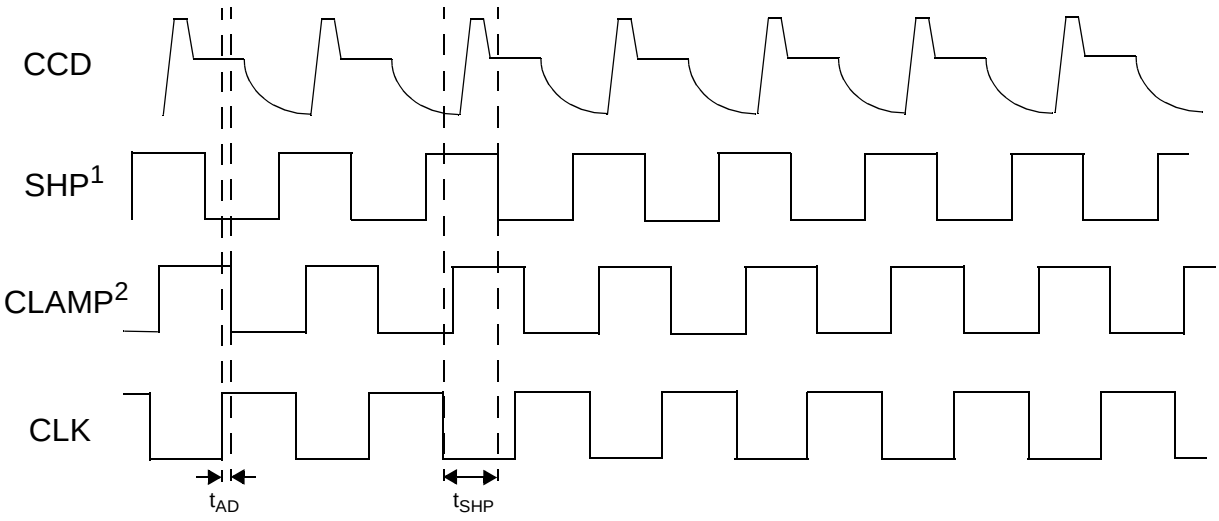
Grounded Input Noise @ 18MHz Clock Frequency



Spectral Response @ 20MHz Clock, Fin= 4.4MHz

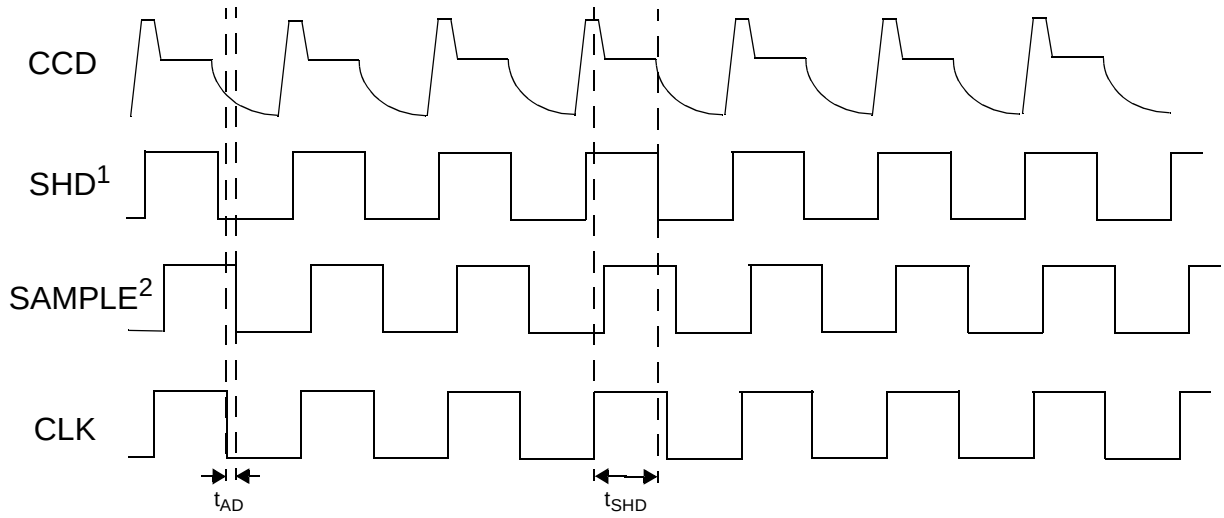


CDS Sampling Timing



[1]SHP overrides the CLAMP signal's falling edge for sampling the reset voltage (SHP is active-low by default).
[2]The CLAMP signal is an internal signal derived from the CLK input whose falling edge samples the CCD reset voltage by default.

Figure 4: Pixel Rate Reset Voltage Sampling



[1]SHD overrides the SAMPLE signal's falling edge for sampling the video signal (SHD is active-low by default).
[2]The SAMPLE signal is an internal signal derived from the CLK input whose falling edge samples the CCD video signal by default.

Figure 5: Pixel Rate Video Signal Sampling

Horizontal Interval Timing

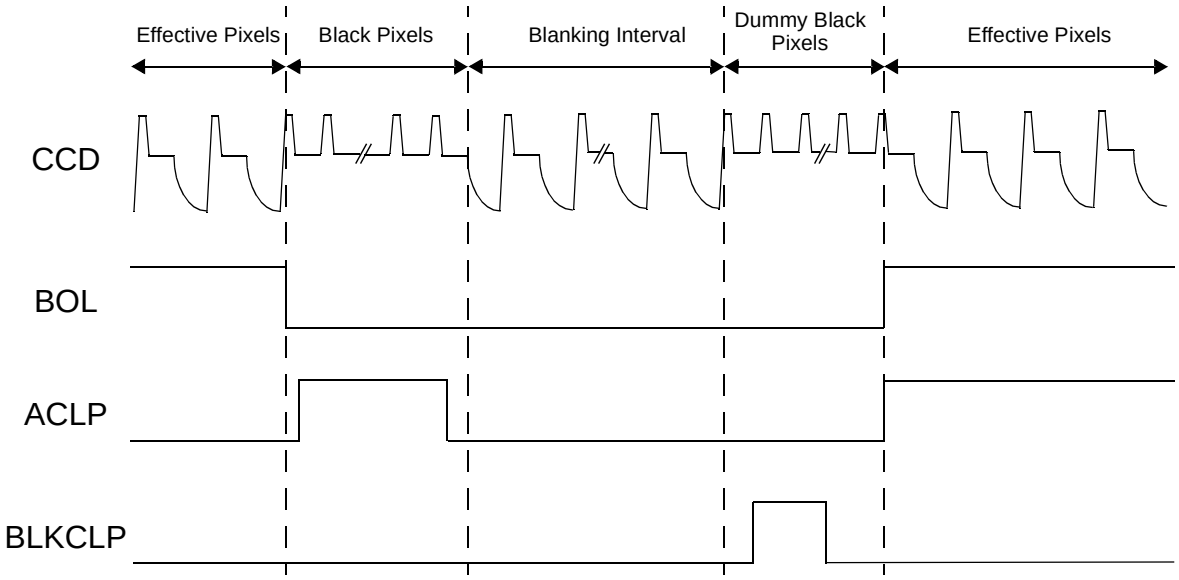


Figure 6: Typical Horizontal Interval Timing

Digital Output Timing

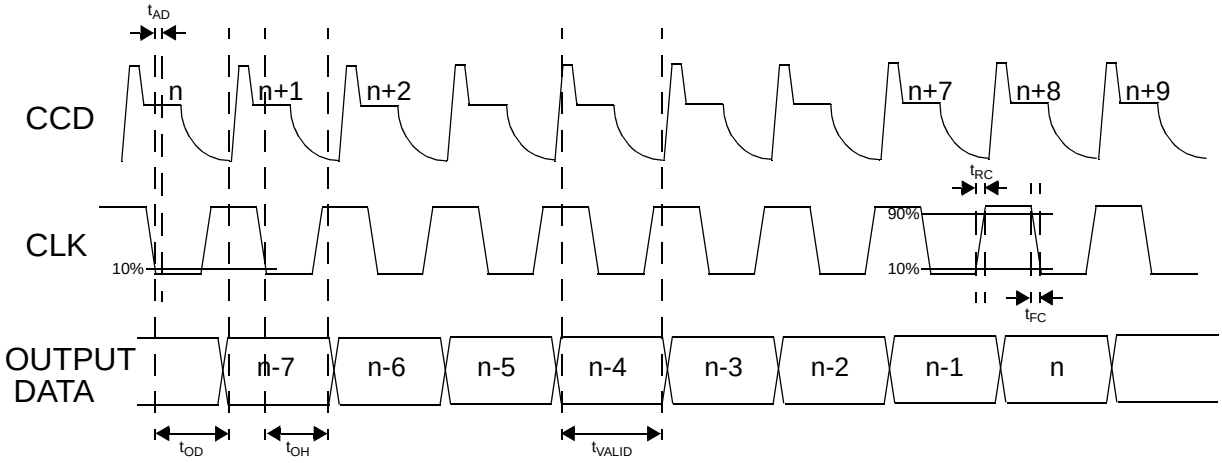


Figure 7: Digital Output Data Timing

System Timing

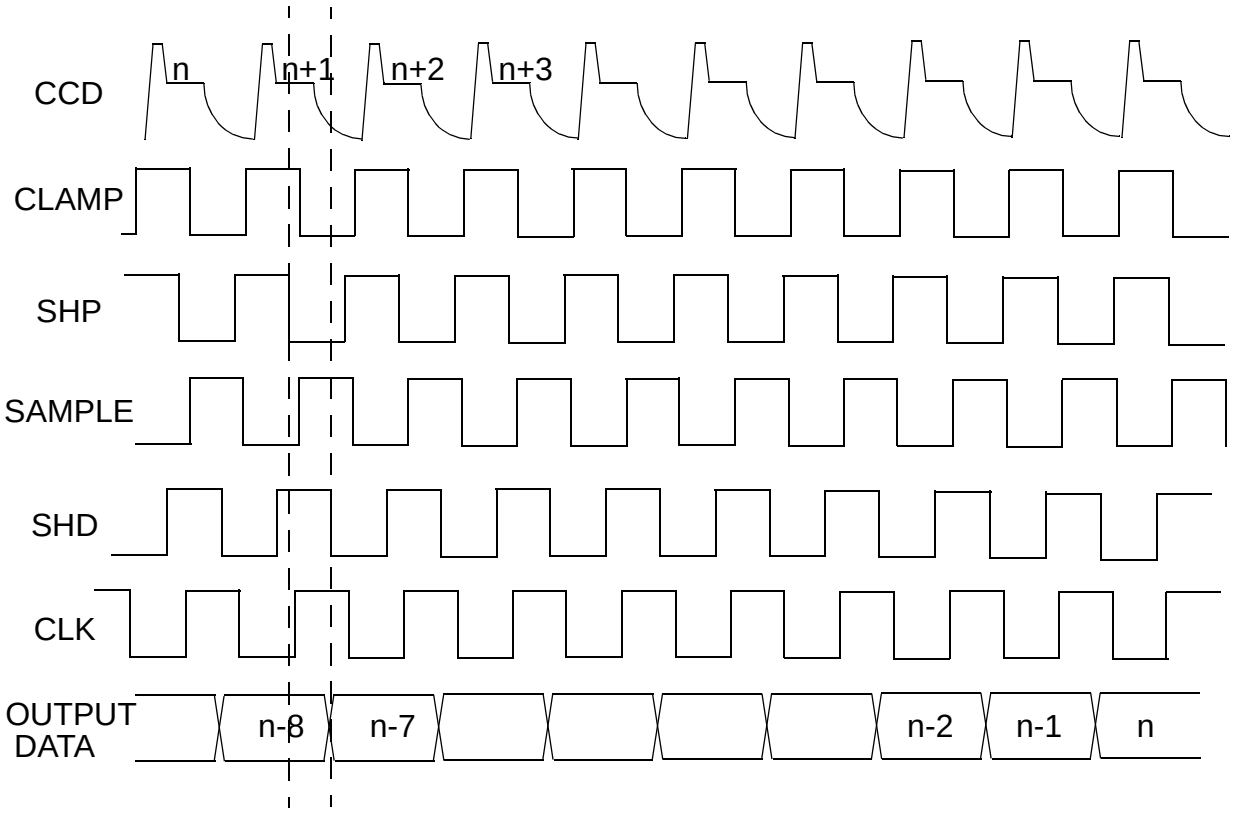


Figure 8: System Timing

System Overview

1.0 Introduction

The LM98503 is a 10-bit, complete analog-to-digital camera signal processor for use with CCD imager systems operating from a single +3 Volt supply. The internal processing is carefully optimized to maintain the signal-to-noise ratio and excellent dynamic performance of most popular CCD imagers. The system block diagram of the LM98503, shown on the cover page of the datasheet, highlights the main features of the device: correlated double sampling (CDS), 0-32dB digitally programmable gain amplifier (PGA), digital black level correction feedback loop, 8-bit DAC, analog clamp, bandgap voltage reference, and a 10-bit, 18MHz analog-to-digital converter.

1.1 Correlated Double Sampling

Correlated double sampling (CDS) is a key feature in CCD image processors. The sampling process consists of two samples being taken for each pixel. The first stores the reset voltage of the input pixel, and the second sample stores the video signal amplitude. The two samples are subtracted from one another, effectively removing the reset error offset of each pixel. This sampling system operates from 1 to 18MHz. .

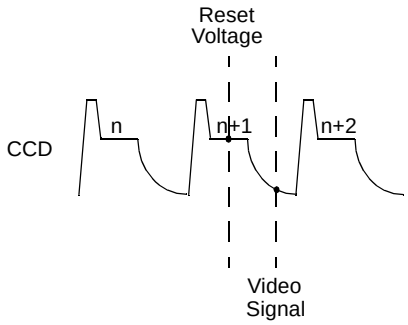


Figure 9: Correlated Double Sampling

1.2 Programmable Gain Amplifier

The amplifier has a gain ranging from 0-32dB, and is “linear in dB” as shown in Figure 15. The PGA is addressed via an 8 bit word downloaded through the serial interface.

1.3 Black Level Clamp

CCD signal processors require a reference level for the proper handling of input signals; this reference level is commonly referred to as the black level. The LM98503 is designed to determine a signal’s black level during the CCD imager’s optical black pixels.

The LM98503 provides both an analog clamp and a digital black level correction loop. Pulsing the ACLP pin during optical black pixels causes the analog clamp circuitry to remove the offset associated with the input signal. Pulsing the BLKCLP pin during dummy black pixels at the begining of a horizontal line enables the digital black level correction loop.

Black level correction may be performed through one of two available methods- automatic or manual. In automatic mode, the black level is sampled from the ADC output during black pixels by setting the BLKCLP input of the LM98503. The ADC black level output value is then averaged over eight pixels and subtracted from the desired black level code stored in the black level configuration register. The result of the subtraction may then be integrated by a preset scaling factor, effectively smoothing any sharp transitions present in the black level signal, before the resulting error is finally applied to the input of the PGA as an analog offset generated by the DAC. The offset integration scaling factor is stored in two bits of the software control register 0, and the values available range from full offset to offset divided-by-16. In addition, an offset output enable bit is provided in the software control register 0, which when set, routes the offset value to the digital output bus rather than the DAC. Use of the automatic mode involves enabling the black level offset auto-calibration bit in the software control register 0 through the serial interface. Refer to Figure 10.

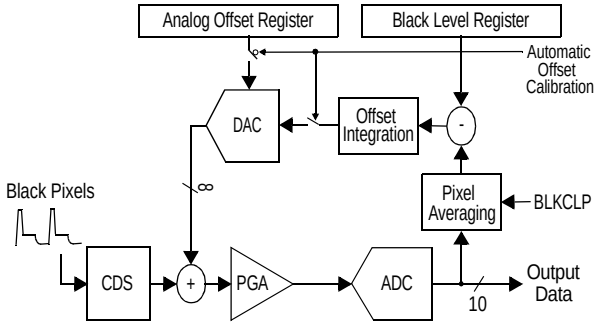


Figure 10: Digital Black Level Correction Loop

The manual method is intended for use with processing systems where the desired black level correction loop is external to the LM98503. In this mode, up to four available configuration registers may be used to store predetermined offset values that will be applied on a pixel-rate basis. During the vertical interval, new values may be stored in these registers for each horizontal line.

1.4 Auxiliary Input

The LM98503 includes a high-level video switch that allows a an auxiliary video signal to be selected instead of the camera image. When the auxiliary input is selected, the PGA gain and DAC offset are fixed to the value in register 0, so the appropriate gain and offset values should be written to PGA gain and DAC offset register 0 prior to AUX IN usage.

1.5 Analog Clamp

During optical black pixels, a signal appears at the CCD output. This signal is generally refered to as the “black signal level”. This signal may be seen by the CDS circuitry as a valid video signal rather than the actual black level signal; therefore, the LM98503 provides an analog clamp designed to eliminate this black signal level. Pulsing the analog input pin, ACLP, causes the output of the CDS to be sampled by the analog clamp circuitry. Subsequently, an adjustment is made to the CDS reference voltages by the analog clamp to effectively eliminate any signal level present during black pixels.

10-Bit Analog-to-Digital Converter

The selected imager’s analog signal is sampled by the CDS and amplified to match the input requirements of the 10-bit analog to digital converter by the PGA. The final step performed by the system is to convert the selected analog image to digital values with a 10 bits of resolution. The ADC has differential inputs which aids in the coping with headroom constraints common to +3 Volt systems. Data is acquired at the falling edge of the clock and is available at the digital output pins 7.0 clock cycles plus t_{OD} later.Internal Timing Generation

All if the necessary clocks for the CDS and ADC operation are generated internally from the LM98503’s master clock input. The CDS sampling clocks may be overridden by the user via the SHP and SHD clock inputs. As depicted in Figure 4 and Figure 5, there are two signals generated internally for CDS sampling

System Overview (continued)

referred to as CLAMP and SAMPLE.These signals provide the rising edge reference for the sampling of the CCD input signal. The timing of CLAMP and SAMPLE is derived from the clock; therefore, shifting the clock phasing with respect to the CCD input signal would also shift the rising (and falling) edges of CLAMP and SAMPLE. The actual sampling of the CCD's reset voltage and video signal is performed on the falling edges of the CLAMP and SAMPLE signals respectively. The user may modify the position of the falling edges where the sampling of the CCD input occurs by driving the SHP and SHD inputs of the LM98503. The falling edges of SHP and SHD will supersede the falling edges of CLAMP and SAMPLE respectively and cause the duration of the sample pulse to shorten accordingly. As evidenced in Figure 4 and Figure 5, the falling edges of SHP and SHD should not occur earlier than t_{SHP} or t_{SHD} after the respective falling [SHP] (or rising [SHD]) edge of CLK.

1.6 Serial Interface and Configuration Registers

There are many options available to the user that may be programmed via the LM98503's serial interface. Configuration values are stored in registers for use by several functions such as programmable gain, offset, black level, and color filter array.

The LM98503's serial interface is used to store values into 16 8-bit configuration registers. Upon power-up or external reset, the configuration registers will contain their respective default values. Default values place the LM98503 in 'single channel' mode, where only one PGA gain and offset are applied to the input signal.

The master CLK input is required to be running during serial interface commands. Each command issued through the serial interface must have a minimum of 13 data bits (see Figure 12 and Figure 13).

1.7 PGA Gain Registers

Four PGA gain registers store four possible gain values for the programmable gain amplifier (PGA). For example, these four gain values may correspond to four possible colors in a color filter array.

1.8 Analog Offset

Four analog offset registers store four possible offset values that correspond to the four PGA gain values. For example, the value stored in the PGA gain register 0 (address 0h) is used in conjunction with the offset value stored in the analog offset register 0 (address 4h). This allows for four possible combinations of PGA gain and analog offset, one for each color filter. These registers are read-only when offset auto-calibration is enabled in the software control register 0. It should be noted that each offset DAC step (1 LSB) corresponds to a 0.4 LSB step at the ADC output. Therefore, if an offset of 20 digital codes is desired at the ADC output, a digital code value of 50 should be stored in the analog offset register(s). As a result, the maximum offset seen at the ADC output as a result of digital code values stored in the analog offset register(s) is ±54 codes. It is possible to increase the digital output range of the analog offset DAC, resulting in an increased maximum ADC output code corresponding to a given DAC input, but at the expense of DAC step resolution. For more information on increasing the DAC range, please see "Analog Offset DAC Range Adjustment" on page 23.

1.9 Output Black Level

The output black level register is occupied by an 8-bit word stored by the user that specifies the output level corresponding to optical black. For example, a user that wants an output level of 16 for black pixels must write this value into the register during the horizontal interval. Note that it is not recommended that a value of 0 be stored as the output black level. Once this has been accomplished, driving the BLKCLP high for 20 cycles of CLK activates the digital black clamp loop and the black level is forced to the value stored in the output black level register, in the example case the code value of 16. As a result of the relationship between the DAC input and the ADC output, under default conditions the largest black level code the LM98503 is capable of clamping to is 36 codes. As a result, the offset DAC may be 'pinned' at full range when the default setting of 32 is used. When this occurs, the result may be that the DAC is unable to correct line to line variations in the black level. consequently, horizontal lines or 'banding' may be observed. See Analog Offset DAC Range Adjustment, Section 3.0 of the applications information for instructions on how to increase this range.

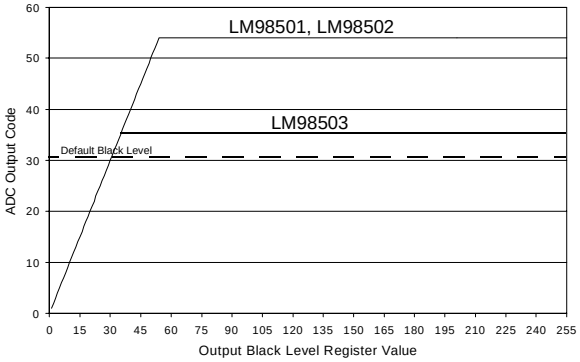


Figure 11: ADC Output vs. Black Level Register Value

1.10 Color Filter Array (CFA) Configuration

In order to utilize the LM98503's programmable pixel-rate gain, a color filter array (CFA) pattern must be defined. Some commonly used CFA patterns are as follows:

Bayer Pattern

Line 0	Green	Red	Green	Red
Line 1	Blue	Green	Blue	Green

CMYG Pattern

Line 0	Cyan	Magenta	Yellow	Green
Line 1	Cyan	Green	Yellow	Magenta

Therefore, two 8-bit words must be written to the CFA line registers to specify the CFA pattern being used. Also, two 2-bit numbers must be written to the CFA definition register indicating the number of pixels per pattern in each line of the defined CFA pattern. The information contained in the CFA line registers indicates the registers where the respective PGA gain and offset values are stored. For example, a system using the Bayer pattern defined above would first write four PGA gains and their respective offsets into the four PGA gain and four analog offset registers. Next, two 8-bit words (one word/CFA line) would be written to the CFA configuration registers. The 8-bit CFA configuration words each consist of four 2-bit numbers, each of which is the address for the gain and offset values of the of the color that appears in that location in the CFA line. Finally, two 2-bit numbers specifying the number of elements in each CFA line must be written into the CFA definition register. A CFA configuration will then contain four 2-bit numbers indicating the registers where the gain and offset values are located for a

System Overview (continued)

configuration will then contain four 2-bit numbers indicating the registers where the gain and offset values are located for a maximum of four colors on each CFA line. In addition, the CFA definition register will contain two 2-bit numbers that designate the number of elements used in each CFA line for the particular CFA pattern being applied to the system.

Example A contains a CFA pattern that repeats the colors cyan and magenta on the first line, and repeats the pattern blue, green, green, blue on the second line. Each 2-bit number in the CFA line registers refers to a common set of PGA gain and offset registers for each color. The first line indicates that the color magenta uses the gain and offset values stored in PGA gain register 1 (address 1h) and analog offset register 1 (address 5h). Also, the first line indicates that the color cyan uses the gain and offset values in PGA gain register 2 (address 2h) and analog offset register 2 (address 6h). The second line indicates gain and offset values for the color blue and the color green in the same fashion as the first line.

Example A

	7			0
CFA Line 0	XX	XX	01	10
CFA Line 1	11	00	00	11
CFA Definition	00	00	11	01

In addition to specifying the gain and offset for each line, it is also necessary to specify the number of elements contained in each CFA line's pixel pattern. The CFA definition register is used to store this value (number of elements per line). In example A, the user has stored the 2-bit binary number **01** into the CFA definition register's two LSB's indicating that the pattern in line 0 contains two repeating colors or elements. Also, the 2-bit binary number **11** has been written into bit 2 and bit 3 of the CFA definition register indicating that the respective CFA pattern contains four repeating colors or elements, as the colors blue and green alternate position in the example pattern.

Once both lines for the pattern have been stored, it is applied when the beginning of line (BOL) signal is asserted by the user. One line of the CFA pattern is applied repeatedly until the BOL signal is reset (at the end of the current line). Once the BOL signal is set again, the CFA line information is changed from that defined by the CFA line 0 register to that defined by the CFA line 1 register and the process starts again. For more details of the timing of the BOL signal, please refer to Figure 6.

1.11 Software Control

There are two software control registers accessible via the serial interface. The software control registers are divided into customer (register 0) and advanced (register 1) functions. Please refer to the register data descriptions for more information on the software control registers.

1.12 Power Level Control

The LM98503 is equipped with two power trim registers that may be used to adjust power levels of various circuits internal to the device. In its default condition, the LM98503 is set for optimum power and performance, and modifying the values stored in the power level control registers will affect performance as a result of the change in power level(s). In applications where maximum performance is desired, the default values should be used. Otherwise, power levels may be decreased at the slight expense of performance. Please refer to the register data descriptions for more information regarding the power level control registers.

The ADC coarse and fine bank power adjustment bits are located in the power level control 2 register, bits 7:4. Altering these bits may significantly affect performance and power dissipation. Please see 'DNL vs. Power Control Setting @ 18MHz Clock Frequency' and 'Power Dissipation vs. Power Control Setting' on page '13.

Register Memory Map

Title	Address	Default Value
PGA Gain 0	0000	0000 0000 (0d)
PGA Gain 1	0001	0000 0000 (0d)
PGA Gain 2	0010	0000 0000 (0d)
PGA Gain 3	0011	0000 0000 (0d)
Analog Offset 0	0100	0000 0000 (0d)
Analog Offset 1	0101	0000 0000 (0d)
Analog Offset 2	0110	0000 0000 (0d)
Analog Offset 3	0111	0000 0000 (0d)
CFA Configuration 0	1000	0000 0000 (0d)
CFA Configuration 1	1001	0000 0000 (0d)
CFA Definition	1010	XXXX 0000 (0d)
Output Black Level	1011	0001 0000 (32d)
Software Control 0	1100	0100 1110 (78d)
Software Control 1	1101	XX00 0X00 (0d)
Power Level Control 0	1110	1010 1010 (170d)
Power Level Control 1	1111	0101 1010 (90d)

Register Data

The following section describes all available registers in the LM98503 register bank and their functions.

2.0 PGA Gain Registers

Register Name PGA Gain 0
Address 0 Hex
Type Read/Write
Reset Value 0000 0000 Binary

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB - 32.0dB in 0.125dB steps.

Register Name PGA Gain 1
Address 1 Hex
Type Read/Write
Reset Value 0000 0000 Binary.Register NamePGA Gain

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB - 32.0dB in 0.125dB steps.

2
Address 2 Hex
Type Read/Write
Reset Value 0000 0000 Binary

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB - 32.0dB in 0.125dB steps.

Register Name PGA Gain 3
Address 3 Hex
Type Read/Write
Reset Value 0000 0000 Binary

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB - 32.0dB in 0.125dB steps.

3.0 Analog Offset Registers

Register Name Analog Offset 0
Address 4 Hex
Type: Read/Write
Reset Value 0000 0000 Binary

Bit	Bit Symbol	Description
[7:0]	Signed Analog Offset	Digital representation of the analog offset to be applied to the input of the PGA. See “Analog Offset” on page 15.

Register Data (continued)

Register Name **Analog Offset 1**
Address **5 Hex**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Signed Analog Offset	Digital representation of the analog offset to be applied to the input of the PGA. See "Analog Offset" on page 15.

Register Name **Analog Offset 2**
Address **6 Hex**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Signed Analog Offset	Digital representation of the analog offset to be applied to the input of the PGA. See "Analog Offset" on page 15.

Register Name **Analog Offset 3**
Address **7 Hex**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Signed Analog Offset	Digital representation of the analog offset to be applied to the input of the PGA. See "Analog Offset" on page 15.

4.0 Color Filter Array Registers

Register Name **Color Filter Array Configuration 0**
Address **8 Hex**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[7:6]	Line0:Pixel3 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 3 of the CFA pattern are stored.
[5:4]	Line0:Pixel2 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 2 of the CFA pattern are stored.
[3:2]	Line0:Pixel1 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 1 of the CFA pattern are stored.
[1:0]	Line0:Pixel0 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 0 of the CFA pattern are stored.

Register Name **Color Filter Array Configuration 1**
Address **9 Hex**
Type **Read/Write**
Reset Value **0000 0000 Binary)**

Bit	Bit Symbol	Description
[7:6]	Line1:Pixel3 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 3 of the CFA pattern are stored.
[5:4]	Line1:Pixel2 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 2 of the CFA pattern are stored.
[3:2]	Line1:Pixel1 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 1 of the CFA pattern are stored.
[1:0]	Line1:Pixel0 Gain/Offset	2 LSB's of register addresses where the gain and offset for pixel 0 of the CFA pattern are stored.

Register Name **Color Filter Array Definition**
Address **A Hex**
Type **Read/Write**
Reset Value **XXXX 0000 Binary**

Bit	Bit Symbol	Description
[3:2]	Line 1 Pixels	Number of pixels in CFA pattern defined in CFA line 1.
[2:1]	Line 0 Pixels	Number of pixels in CFA pattern defined in CFA line 0.

5.0 Output Black Level Register

Register Name **Output Black Level**
Address **B Hex**
Type **Read/Write**
Reset Value **0001 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Black Level	0 - 256 output black level digital code value. (see "Output Black Level" on page 15)

6.0 Software Control Registers

Register Name **Software Control 0 (Customer)**
Address **C Hex**
Type **Read/Write**
Reset Value **0100 1110 Binary**

Bit	Bit Symbol	Description
[7]	Offset Output Enable	Directs the offset error calculated by the digital black level correction loop to the 10 digital output data pins.
[6]	Serial Output Enable	Enables the serial interface output for reading register values.

Register Data (continued)

Register Name **Software Control 1**
Address **D Hex**
Type **Read/Write**
Reset Value **XX00 0X00 Binary**

Bit	Bit Symbol	Description
[5:4]	Analog Output Select	Routes the selected internal analog signal to the differential analog output pins AOUT+ and AOUT-. **00 CDS** **01 PGA Stage 1** **10 PGA Stage 2** **11 PGA Stage 3**
[3]	Analog Output Enable	Enables the differential analog output pins AOUT+ and AOUT-. If the analog outputs are disabled, the pins should not be loaded.
[1]	ADC Reference Select	Reference biasing selection for the analog-to-digital converter. **0 Passive biasing (resistors)** **1 Active biasing (bandgap)**
[0]	DAC Reference Select	Reference biasing selection for the digital-to-analog converter. **0 Active biasing (bandgap)** **1 Passive biasing (resistors)**
[5:4]	Offset Integration	Offset integration factor selection: **00 No Scaling** **01 Divide-by-4** **10 Divide-by-8** **11 Divide-by-16**
[3]	Offset Auto-Calibration Enable	Enables the digital black level correction loop. A*nalog offset registers are read-only when offset auto-calibration is enabled*.
[2]	SHP/SHD Active-HIGH Enable	Inverts the SHP and SHD inputs causing the CDS to sample on the rising edges of SHP and SHD. *Sampling is performed on the falling edges of SHP and SHD when the signals are active-low.*
[1]	CDS Enable (*AUX-In disable*)	Instructs the CDS to sample the CCD input. *Otherwise, the AUX In input is sampled in sample-and-hold mode*.
[0]	Analog Power Down	Cuts power to the on-chip analog circuitry including the CDS, PGA, ADC, and bandgap references.

Register Name **Power Level Control 0**
Address **E Hex**
Type **Read/Write**
Reset Value **1010 1010 Binary**

Bit	Bit Symbol	Description
[7:6]	PGA Stage 1 Amplifier Bias	Adjusts the power level of the PGA stage 1 amplifier. The power level is relative to the value of the binary number stored.
[5:4]	PGA Common-Mode Input Bias	Adjusts the power level of the PGA common-mode input. The power level is relative to the value of the binary number stored.
[3:2]	CDS Amplifier Bias	Adjusts the power level of the CDS amplifier. The power level is relative to the value of the binary number stored.
[1:0]	CDS Common-Mode Input Bias	Adjusts the power level of the CDS common-mode input. The power level is relative to the value of the binary number stored.

Register Name **Power Level Control 1**
Address **F Hex**
Type **Read/Write**
Reset Value **0101 1010 Binary**

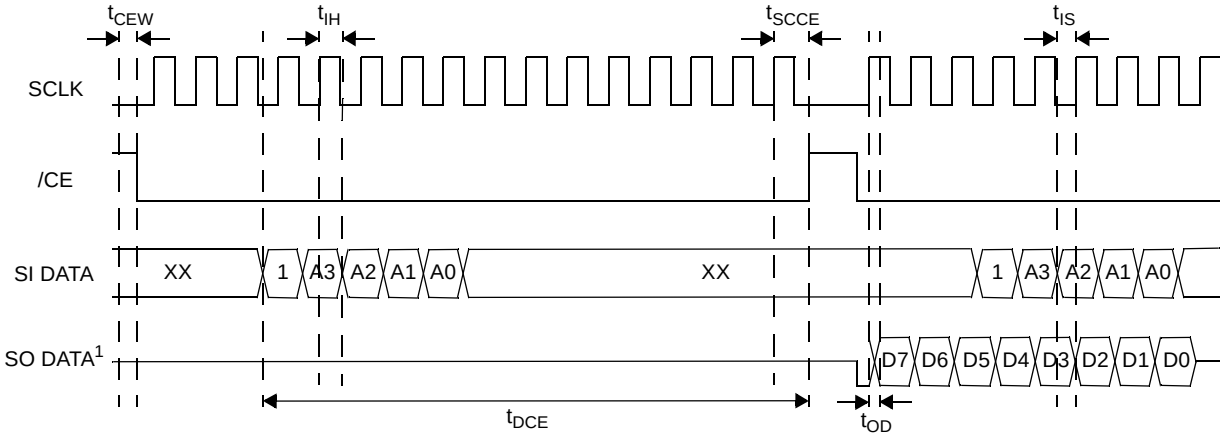
Bit	Bit Symbol	Description
[7:6]	ADC Coarse Bank Bias	Adjusts the power level of the ADC coarse bank. The power level is relative to the value of the binary number stored.
[5:4]	ADC Fine Bank Bias	Adjusts the power level of the ADC fine bank. The power level is relative to the value of the binary number stored.
[3:2]	PGA Stage 3 Amplifier Bias	Adjusts the power level of the PGA stage 3 amplifier. The power level is relative to the value of the binary number stored.
[1:0]	PGA Stage 2 Amplifier Bias	Adjusts the power level of the PGA stage 2 amplifier. The power level is relative to the value of the binary number stored.

Serial Interface Timing Specifications

The following specifications apply for all supply pins = +3.0V, C_L = 10pF, and f_{CLK} = 18MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

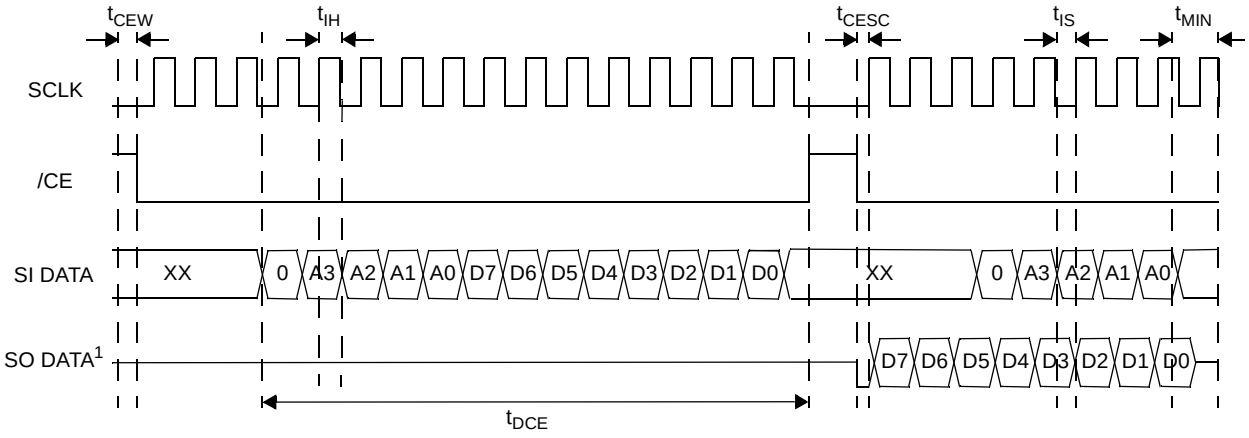
Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
t_{MIN}	SCLK Period		55			ns
	SCLK Duty Cycle			50/50	60/40	%
	SCLK Rise / Fall Time				4	ns
t_{CESC}	SCLK Start Time After $\overline{CE}$ Low		10			ns
t_{DCE}	Input Data to $\overline{CE}$ Rising Edge		13			t_{MIN}

Serial Interface Timing



[1] Serial output enable must be set in software control 0 for SO DATA output. Please see register data section for more information.

Figure 12: Serial Interface Read Command Timing



[1] Serial output enable must be set in software control 0 for SO DATA output. Please see register data section for more information.

Figure 13: Serial Interface Write Command Timing

Serial Interface Read/Write Description

1.0 Writing to the Serial Registers

To write to the serial registers, the timing diagram shown in Figure 13 must be met. First $\overline{CE}$ is toggled low. SI DATA may then be clocked in, and the data present on the rising edge of the serial clock is loaded in. The data continues to be clocked in, until $\overline{CE}$ toggles high. The data present in the register is the last 13 bits of data sent before $\overline{CE}$ toggled high. Therefore, for example, if 20 bits were sent when $\overline{CE}$ was toggled low, the first 7 bits were discarded, and the data loaded are the remaining 13 bits. As seen in Figure 13, these 13 bits are composed of 8 data bits, 4 address bits, and 1 read/write bit. When writing to the registers, the read/write bit must be low. When $\overline{CE}$ toggles high, the register is written to, and the LM98503 now functions with this new data.

2.0 Reading the Serial Registers

To read the serial registers, the timing diagram shown in Figure 12 must be met. When $\overline{CE}$ is toggled low, and data is loaded as described above in the writing sequence. When $\overline{CE}$ toggles high, the new 13 bit word is considered, except this time the read/write bit should be a 1 indicating a read. The 8 data bits are not considered, but act only as place holders. When $\overline{CE}$ toggles low again, the data that resides at the address considered in the previous read or write routine, begins clocking out SO DATA. The data streams out MSB-LSB as shown in Figure 12. Whether a read or a write was invoked in the previous sequence, the SO DATA will clock out the contents of the address considered in the previous sequence.

PGA Gain Plots

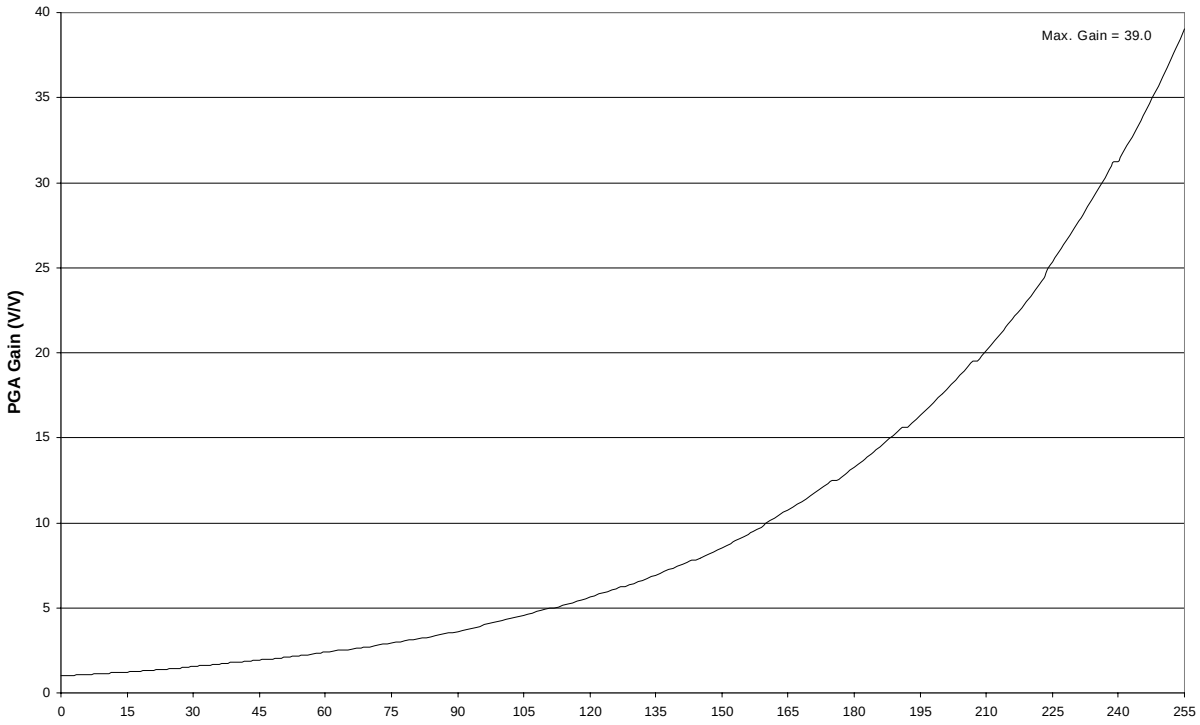


Figure 14: PGA Gain (Linear Scale) vs. PGA Gain Code

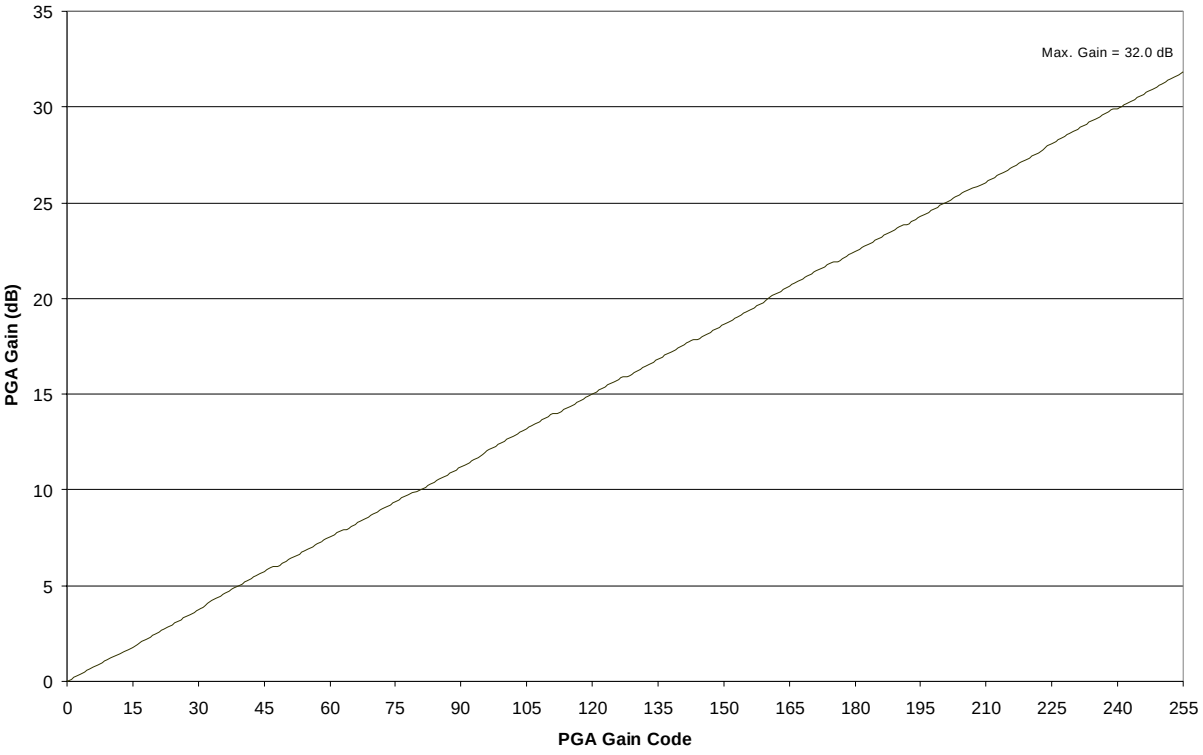


Figure 15: PGA Gain (Logarithmic Scale) vs. PGA Gain Code

Applications Information

3.0 Analog-to-Digital Converter Reference Bypassing

Figure 16 shows a simple reference bypassing scheme with minimal components. The V_{REFT} and V_{REFB} pins should each be bypassed to analog ground with 10µF tantalum as well as 0.1µF ceramic capacitors. In a case where the internally generated reference voltages are not sufficient, the user may supply external voltages to the reference pins. However, the reference pin V_{REFT} should be within the range of 2.0 to 2.5 Volts. Similarly, V_{REFB} should be driven in the range of 0.4 to 0.9 Volts. Any device used to drive the reference pins should be able to source adequate current into the V_{REFT} and sink adequate current from the V_{REFB} pin when the reference resistor ladder is at its minimum resistivity of 850Ω.

The reference voltage at the top of the resistor ladder (V_{REFT}) may be as low as 1.2 Volts above the voltage at the bottom of the resistor ladder (V_{REFB}) and may be as high as 1.8 Volts above. V_{REFB} may be as low as 0.4 Volts and as high as 0.9 Volts above ground. However, noise effects will be minimized and accurate conversions insured when the total reference voltage is approximately 2.25 Volts and offset from ground by 0.75 Volts.

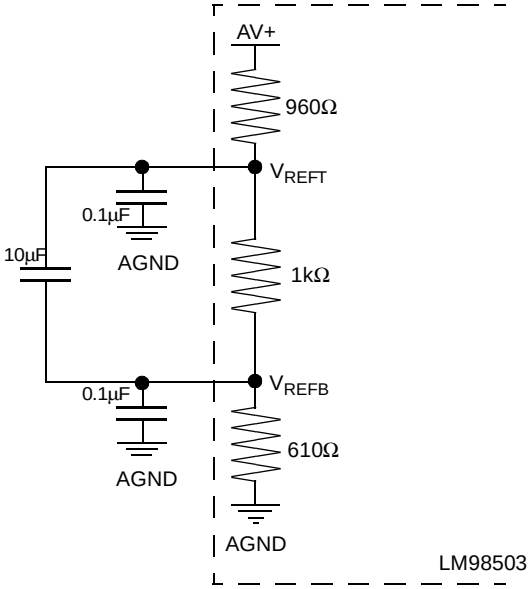


Figure 16: Reference Bypassing

4.0 Analog Offset DAC Reference Bypassing

The analog offset DAC reference pins, VREFP and VREFN, should be capacitively bypassed in the same fashion as the ADC reference pins VREFT and VREFB (See “Analog-to-Digital Converter Reference Bypassing”).

5.0 Analog Offset DAC Range Adjustment

The analog offset DAC has an input range of ±127 LSB (see “Register Data” on page 17). Each DAC LSB corresponds to approximately 0.4 LSB at the ADC output. Therefore, the offset DAC is limited to providing offset values less than or equal to ±64 LSB at the ADC output. In some applications, this range of output may not be sufficient. It is possible to increase the range of the DAC by adjusting the DAC reference range. The DAC reference range may be adjusted by lowering the voltage at the lower DAC reference voltage pin, VREFN, via use of a pull-down resistor from VREFN to AGND. A resistor value of 1.50kΩ will increase the DAC range by a factor of 2.0x, allowing for offsets of ±128 LSB to be applied at the ADC output rather than the default maximum and minimum offsets of ±64 LSB, resulting in a 0.8 LSB DAC step to 1 LSB ADC output step relationship.

Power Supply Considerations

The LM98503 may draw a sufficient amount of current to corrupt improperly bypassed power supplies. A 10µF to 50µF capacitor should be placed within 1cm of the analog power (AV+) pins of the device in parallel with a 0.1µF ceramic chip capacitor placed as close to the device as layout permits. Leadless chip capacitors are preferred because they have a low lead inductance. As is the case with virtually all high-speed semiconductors, the LM98503 should be assumed to have little power supply rejection; therefore, a noise-free analog power source is required.

The analog and digital power supplies of the LM98503 should be sourced from the same supply voltage, but the supply pins should be well isolated from one another. Isolating the supplies prevents digital noise from coupling back into the analog supply pins. A choke (ferrite bead) is recommended to be placed between the analog and digital power supply pins as well as a ceramic chip capacitor placed as close as possible to the analog supply pin(s) of the device. Additionally, it is not recommended that the LM98503’s digital supply be used for any other digital circuitry on the circuit board. All other digital devices should be powered from a separate digital supply well isolated from both the analog and digital supplies of the LM98503.

6.0 The LM98503 Clock

Although the LM98503 is tested and its performance guaranteed with a 18MHz clock, it typically will function with clock frequencies ranging from 1MHz to 20MHz (see the LM98501 for conversion speeds greater than 20MHz). Performance is best if the clock rise and fall times are less than 5ns and the clock trace is terminated near the clock input pin with a series RC network consisting of a 100Ω resistor and a 47pF capacitor.

7.0 Layout and Grounding Techniques

The proper routing of all signals and pertinent grounding techniques are essential to insure the best signal-to-noise ratio and dynamic performance possible. Separate analog and digital ground planes ease meeting the datasheet limits. The analog ground plane should be low impedance and free from noise of other components of the system. All bypass capacitors should be located as close to the pin as possible and connected to the appropriate ground plane with short traces (<1cm). The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input.

Figure 17 provides an example of a suitable layout, including power supply routing, ground place separation, and bypass capacitor placement. All input amplifiers, filters, and reference components should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be placed over and grounded via the digital ground plane. Digital and analog signal lines should never run parallel to each other in close proximity with each other. These signals should only cross when absolutely necessary and then only at 90° angles.

Applications Information (continued)

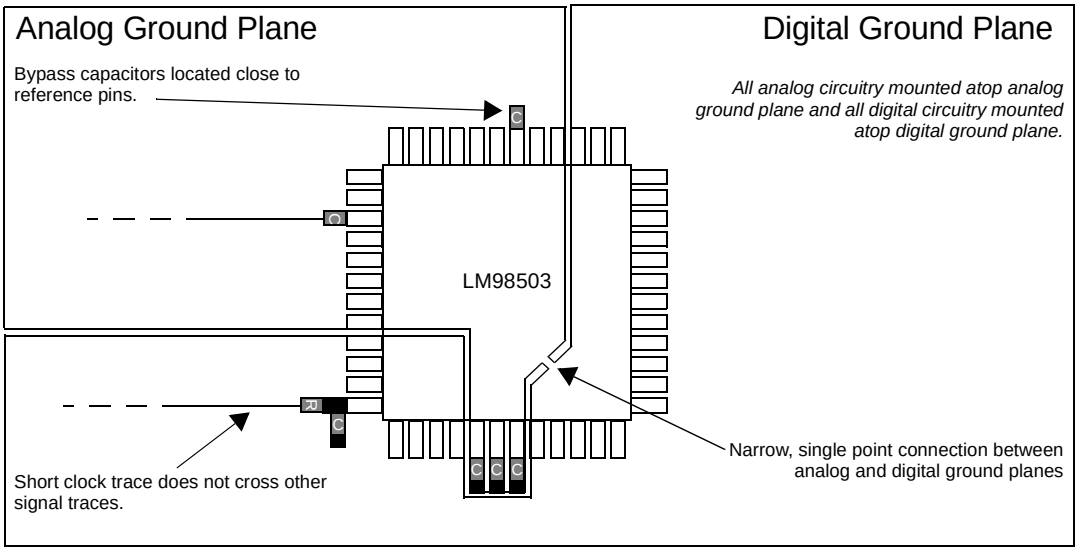


Figure 17: Recommended Layout Pattern

8.0 Dynamic Performance

The LM98503 is AC tested and its dynamic performance is guaranteed. The clock source driving the CLK input must be free of jitter. For best AC performance, the clock source should be isolated from other system digital circuitry with a clock tree buffer(s). Meeting noise specifications depends largely upon keeping digital noise out of the analog input of the LM98503.

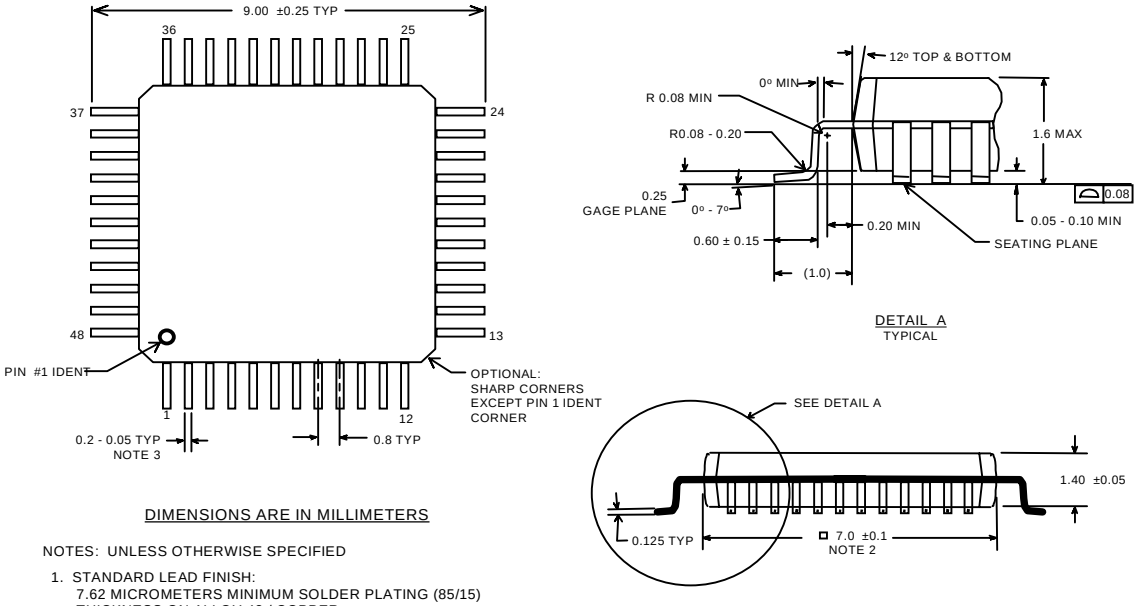
9.0 Common Application Pitfalls

Driving the inputs (analog or digital) beyond the power supply potential. For proper operation, all input potentials should not be greater than 300mV above that of the power supply. It is not uncommon for high speed digital circuits (e.g. 74F and 74AC devices) to exhibit undershoot that falls to a potential greater than 1.0 Volt below the ground potential and overshoot that rises to a potential greater than 1.0 Volt above the power supply potential. A resistor of 50Ω to 100Ω in series with the offending digital input will, in most cases, eliminate this problem.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers have to charge for each conversion output, the more current is required from the DV+ I/O and DGND I/O supply pins. The large charging current spikes can couple into the analog section and subsequently may degrade dynamic performance of the system. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem on the application system board. Buffering the digital data outputs may be necessary if the data bus being driven by the LM98503 is heavily loaded. Dynamic performance may also be improved by adding series resistors of 47Ω at each digital output.

Driving the reference pins with devices that cannot source or sink the current required by the reference resistor ladder. As mentioned previously, any devices driving the reference resistor ladder must source sufficient current into the top of the ladder. Additionally, the device connected to the bottom ofladder voltages are not stable the converter output will not generate ladder must be able to sink the necessary amount of current to thekeep the reference voltage(s) stable. If the reference resistor predictable output codes.

Physical Dimensions (millimeters)



DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON ALLOY 42 / COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
   MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
3. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE PROTRUSION SHALL BE 0.15mm.
4. REFERENCE JEDEC REGISTRATION MO-136, VARIATION BE.
   DATED 4/93.

VBH48A

48 Lead LQFP Package
Order Number LM98503CCVV
NS Package Number VBH48A

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