Rev 3.3 March 2005

National Semiconductor

LM98513 Dual-Channel, 10-Bit, 50 MSPS Copier Signal Processor

General Description

The LM98513 is a fully integrated, high performance 10-Bit, 50 MSPS CCD signal processing solution for digital copiers and scanners. High-speed signal throughput is achieved with an innovative 2-channel architecture including sample and hold, programmable gain and offset correction and analog-to-digital conversion. The fully differential processing channels show exceptional noise immunity, having a very low noise floor of -68dB each. The fast, temperature stable, 8 bit programmable gain amplifiers are linear-in-dB which enables fine adjustments to the signal gain and minimizes cross-channel gain error caused by mismatch in the CCD output circuitry. The independently controlled offset correction circuits utilize 8-bit offset DACs to correct signal and cross-channel offsets. The 10-bit analog-to-digital converters have excellent dynamic performance making the LM98513 transparent in the image reproduction chain.

Applications

- Digital Plain Paper Copiers
- Multi-Function Printers
- Facsimile Equipment
- Desktop Publishing
- Flatbed or Handheld Color Scanners
- High-speed Document Scanner

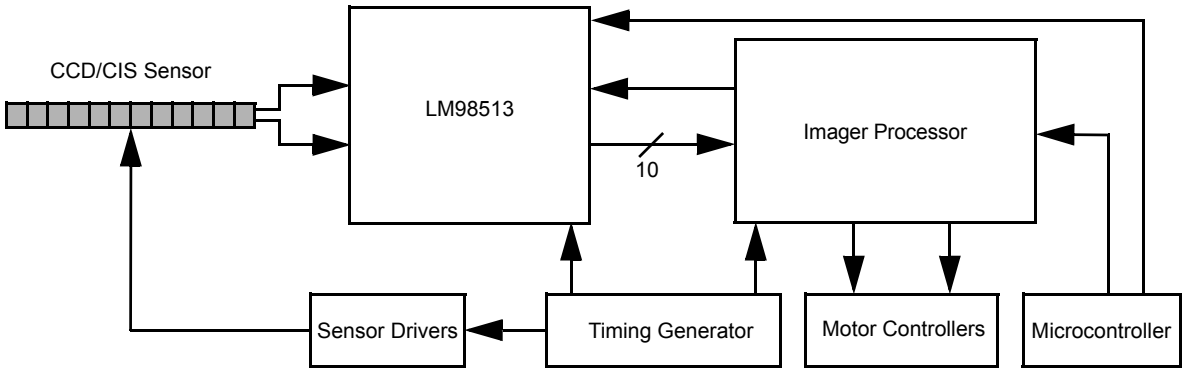
Features

- 3 Volt Single Power Supply
- Low Power CMOS Design
- 4 Wire Serial Interface
- 2.5 Volt Data Output Levels
- Dual Inputs with Symmetrical Architecture
- Even/Odd Channel Offset Correction
- Digital Black Level Clamp
- Programmable Input Clamp

Key Specifications

Maximum Input Level	1.5 Volt peak-peak
Input Sampling Rate	25 MSPS
PGA Gain Steps	256 Steps
PGA Gain Range	0.0 - 20.0 dB
ADC Resolution	10-Bit
ADC Sampling Rate	25 MSPS
Noise Floor 0.0 dB Gain,1.5 Volt input	-68dB
Power Dissipation AV+=DV+=DV+I/O=3.0V	415 mW (typical)
Operating Temp	0 to 70^{o}C

System Block Diagram



Overall Chip Block Diagram

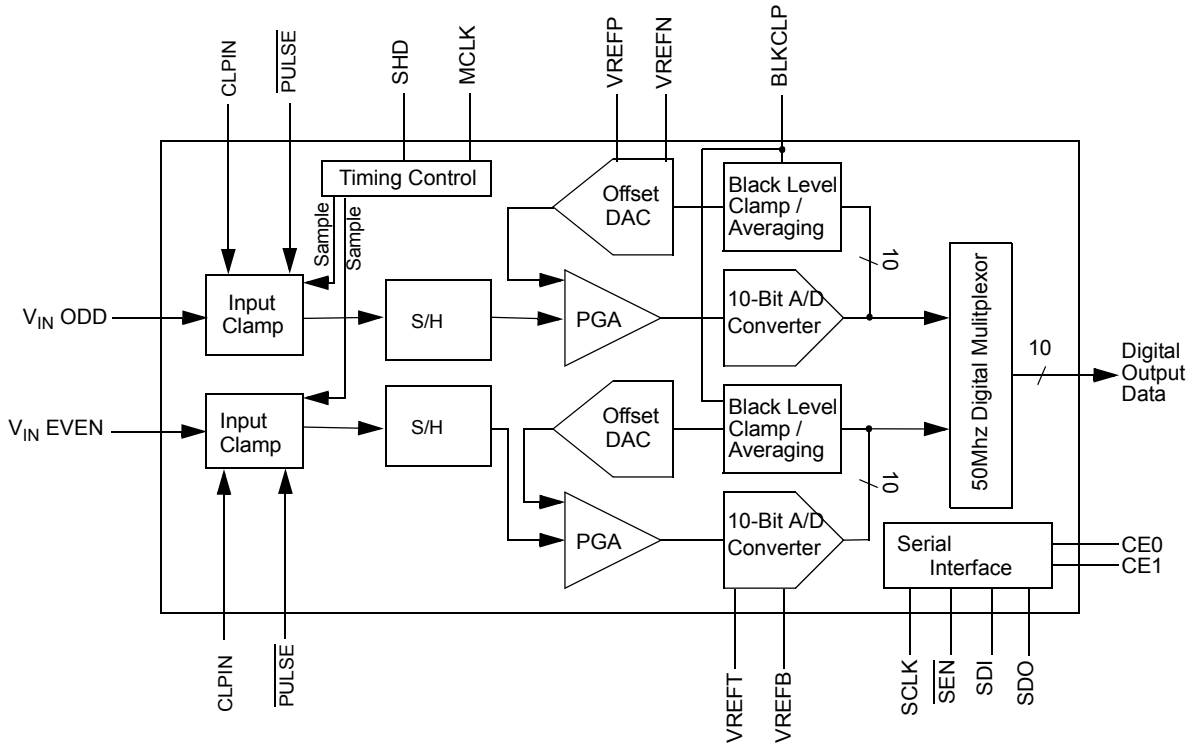


Figure 1: Chip Block Diagram

LM98513 TSSOP Chip Pin Out Diagram

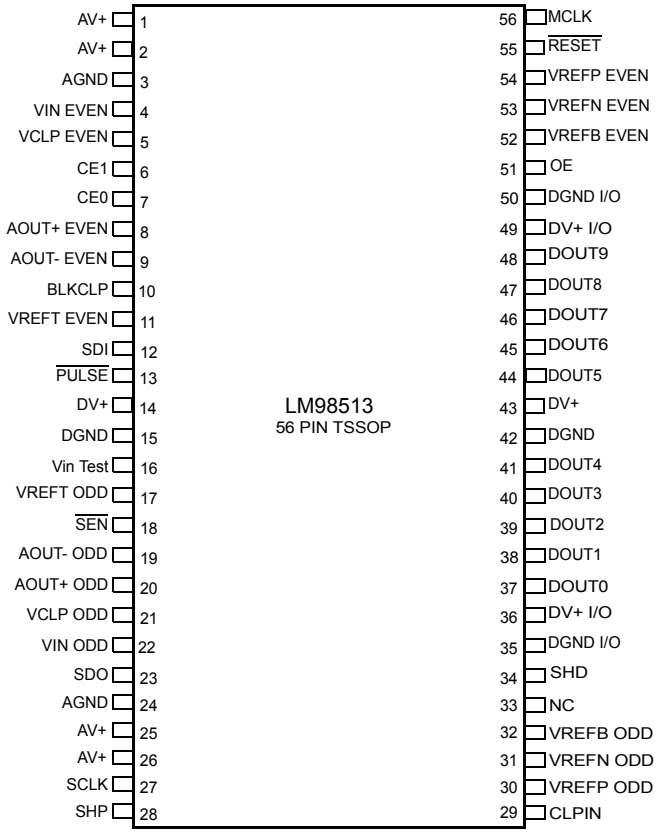


Figure 2: LM98513 Pin Out Diagram

Ordering Information

Commercial ($0°C \leq T_A \leq +70°C$)	NS Package
LM98513 CCMT	TSSOP

Typical Application Circuit

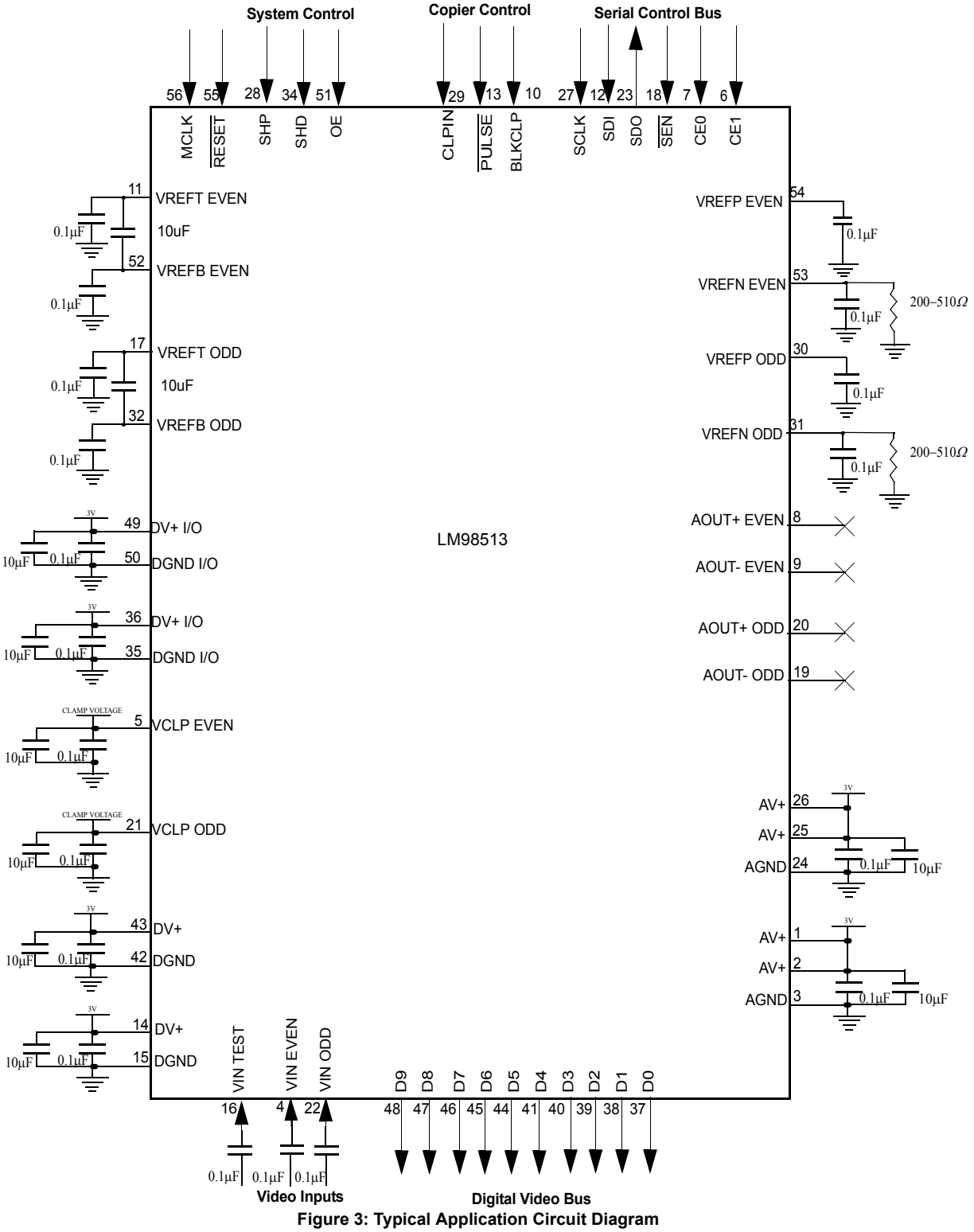


Figure 3: Typical Application Circuit Diagram

Pin Descriptions

Pin	Name	I/O	Typ	Res	Description
1	AV+	I	P		+3.3 Volt power supply for the analog circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
2	AV+	I	P		+3.3 Volt power supply for the analog circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
3	AGND		P		Analog ground return.
4	VIN EVEN	I	A		Even channel analog input signal. AC-couple to imager output through a 0.1μF capacitor.
5	VCLP EVEN	IO	A		Input Clamp Voltage (1.5V). Normally bypassed with a 0.1μF, and a 10μF capacitor to ground. An external reference voltage may be applied to this pin.
6	CE1	I	D		MSB of Chip Enable function for use in systems with multiple LM98513s in conjunction with the serial interface. See ”Chip Enable” on page 14.
7	CE0	I	D		LSB of Chip Enable function for use in systems with multiple LM98513s in conjunction with the serial interface. See ”Chip Enable” on page 14.
8	AOUT+ EVEN	O	A		Even channel positive differential analog output from S/H or PGA. AOUT+ EVEN should be left as NC when function is not being employed. See ”Analog Output Option” on page 14.
9	AOUT- EVEN	O	A		Even channel negative differential analog output from S/H or PGA. AOUT- EVEN should be left as NC when function is not being employed. See ”Analog Output Option” on page 14.
10	BLKCLP	I	D	PD	Active-high black level clamp switch input. Pulse high during black pixels to eliminate black pixel offset from video signal. BLKCLP should be tied to DGND when auto-BLKCLP pulse is enabled or the function is not being employed.
11	VREFT EVEN	IO	A		Top of even channel ADC reference ladder. Normally bypassed with a 0.1μF capacitor to ground and 10μF cap to VREFB EVEN. An external ADC reference voltage may be applied to this pin.
12	SDI	I	D		Serial interface input port.
13	$\overline{\text{PULSE}}$	I	D	PU	External Input Clamp Pulse.
14	DV+	I	P		+3.3 Volt power supply for the digital circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
15	DGND		P		Digital ground return.
16	VIN TEST	I	A		Test input. See ”VIN Test Option” on page 13.
17	VREFT ODD	IO	A		Top of odd channel ADC reference ladder. Normally bypassed with a 0.1μF capacitor to ground and 10uF cap to VREFB ODD. An external ADC reference voltage may be applied to this pin.
18	$\overline{\text{SEN}}$	I	D		Active-low chip enable for the serial interface.
19	AOUT- ODD	O	A		Odd channel negative differential analog output from S/H or PGA. AOUT- ODD should be left as NC when function is not being employed. See ”Analog Output Option” on page 14.
20	AOUT+ ODD	O	A		Odd channel positive differential analog output from S/H or PGA. AOUT+ ODD should be left as NC when function is not being employed. See ”Analog Output Option” on page 14.
21	VCLP ODD	IO	A		Input Clamp Voltage (1.5V). Normally bypassed with a 0.1μF, and a 10uF capacitor to ground. An external reference voltage may be applied to this pin.

Pin	Name	I/O	Typ	Res	Description
22	VIN ODD	I	A		Odd channel analog input signal. AC-couple to imager output through a 0.1μF capacitor.
23	SDO	O	D		Serial interface output port.
24	AGND		P		Analog ground return.
25	AV+	I	P		Power supply for the analog circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
26	AV+	I	P		Power supply for the analog circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
27	SCLK	I	D		Serial interface shift register clock.
28	SHP		D		Clamp override. (Not used in the LM98513) Connect to GND if Analog Input Control Register bit [0] = 0 (default). Connect to Vdd if bit[0] = 1.
29	CLPIN	I	D	PD	Input Clamp Enable.
30	VREFP ODD	IO	A		Top of odd channel DAC reference ladder. Normally bypassed with a 0.1μF capacitor to ground. An external DAC reference voltage may be applied to this pin.
31	VREFN ODD	IO	A		Bottom of odd channel DAC reference ladder. Normally bypassed with a 0.1μF capacitor. An external DAC reference voltage may be applied to this pin.
32	VREFB ODD	IO	A		Bottom of odd channel ADC reference ladder. Normally bypassed with a 0.1μF capacitor to ground, and a 10μF capacitor to VREFT ODD. An external ADC reference voltage may be applied to this pin.
33	NC				
34	SHD	I	D		Sample override. Programmable active-high or active-low through serial interface. Connect to ground when function not being used (registers values in default condition).
35	DGND I/O		P		Digital output driver ground return.
36	DV+ I/O	I	P		Power supply for the digital output driver circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
37	DOUT0	O	D		Digital output. Bit 0 of 10 of the digital video output bus.
38	DOUT1	O	D		Digital output. Bit 1 of 10 of the digital video output bus.
39	DOUT2	O	D		Digital output. Bit 2 of 10 of the digital video output bus.
40	DOUT3	O	D		Digital output. Bit 3 of 10 of the digital video output bus.
41	DOUT4	O	D		Digital output. Bit 4 of 10 of the digital video output bus.
42	DGND		P		Digital ground return.
43	DV+	I	P		Power supply for the digital circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
44	DOUT5	O	D		Digital output. Bit 5 of 10 of the digital video output bus.
45	DOUT6	O	D		Digital output. Bit 6 of 10 of the digital video output bus.
46	DOUT7	O	D		Digital output. Bit 7 of 10 of the digital video output bus.
47	DOUT8	O	D		Digital output. Bit 8 of 10 of the digital video output bus.
48	DOUT9	O	D		Digital output. Bit 9 of 10 of the digital video output bus.

Pin	Name	I/O	Typ	Res	Description
49	DV+ I/O	I	P		Power supply for the digital output driver circuits. Bypass supply each supply pin with 0.1μF and 10μF capacitors in parallel.
50	DGND I/O	I	P		Digital output driver ground return.
51	OE	I	D	PU	Output enable function for digital output bus. Digital output bus will be held in tri-state when OE is driven low.
52	VREFB EVEN	IO	A		Bottom of even channel ADC reference ladder. Normally bypassed with a 0.1μF capacitor to ground, and a 10μF capacitor to VREFTEVEN. An external ADC reference voltage may be applied to this pin.
53	VREFN EVEN	IO	A		Bottom of even channel DAC reference ladder. Normally bypassed with a 0.1μF capacitor. An external DAC reference voltage may be applied to this pin.
54	VREFP EVEN	IO	A		Top of even channel DAC reference ladder. Normally bypassed with a 0.1μF capacitor. An external DAC reference voltage may be applied to this pin.
55	$\overline{\text{RESET}}$	I	D	PU	Active-Low master reset. NC when function not being used. Please refer to “Power-On and Reset Timing Specifications” for further timing requirements.
56	MCLK	I	D		25MHz (nominal) master clock input.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog), (PU=Pull Up with an internal 10kΩ resistor), (PD=Pull Down with an internal 10KΩ resistor.).

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	4.2V
Voltage On Any Analog Input or Output Pin	-0.3V to 4.2V
Voltage On Any Digital Input or Output Pin	-0.3V to 4.2V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3	±50mA
Package Dissipation at T_A = 25°C (Note 4)	
ESD Susceptibility (Note 5)	
Human Body Model	3000V
Machine Model	300V
Soldering Temperature	
Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	-65°C to 150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	0°C≤T_A≤+70°C
All Supply Voltages	+2.7V to +3.6V
V IN Voltage Range	0.0V to AV+
Serial I/O Voltage Range	-0.05V to 3.6V

DC and Logic Level Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
Digital Input Characteristics						
VIH	Logical “1” Input Voltage	DV+ = 3.6V	**2.0**			V
VIL	Logical “0” Input Voltage	DV+ = 2.7V			**1.0**	V
IIH	Logical “1” Input Current	VIH = DV+		500		nA
IIL	Logical “0” Input Current	VIL = DGND		-100		nA
Digital Output Characteristics						
VOH	Logical “1” Output Voltage	DV+ = 3.6V, Iout = -0.5mA DV+ = 2.7V, Iout = -0.5mA	**2.5** **2.3**			V
VOL	Logical “0” Output Voltage	DV+ = 3.6V, Iout = 1.6mA DV+ = 2.7V, Iout = 1.6mA			**0.4** **0.4**	V
IOZ	Tri-State Output Current	Vout = DGND Vout = DV+		-100 100		nA
IOS	Output Short Circuit Current			60		mA
Power Supply Characteristics						
IA	Analog Supply Current	P_D = LOW, AV+ = 3.6V P_D = HIGH, AV+ = 3.0V		159.0 24.0		mA mA
ID	Digital Supply Current	P_D = LOW, AV+ = 3.6V P_D = HIGH, AV+ = 3.0V		12.7 1.3		mA mA
ID I/O	Digital Output Driver Supply Current	P_D = LOW, AV+ = 3.6V P_D = HIGH, AV+ = 3.0V		9.0 8.0		mA mA

Power Dissipation Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
PWR	Average Power Dissipation	AV+ = DV+ = DV+ I/O = 3.0V AV+ = DV+ = DV+ I/O = 3.3V AV+ = DV+ = DV+ I/O = 3.6V		414 510 652		mW

Input Sampling Circuit Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
V_{IN}	Input Voltage Level			1.5		V_{p-p}
I_{IN}	Input Leakage Current		**0**	500		nA
C_{IN}	Input Capacitance			5		pF
R_{IN}	Input Resistance			3000		kΩ
t_{AD}	Aperture Delay			2		ns
t_{SHD}	MCLK rising edge to SHD falling edge		**14**			ns

PGA Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
	Gain Resolution			8		Bits
	Step Size	(Gain / Resolution)		0.078		dB
	Maximum Gain			20.0		dB
	Minimum Gain			0.0		dB
	Temperature Drift Gain Error @ 25MHz	Deviation from best-fit line after end-point correction			±**3**	%
	Total Gain Error @ 25MHz	Deviation from best-fit line after end-point correction			±**5**	%

Offset DAC Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
	Resolution			±7		Bits
	Offset Adjustment Range	PGA Gain = 1.0		±100		mV
	DAC Step Size			0.78		mV/ LSB
	Temperature Drift Offset Error				±**3**	mV
					±**4**	LSB
Vrefp	Top of Reference Ladder			1.83		V
Vrefn	Bottom of Reference Ladder			1.71		V

Black Level Clamp Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
	Black Level Clamp Accuracy	PGA Gain = 0.0dB		±.5		LSB
		PGA Gain = 20.0dB		±.5		LSB
t_{BLKCLP}	Black Clamp Switch Pulse Width	# of pixels averaged + 1	5		33	T_{MCLK}
t_{CLPIN}	CLPIN Pulse Width		320			ns

Analog to Digital Converter Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
R_{REF}	Reference Ladder Resistance		750	950	1150	Ω
V_{REFT}	Top of Reference Ladder			2.46		V
V_{REFB}	Bottom of Reference Ladder			0.82		V
V_{REFT} - V_{REFB}	Differential Reference Voltage			1.64		V
	Overrange Output Code	$V_{IN} > V_{REFT}$		1023		
	Underrange Output Code	$V_{IN} < V_{REFB}$		0		

AC Electrical Characteristics

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
f_{MCLK}	Input Clock Frequency		1	25	27	MHz
T_{MCLK}	Input Clock Period		37	40	1000	ns
t_{ch}	Clock High Time	@ $MCLK_{max}$	15	17		ns
t_{cl}	Clock Low Time	@ $MCLK_{max}$	15	17		ns
	Clock Duty Cycle	@ $MCLK_{max}$		45/55		min/max
t_{rc}, t_{fc}	Clock Input Rise and Fall Time			3		ns
	Pipeline Delay (Latency)	Odd Channel		6		T_{MCLK}
		Even Channel		6.5		T_{MCLK}
t_{VALID}	Data valid time			16.4		ns
t_{OH}	Output Data Hold Time			7.0		ns
t_{OD}	Output Delay Time			11.0		ns

Full Channel Performance Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted.

Boldface limits apply for TA = T_{MIN} to T_{MAX}: all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
DNL	Differential Non-Linearity	@ f_{MCLK} = 25MHz		±0.7		LSB
		@ f_{MCLK} = 10MHz		±0.5		LSB
INL	Integral Non-Linearity	@ f_{MCLK} = 25MHz		±6.0		LSB
		@ f_{MCLK} = 10MHz		±3		LSB
NOISE	Noise Floor Level @ 0.0dB Gain	@ f_{MCLK} = 25MHz		-68		dB
		@ f_{MCLK} = 10MHz		-72		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

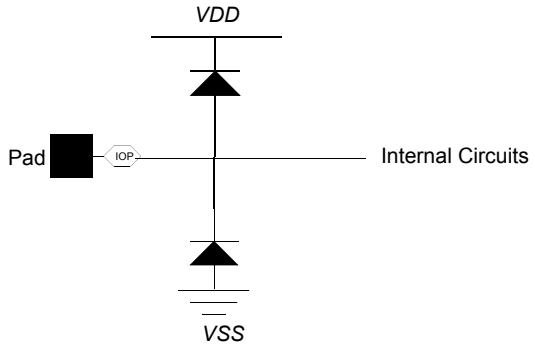
Note 3: When the voltage at any pin exceeds the power supplies (VIN < GND or VIN > AV+ or DV+), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.

Note 4: The absolute maximum junction temperature (TJmax) for this device is 150°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (*JA), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJmax - TA)/*JA. In the 56-pin TSSOP, *JA is 76.2°C/W, so PDMAX = 1,640mW at 25°C and 1,050mW at the maximum operating ambient temperature of 70°C. Note that the power dissipation of this device under normal operation will typically be about 510 mW. The values for maximum power dissipation listed above will be reached only when the LM98513 is operated in a severe fault condition.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

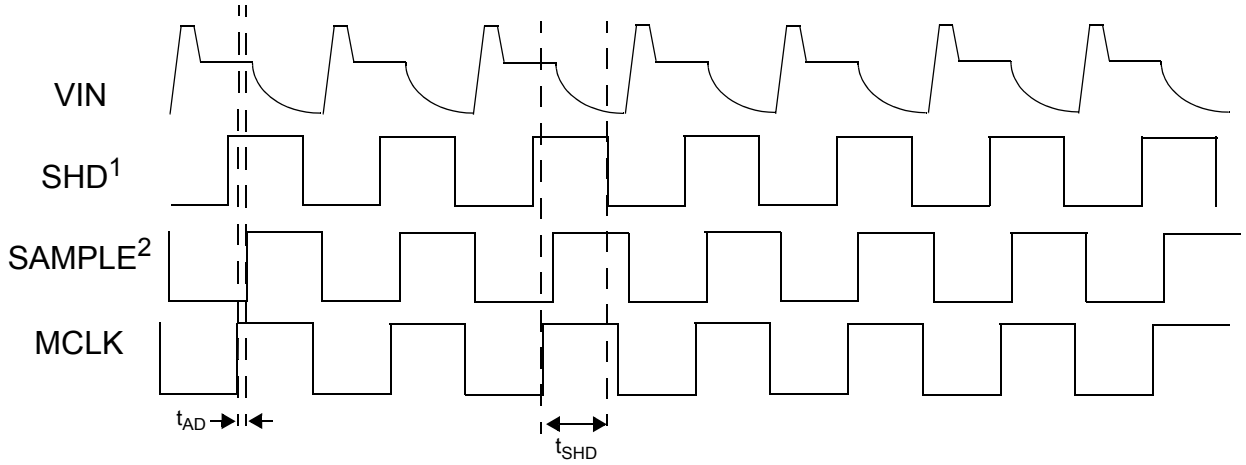
Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above AV+ and below AGND.



Note 8: Typical figures are at TJ = 25°C, and represent most likely parametric norms

Note 9: Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level)

Input Sampling Timing



[1]SHD may override the SAMPLE signal's falling (and rising) edge(s) for sampling the video signal (SHD is active-low by default).
[2]The SAMPLE signal is an internal signal derived from MCLK whose falling edge samples the CCD video signal by default.
[3]Timing shown above is for SHD polarity active-high (Bit [0] in Analog input control register = 1).

Figure 4: Input Sample Timing

Digital Output Timing

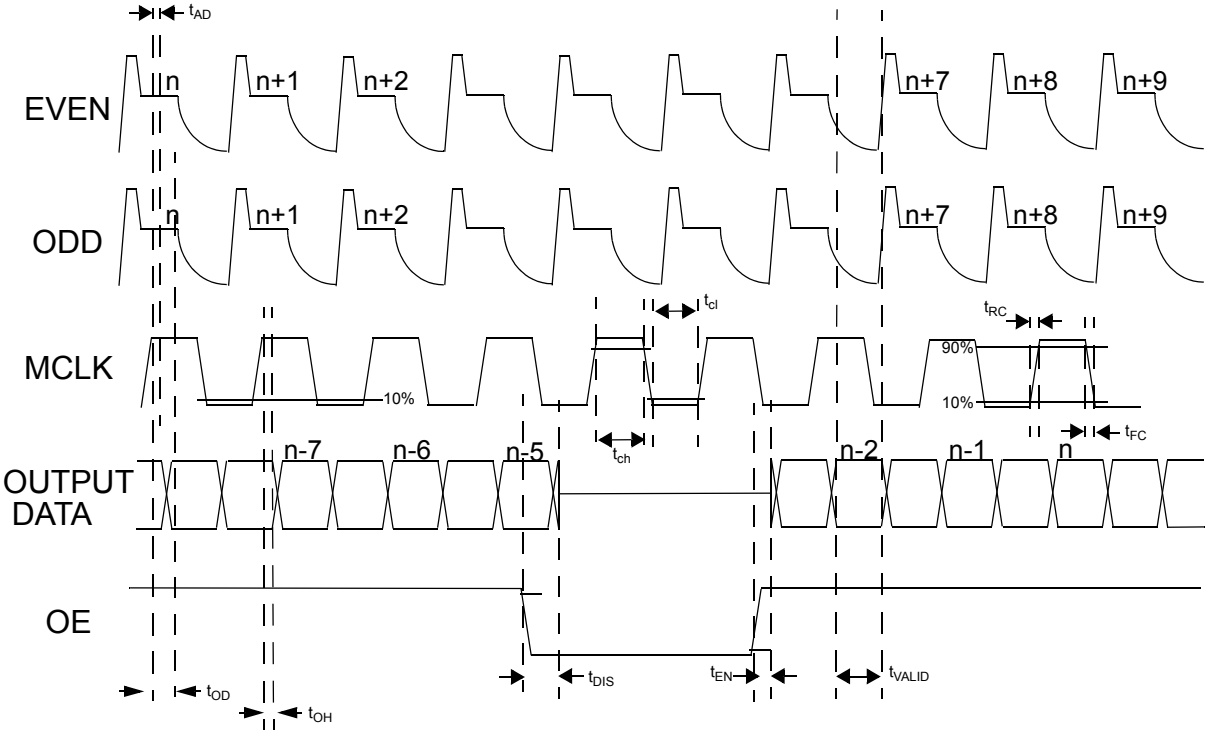


Figure 5: Digital Output Data Timing

Black Level Correction Timing

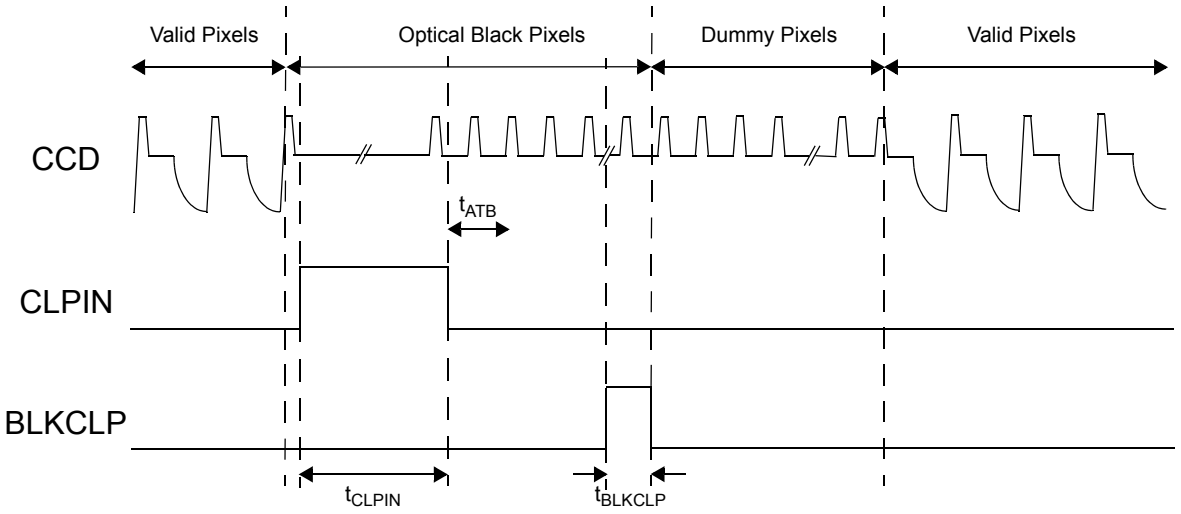


Figure 6: Black Level Correction Timing

System Overview

Introduction

The LM98513 is a 10-bit, dual-channel, complete analog-to-digital copier signal processor.The internal processing is carefully optimized to maintain high signal-to-noise ratio, and excellent dynamic performance. The system block diagram of the LM98513, shown in Figure 1 of the datasheet highlights the main features of the device: Two 25 MHz Sample/Hold amplifiers, 0-20dB digitally programmable gain amplifier (PGA), digital black level correction feedback loop containing an 8-bit DAC. The LM98513 also has input and backend clamps, and two 10-bit, 25MHz analog-to-digital converters with 50MHz digitally-multiplexed outputs.

Input Clamp

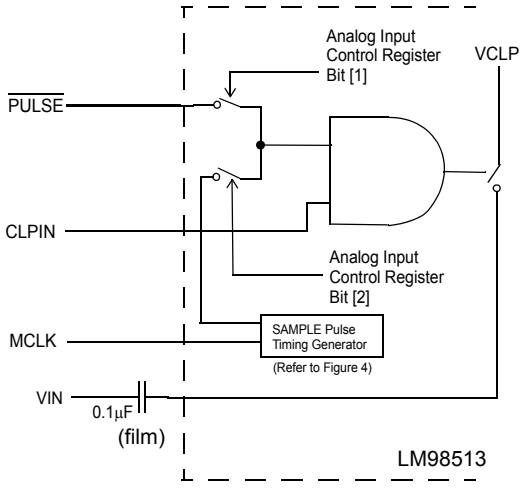


Figure 7: Input Bias Schematic

The input to the LM98513 should be AC coupled through a 0.1uF film capacitor. The DC bias of the input is set using the circuit of Figure 7. The CLPIN pulse is usually asserted during black pixels, as shown in Figure 6. Asserting CLPIN causes the input pin (Vin) to be shorted to the voltage VCLP, as shown in Figure 7. There are three modes available to control precisely where the CLPIN pulse will clamp the CCD waveform.These modes are selected by using the Analog Input Register, bits [1] & [2] which gate the CLPIN pulse by either an internal clock (Sample), or by a clock supplied by the user ($\overline{\text{PULSE}}$), as shown in Figure 8.

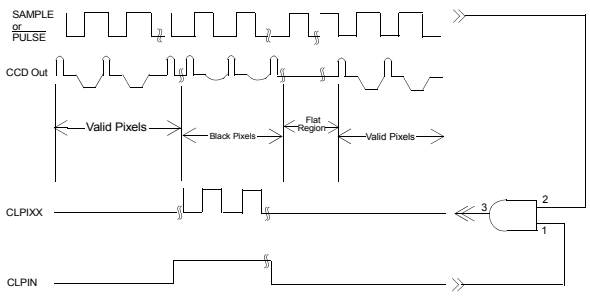


Figure 8: CLPIN gated by 'Sample' or $\overline{\text{Pulse}}$.

Sample and Hold

A typical CCD output waveform is shown in Figure 4. Also shown is the internally generated SAMPLE pulse. The SAMPLE pulse samples the 'signal' level of the CCD output waveform. The rising and falling edges of the SAMPLE pulse is set by the rising and falling edges of MCLK as shown in Figure 4.

The CCD output waveform samples are taken at the falling edges of the SAMPLE pulse. The falling edge of the SAMPLE can be adjusted by using the SHD input.

If the SHD input is used, it overrides the falling edge of the SAMPLE pulse, and the CCD output waveform samples are taken at the falling edges of SHD. The CCD output waveform samples can be taken on the rising edge of SHD if bit [0] of the analog input control register is set to 0.

The CCD output waveform samples are then compared to the voltage VCLP. Therefore, clamping the input Vin to the voltage VCLP, establishes the zero-signal level.

Programmable Gain Amplifier

The amplifier has a gain ranging from 0-20dB, and is "linear in dB" as shown in Figure 17. The PGA's gain setting is determined from an 8-bit word downloaded through the serial interface. Each channel has an independent gain amplifier to maintain gain balance.

System Overview (Continued)

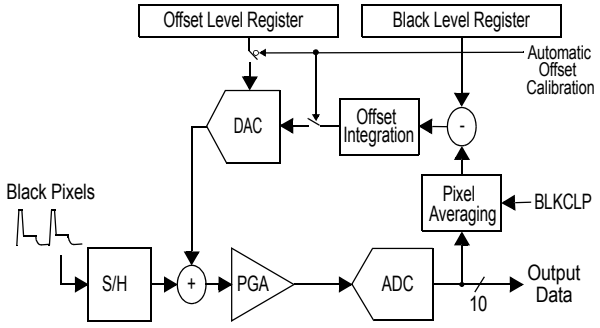


Figure 9: Digital Black Level Correction Loop

Black Level Correction

CCD signal processors require a reference level for the proper handling of input signals; this reference level is commonly referred to as the black level. The LM98513 is designed to determine a signal's black level during the CCD imager's optical black pixels.The LM98513 provides both an analog clamp and a digital black level correction loop as shown in Figure 9. The timing for these pulses is shown in Figure 6.

Black Level Clamp

Black level correction may be performed through one of two available methods: automatic or manual. In automatic mode, the black level is determined from the ADC output during black pixels by asserting the BLKCLP input of the LM98513 as shown in Figure 6. The ADC black level output value is then averaged over a programmed number of pixels and subtracted from the desired black level code stored in the output black level register. The result of the subtraction may then be integrated by a preset scaling factor, effectively smoothing any sharp transitions present in the black level signal, before the resulting calculated offset is finally applied to the input of the PGA as an offset level generated by the DAC. The offset integration scaling factor is stored in two bits of the black level clamp control register, and the values available range from full offset to offset divided-by-16. Use of the automatic mode involves enabling the black level offset auto-calibration bit in the black level clamp control register through the serial interface.The manual method is intended for use with processing systems where the desired black level correction loop is external to the LM98513. In this mode the external processor may store offset values in the offset level registers.

The BLKCLP pulse may be generated internally automatically by setting bit [1] of the Digital Black Level Correction Register to a "1". This is the default condition of the LM98513. The automatic BLKCLP pulse begins 10 MCLK periods after the falling edge of the CLPIN pulse and ends after the programmed number of pixels have been averaged.

Internal Timing Generation

The CCD sampling clock may be overridden by the user via the SHD clock input. As depicted in Figure 4 there is a signal generated internally for input sampling referred to as SAMPLE. This signal provides the rising edge reference for the sampling of the CCD input signal. The timing of the SAMPLE is derived from the clock; therefore, shifting the clock phasing with respect to the CCD input signal would also shift the rising and falling edges of SAMPLE. The actual sampling of the CCD's reference level and video signal is performed on the falling edge of the SAMPLE signal. The user may modify the position of the falling edges where the sampling of the CCD input occurs by driving SHD input of the LM98513. The falling edge of SHD will override the falling edge of SAMPLE and cause the duration of the sample pulse to shorten accordingly. As is evident in Figure 4 the falling edge of SHD should not occur earlier than t_{SHD} after the rising edge of MCLK.

VIN Test Option

The LM98513 may be placed into test mode for system debugging capability. When in test mode, the ODD and EVEN channel inputs are both internally connected to the VIN TEST input. Test mode is activated (and de-activated) via the serial interface.

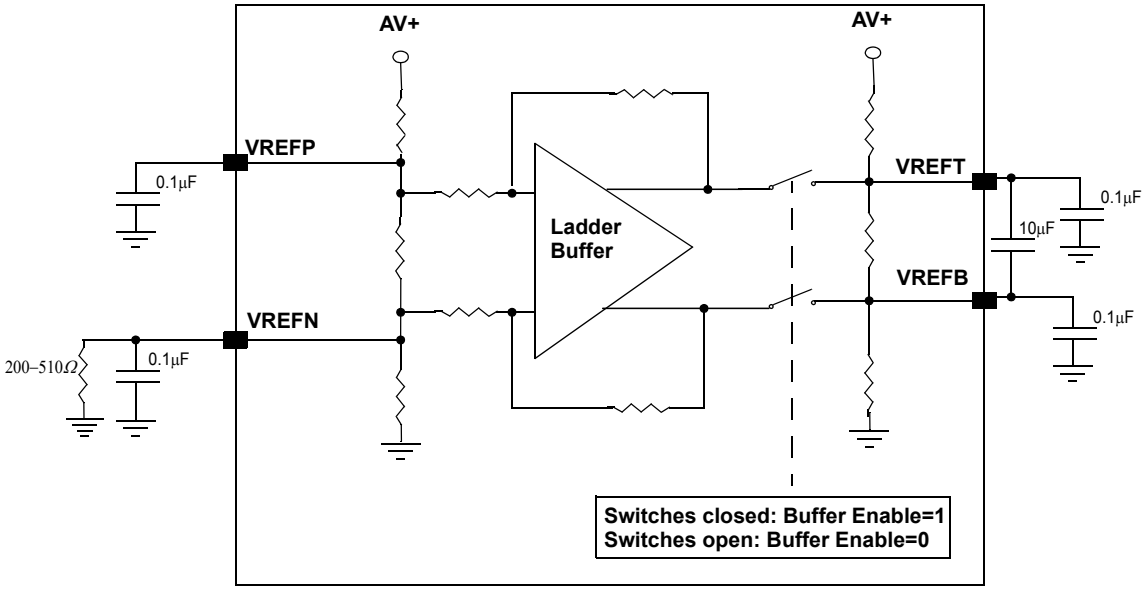


Figure 10: The ADC Ladder Buffer.

System Overview (Continued)

ADC Ladder Buffers

The top and bottom voltages of ADC reference ladder (VREFT & VREFB) define the analog input range. These reference voltages may experience a small amount of droop under certain operating conditions. For example, high operating frequencies or abrupt changes in input. An internal buffer is available to reduce this droop, if it occurs. The buffer is enabled by setting bit [1] of the Even/Odd Channel Software Control registers. (See Figure 10.)

Serial Interface and Configuration Registers

There are many options available to the user that may be programmed via the LM98513's serial interface. Configuration values are stored in registers for use by several functions such as programmable gain, offset, black level, and digital black level correction options. See "Register Memory Map" on page 15.

Upon power-up or external reset, the configuration registers will contain their respective default values. The master MCLK input is required to be running during serial interface commands. Each command entered through the serial interface must have a minimum of 15 bits (see Figure 14 and Figure 15). In addition, note that after a write command, the data written will be outputted during the next command (for verification). Likewise, a read command requires an additional command after issuing the read command to read back the data from the register.

Chip Enable

A chip enable function is provided for use in systems with multiple LM98513s attached to a common serial interface bus. The two chip enable pins (CE0 and CE1) should be driven either high or low during power-on or reset to indicate the device address. Subsequently, this address is included in the serial interface address as the two most significant bits (see Figure 14 and Figure 15).

Analog Output Option

The LM98513 supports the option of driving the differential analog output pins with analog signals normally internal to the device. For more information, see "Software Control Registers" on page 16.

Analog Level Offset

The offset level registers store the offset value that is required to meet the respective channel's black level requirements. These registers are read-only when automatic offset calibration is enabled. It should be noted that each offset DAC step (1 LSB) corresponds to a 0.5 LSB step at the ADC output. Therefore, if an offset of 20 digital codes is desired at the ADC output, a digital code value of 40 should be stored in the offset level register(s). As a result, the maximum offset seen at the ADC output as a result of digital code values stored in the offset level register(s) is ±64 codes. It is possible to increase the digital output range of the offset level DAC, resulting in an increased maximum ADC output code corresponding to a given DAC input. For more information on increasing the DAC range, please see "Offset Level DAC Range Adjustment" on page 21.

Output Black Level

The output black level register is an 8-bit word stored by the user that specifies the desired ADC output level corresponding to optical black. For example, a user who requires an ADC output level of 16 for black pixels would write this value into the register. Upon programming this register, assertion of the BLKCLP signal activates the digital black clamp loop and the black level is steered toward the value stored in the output black level register. The digital black clamp loop is only limited in it's range by the offset DAC's range (see "offset level DAC Range Adjustment on page 21").

Software Control

There is a software control register available for each channel accessible via the serial interface. The software control registers provide selections for internal referencing options and analog outputs for debugging purposes. Please refer to the register data descriptions for more information on the software control registers.

Power Level Control

The LM98513 is equipped with two power trim registers that may be used to adjust power levels of various circuits internal to the device. In its default condition, the LM98513 is set for optimum power and performance, and modifying the values stored in the power level control registers will affect performance as a result of the change in power level(s). In applications where maximum performance is desired, the default values should be used. Otherwise, power levels may be decreased at the slight expense of performance. Please refer to the register data descriptions for more information regarding the power level control registers.

Offset Integration

The clamping of the ADC output during optical black pixels can be controlled to slow down or damp changes in offset values calculated as a result of the digital black clamp loop. Each time the BLKCLP signal is activated the ADC output is compared to the desired value of black (See Black Pixel Averaging). If the output does not match the desired value during comparison, an error or deviation value results. The user has the option of integrating either all or a programmable fraction of this deviation into the previously calculated offset value. This has the effect of slowing down the offset convergence resulting in a calculation for offset that is less susceptible to noise.

Black Pixel Averaging

In order to obtain a snapshot of the current value for black (for comparison with the desired level of black) the ADC output is sampled upon activation of BLKCLP. Since a single optical black pixel is unlikely to be an accurate representation of the black level, a number of black pixels are averaged. The number of pixels to be averaged during optical black is another programmable parameter of the LM98513. The ability to select the number of pixels to be averaged provides greater flexibility allowing the LM98513 to be used with different CCDs having differing number of black pixels.

DAC Format

There are two available formats for the input to the offset DAC. The format is changed via the configuration bit in the digital black level clamp control register (Reg 0x05, bit[6])..

DAC	Default Format	Optional Format
00000000	-100mV	+/- 0mV
00000001	-99.2mV	+0.78mV
01111111	-0.78mV	+100mV
10000000	+/- 0mV	+/- 0mV
10000001	+0.78mV	-0.78mV
11111110	+99.2mV	-99.2mV
11111111	+100mV	-100mV

Figure 11: DAC Formats

Register Memory Map

Title	Address	Default Value
Even Channel PGA Gain	0000	0000 0000 (0d)
Odd Channel PGA Gain	0001	0000 0000 (0d)
Test	0010	n/a
Test	0011	n/a
Output Black Level	0100	0010 0000 (32d)
Digital Black Level Clamp Control	0101	X101 0011 (83d)
Analog Input Control	0110	XX00 0000 (0d)
Test	0111	n/a
Even Channel offset level	1000	1000 0000 (128d)
Odd Channel offset level	1001	1000 0000 (128d)
Even Channel Software Control	1010	XXX0 0000 (0d)
Odd Channel Software Control	1011	XXX0 0000 (0d)
Power Level Control 0	1100	1010 1010 (170d)
Power Level Control 1	1101	0101 1010 (90d)
Test	1110	n/a
Test	1111	n/a

Figure 12: Register Memory Map

Register Data

The following section describes all available registers in the LM98513 register bank and their functions.

PGA Gain Registers

Register Name **Even Channel PGA Gain**
Address **0 Hex**
Mnemonic **PGAEven**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB-20.0dB in 0.078dB steps.

Register Name **Odd Channel PGA Gain**
Address **1 Hex**
Mnemonic **PGAOdd**
Type **Read/Write**
Reset Value **0000 0000 Binary.**

Bit	Bit Symbol	Description
[7:0]	PGA Gain	0.0dB-20.0dB in 0.078dB steps.

Output Black Level Register

Register Name **Output Black Level**
Address **4 Hex**
Mnemonic **OBL**
Type: **Read/Write**
Reset Value **0010 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Black Level	0 - 256 output black level digital code value.

Digital Black Level Correction Register

Register Name **Digital Black Level Clamp Control**
Address **5 Hex**
Mnemonic **BLKCLP**
Type **Read/Write**
Reset Value **X101 0011 Binary**

Bit	Bit Symbol	Description
[6]	DAC Format	Alters the format of the DAC input registers. For more information, please see Figure 11.
[5:4]	Pixel Averaging	Black pixels averaged selection: **00 4 pixels averaged** **01 8 pixels averaged** **10 16 pixels averaged** **11 32 pixels averaged**
[3:2]	Offset Integration	Offset integration factor selection: **00 No Scaling** **01 Divide-by-2** **10 Divide-by-8** **11 Divide-by-16**
[1]	Auto BLKCLP Pulse Generation Enable	Enables automatic generation of the BLKCLP pulse required to initiate operation of the digital black level correction loop.
[0]	Offset Auto-Calibration Enable	Enables the digital black level correction loop. Offset level *registers are read-only when offset auto-calibration is enabled*.

Register Data (continued)

Analog Input Control Register

Register Name **Analog Input Control**
Address **6 Hex**
Mnemonic **AIC**
Type **Read/Write**
Reset Value **0000 0000 Binary**

Bit	Bit Symbol	Description
[4]	Test Mode Enable	Internally connects the VIN TEST pin to both the EVEN and ODD inputs.
[3]	Analog Power Down	Cuts power to the on-chip analog circuitry including the PGA and ADC.
[2:1]	CLPIN Mode Select	**00** CLPIN gated by $\overline{\text{PULSE}}$ **01** CLPIN (ungated) **10** Reserved **11**CLPIN gated by SAMPLE
[0]	SHD Polarity1 Select	Selection of the polarity of the SHD timing clock. **0 Active-Low** **1 Active-High**

Offset level Registers

Register Name **Even Channel offset level**
Address **8 Hex**
Mnemonic **A0E**
Type **Read/Write**
Reset Value **1000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Signed Offset Level	Digital representation of the offset level to be applied to the input of the PGA. Please see Figure 11 for details regarding the DAC input format.

Register Name **Odd Channel Offset Level**
Address **9 Hex**
Mnemonic **AOO**
Type **Read/Write**
Reset Value **1000 0000 Binary**

Bit	Bit Symbol	Description
[7:0]	Signed Offset Level	Digital representation of the offset level to be applied to the input of the PGA. Please see Figure 11 for details regarding the DAC input format.

Software Control Registers

Register Name **Even Channel Software Control**
Address **A Hex**
Mnemonic **SCE**
Type **Read/Write**
Reset Value **XXX0 0000 Binary**

Bit	Bit Symbol	Description
[4:3]	Analog Output Select	Routes the selected even channel internal analog signal to the differential analog output pins AOUT+ EVEN and AOUT- EVEN. **00 S/H Stage** **01 PGA Stage 1** **10 PGA Stage 2** **11 PGA Stage 3**
[2]	Analog Output Enable	Enables the differential analog output pins AOUT+ EVEN and AOUT- EVEN. Otherwise, the pins should not be connected.
[1]	ADC Reference Buffer Enable	Enables the ladder buffer for the ADC ladder references (VREFT & VREFB). **0 buffer disabled** **1 buffer enabled**
[0]	Set to "0"	**This bit must be set to "0" for proper reference voltages.**

Register Name **Odd Channel Software Control**
Address **B Hex**
Mnemonic **SCO**
Type **Read/Write**
Reset Value **XXX0 0000 Binary**

Bit	Bit Symbol	Description
[4:3]	Analog Output Select	Routes the selected odd channel internal analog signal to the differential analog output pins AOUT+ ODD and AOUT- ODD. **00 S/H Stage** **01 PGA Stage 1** **10 PGA Stage 2** **11 PGA Stage 3**
[2]	Analog Output Enable	Enables the differential analog output pins AOUT+ ODD and AOUT- ODD. Otherwise, the pins should not be connected.
[1]	ADC Ladder Buffer Enable	**0 ladder buffer disabled** **1 ladder buffer enabled**
[0]	Set to "0"	**This bit must be set to "0" for proper reference voltages.**

Register Data (continued)

Power Level Control Registers

Register Name **Power Level Control 0**
Address **C Hex**
Mnemonic **PLC0**
Type **Read/Write**
Reset Value **1010 1010 BinaryRegister NamePower**

[7:6]	PGA Stage 1 Amplifier Bias	Adjusts the power level of the PGA stage 1 amplifier. The power level is relative the value of the binary number stored.
[5:4]	PGA Common-Mode Input Bias	Adjusts the power level of the PGA common-mode input. The power level is relative the value of the binary number stored.
[3:2]	SH Amplifier Bias	Adjusts the power level of the SH amplifier. The power level is relative the value of the binary number stored.
[1:0]	SH Common-Mode Input Bias	Adjusts the power level of the SH common-mode input. The power level is relative the value of the binary number stored.

Level Control 1
Address **D Hex**
Mnemonic **PLC1**
Type **Read/Write**
Reset Value **0101 1010 Binary**

[7:6]	ADC Coarse Bank Bias	Adjusts the power level of the ADC coarse bank. The power level is relative the value of the binary number stored.
[5:4]	ADC Fine Bank Bias	Adjusts the power level of the ADC fine bank. The power level is relative the value of the binary number stored.
[3:2]	PGA Stage 3 Amplifier Bias	Adjusts the power level of the PGA stage 3 amplifier. The power level is relative the value of the binary number stored.
[1:0]	PGA Stage 2 Amplifier Bias	Adjusts the power level of the PGA stage 2 amplifier. The power level is relative the value of the binary number stored.

Serial Interface Timing Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
t_{MIN}	SCLK Period		36			ns
	SCLK Duty Cycle		40/60	50/50	60/40	%
	SCLK Rise / Fall Time				4	ns
t_{IH}	Input Hold Time		5			ns
t_{IS}	Input Setup Time		6			ns
t_{SENSC}	SCLK Start Time After $\overline{SEN}$ Low		10			ns
t_{SCSEN}	$\overline{SEN}$ Low after last SCLK Rising Edge		5			ns
t_{SENW}	$\overline{SEN}$ Pulse Width	MCLK must be active during serial interface commands.	2			T_{MCLK}
t_{DSEN}	Input Data to $\overline{SEN}$ Rising Edge		15			t_{MIN}
t_{OD}	Output Delay Time				15	ns

Serial Interface Timing Details

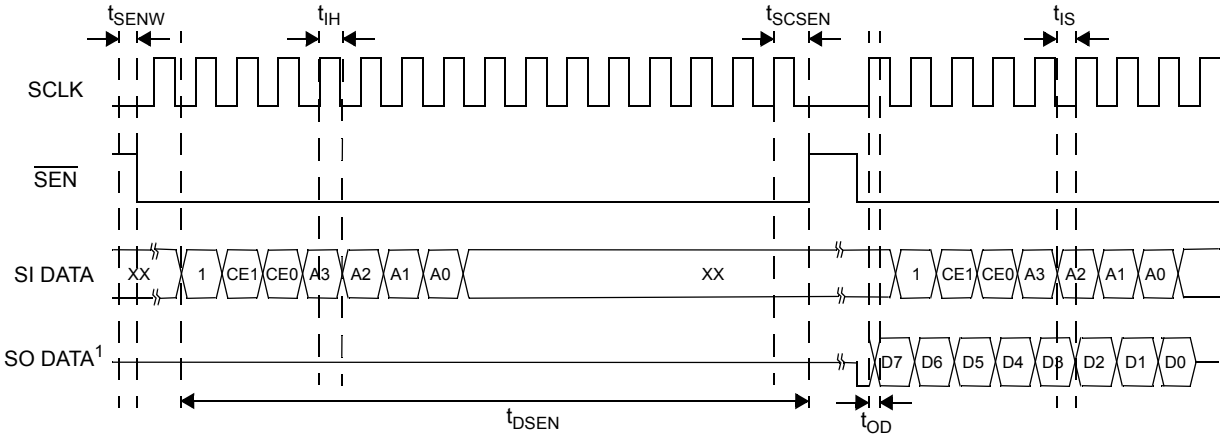


Figure 14: Serial Interface Read Command Timing

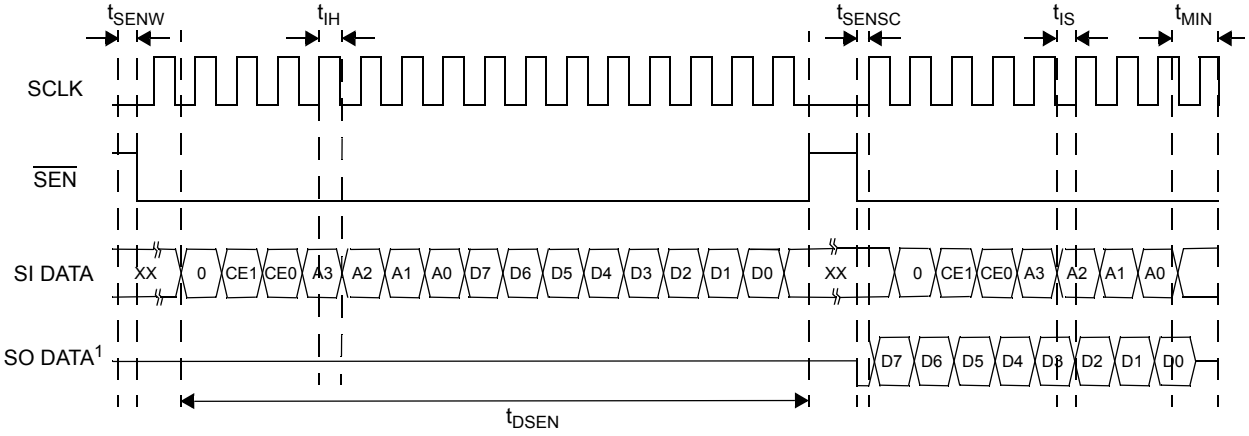


Figure 15: Serial Interface Write Command Timing

Serial Interface Read/Write Description

Writing to the serial registers

To write to the serial registers, the timing diagram shown in Figure 15 must be met. First $\overline{SEN}$ is toggled low. SI DATA may then be clocked in, and the data present on the rising edge of the serial clock is loaded in. The data continues to be clocked in, until $\overline{SEN}$ toggles high. The data present in the register is the last 15 bits of data sent before $\overline{SEN}$ toggled high. Therefore, for example, if 20 bits were sent when $\overline{SEN}$ was toggled low, the first 5 bits were discarded, and the data loaded are the remaining 15 bits. As seen in figure 15, these 15 bits are composed of 8 data bits, 4 address bits, 2 CE bits, and 1 read/write bit. When writing to the registers, the read/write bit must be low. When $\overline{SEN}$ toggles high, the register is written to, and the LM98513 now functions with this new data.

Reading the serial registers

To read the serial registers, the timing diagram shown in Figure 14 must be met.When $\overline{SEN}$ is toggled low, and data is loaded as described above in the writing sequence. When $\overline{SEN}$ toggles high, the new 15 bit word is considered, except this time the read/write bit should be a 1 indicating a read. The 8 data bits are not considered, but act only as place holders. When $\overline{SEN}$ toggles low again, the data that resides at the address considered in the previous read or write routine, begins clocking out SO DATA. The data streams out MSB-LSB as shown in Figure 14. Whether a read or a write was invoked in the previous sequence, the SO DATA will clock out the contents of the address considered in the previous sequence.

Power-On and Reset Timing Specifications

The following specifications apply for AV+ = DV+ = DV+ I/O = 3.3V, C_L = 10pF, and f_{MCLK} = 25MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
t_{POR}	Power-On or Reset Time	Device settling time after power-on or reset pulse			270	ns
t_{PORS}	Power-On or Reset Data Setup Time	Setup time during power-on or reset settling where data must be valid	5			ns
t_{PORH}	Power-On or Reset Data Hold Time	Hold time after power-on or reset settling where data must be valid			0	ns

Power-On and Reset Timing Details

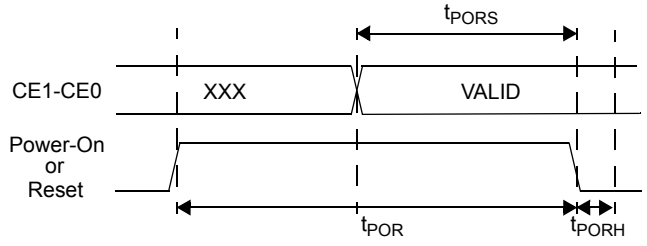


Figure 16: Power-On or Reset Timing

PGA Gain Plots

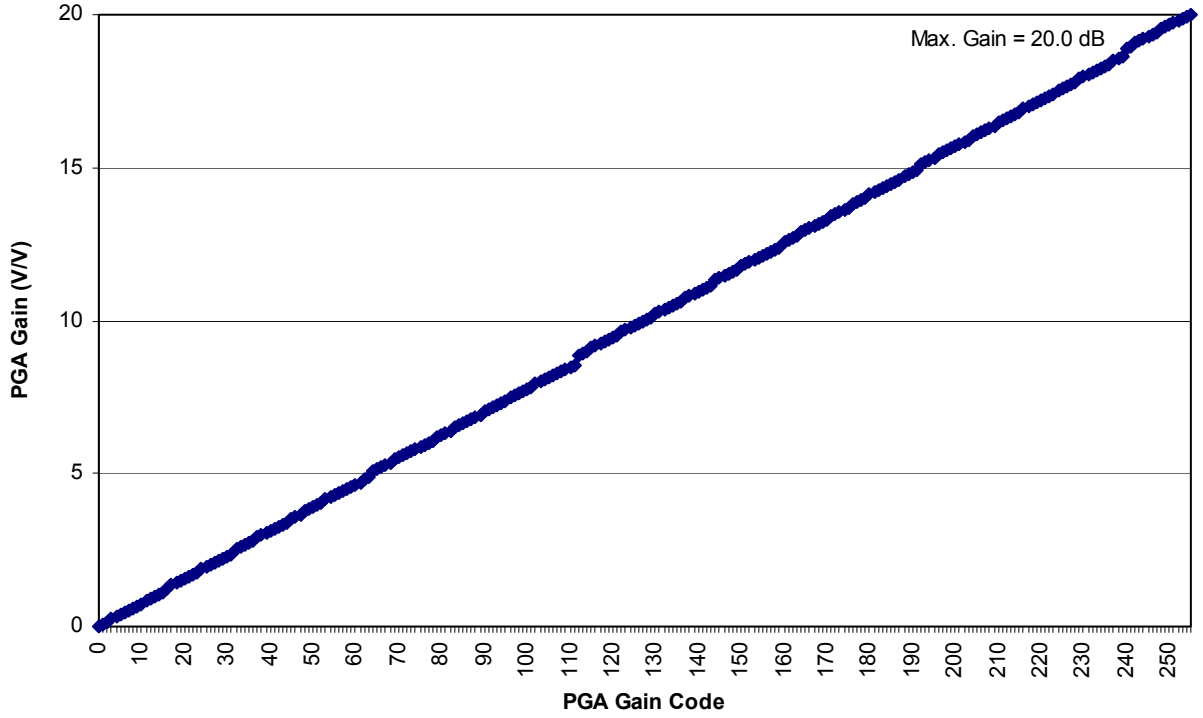


Figure 17: PGA Gain (Linear Scale) vs. PGA Gain Code

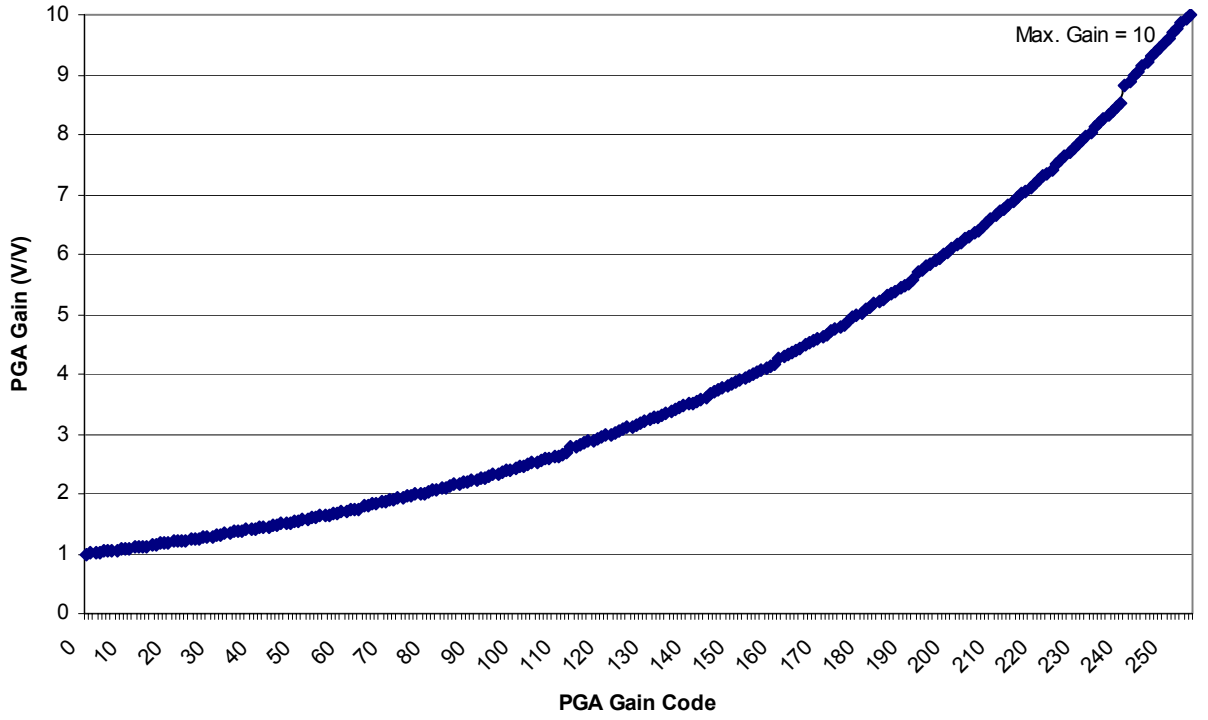


Figure 18: PGA Gain (Logarithmic Scale) vs. PGA Gain Code

Applications Information

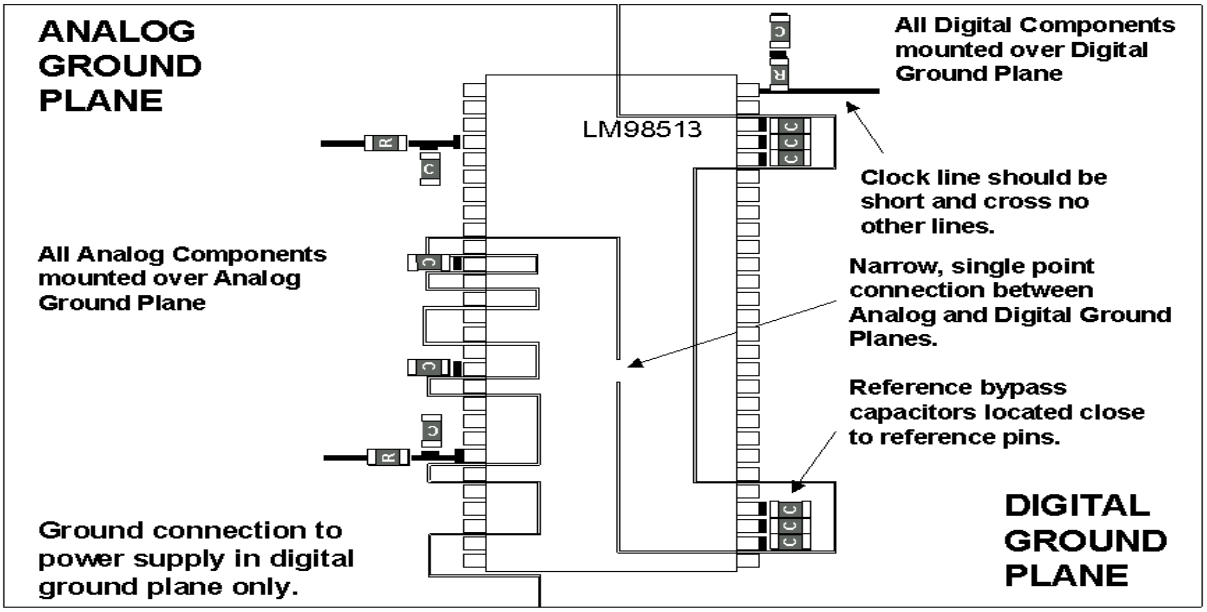


Figure 19: Recommended Layout Pattern

Analog-to-Digital Converter Reference Bypassing

The Analog-to-Digital Converter compares the analog output voltage from the PGA to a series of reference voltages developed along an internal reference ladder. The impedance of this reference ladder is 1000 Ohms. The voltage at the top and bottom of this ladder are set by internal resistors connected between the ladder and the positive and negative supplies, as shown in Figure 19. The top and bottom of the ladder are available to the user via pins 11,17,32,52. These pins can be driven by an external reference buffer. If driven, the top reference voltage (VREFT) should be kept in the range of 2.0 - 2.5V and the bottom reference voltage (VREFB) should be kept in the range of 0.5 - 1.0V. Whether externally driven, or biased internally, these pins should be decoupled to ground through 0.1uF capacitors. When biases internally, an additional bypass capacitor of 10uF should be used between the VREFT and VREFB pins, as shown in Figure 19. Any device used to drive the reference pins should be able to source adequate current into the VREFT pin, and sink adequate current from the VREFB pin, when the resistor ladder is at its minimum resistivity of 750 ohms.

The voltage difference between the top of the ladder (VREFT) and the bottom of the ladder (VREFB) may be as low as 1.0V or as high as 2.0V. However, the performance of the part under voltage differences greater than or less than the default voltage reference difference of 1.7V cannot be guaranteed.

Offset Level DAC Reference Bypassing

The offset level DAC reference pins, VREFP and VREFN, should be capacitively bypassed in the same fashion as the ADC reference pins VREFT and VREFB (see ”Analog-to-Digital Converter Reference Bypassing”).

Offset Level DAC Range Adjustment

The offset level DAC has an input range of ±127 LSB (see Figure 11). This offset level corresponds to 0.5 LSB at the ADC output per DAC input code step. Therefore, the offset DAC is limited to providing offset values less than or equal to ±64 LSB at the ADC output. In some applications, this range of output may not be sufficient. It is possible to increase the range of the DAC by adjusting the DAC reference range. The DAC reference range may be adjusted by lowering the voltage at the DAC lower reference pin, VREFN. It is recommended to use a pull-down resistor from VREFN to AGND to lower the voltage at VREFN. A resistor value of 200-510Ω will increase the DAC range by a factor of 2x, allowing offsets of ±127 LSB to be applied at the ADC output rather than the default maximum and minimum offsets of ±64 LSB.

Power Supply Considerations

The LM98513 may draw a sufficient amount of current to corrupt improperly bypassed power supplies. A 10μF to 50μF capacitor should be placed within 1cm of the analog power (AV+) pins of the device in parallel with a 0.1μF ceramic chip capacitor placed as close to the device as layout permits. Leadless chip capacitors are preferred because they have a low lead inductance. As is the case with virtually all high-speed semiconductors, the LM98513 should be assumed to have little power supply rejection; therefore, a noise-free analog power source is required.

The analog and digital power supplies of the LM98513 should be sourced from the same supply voltage, but the supply pins should be well isolated from one another. Isolating the supplies prevents digital noise from coupling back into the analog supply pins. A choke (ferrite bead) is recommended to be placed between the analog and digital power supply pins as well as a ceramic chip capacitor placed as close as possible to the analog supply pin(s) of the device. Additionally, it is not recommended that the LM98513’s digital supply be used for any other digital circuitry on the circuit board. All other digital devices should be powered from a separate digital supply well isolated from both the analog and digital supplies of the LM98513.

APPLICATIONS INFORMATION (Continued)

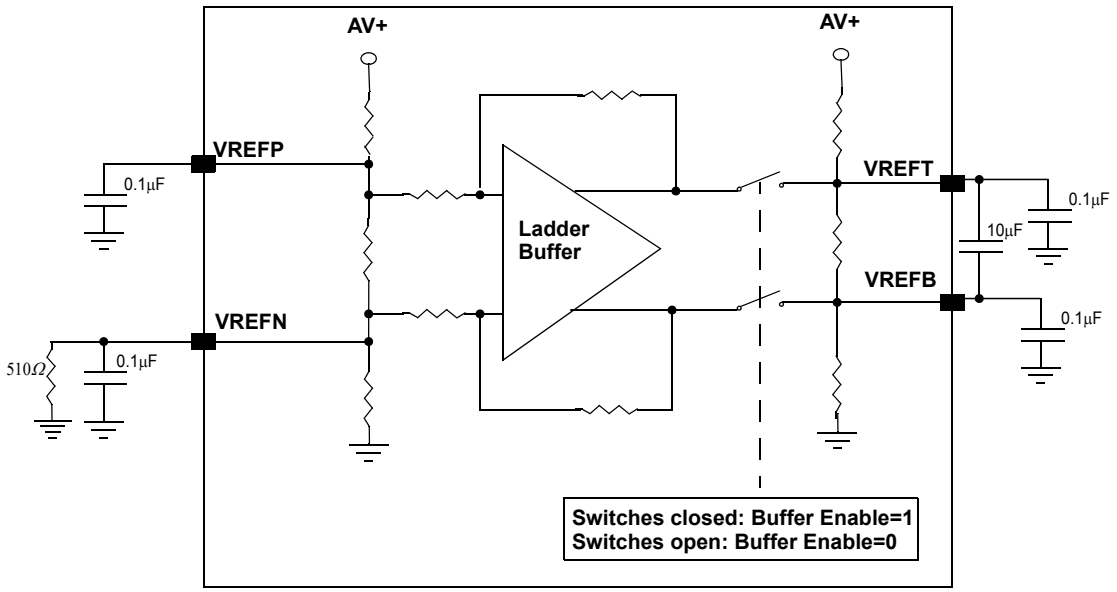


Figure 20: ADC, DAC Reference Bypassing and internal ADC Ladder Buffer

The LM98513 Clock

Although the LM98513 is tested and its performance guaranteed with a 25MHz clock, it typically will function with clock frequencies ranging from 1MHz to 30MHz. Performance is best if the clock rise and fall times are less than 3ns and the clock trace is terminated near the clock input pin with a series RC network consisting of a 100Ω resistor and a 47pF capacitor.

Layout and Grounding Techniques

The proper routing of all signals and relevant grounding techniques are essential to ensure the best signal-to-noise ratio and dynamic performance possible. Separate analog and digital ground planes ease meeting the datasheet limits. The analog ground plane should be low impedance and free from noise of other components of the system. All bypass capacitors should be located as close to the pin as possible and connected to the appropriate ground plane with short traces (<1cm). The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input.

Figure 20 provides an example of a suitable layout, including power supply routing, ground place separation, and bypass capacitor placement. All input amplifiers, filters, and reference components should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be placed over and grounded via to the digital ground plane. Digital and analog signal lines should never run parallel to each other in close proximity with each other. These signals should only cross when absolutely necessary and then only at 90° angles.

Dynamic Performance

The LM98513 is AC tested and its dynamic performance is guaranteed. The clock source driving the MCLK input must be free of jitter. For best AC performance, the clock source should be isolated from other system digital circuitry with a clock tree buffer(s). Meeting noise specifications depends largely upon keeping digital noise out of the analog input of the LM98513.

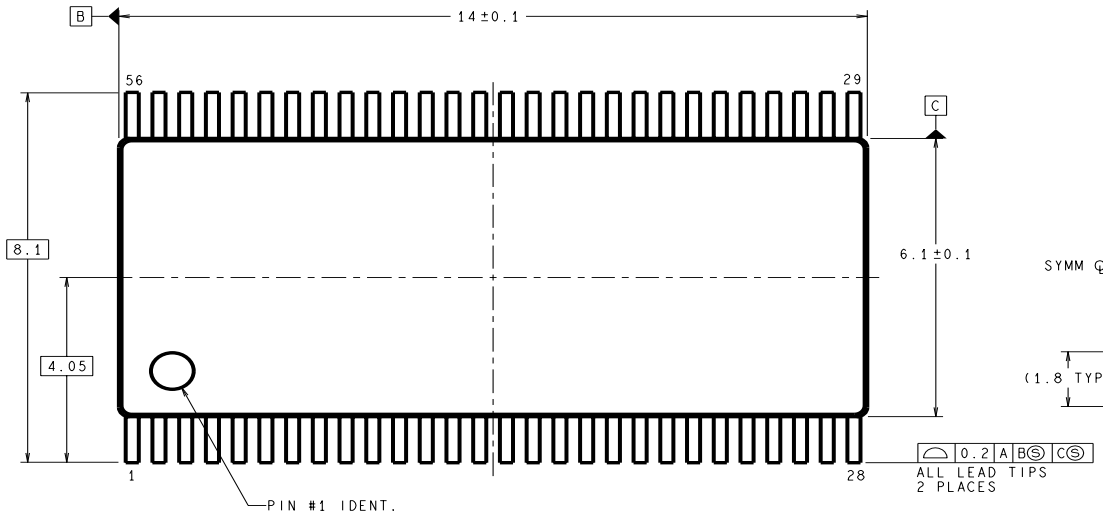
Common Application Pitfalls

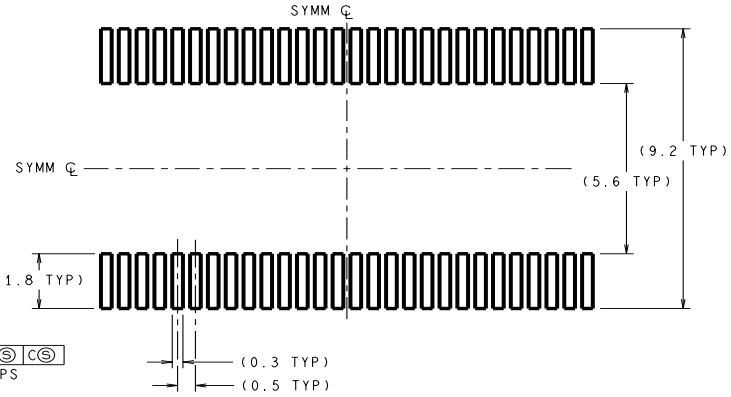
Driving the inputs (analog or digital) beyond the power supply potential. For proper operation, all input potentials should not be greater than 300mV above that of the power supply. It is not uncommon for high speed digital circuits (e.g. 74F and 74AC devices) to exhibit undershoot that falls to a potential greater than 1.0 Volt below the ground potential and overshoot that rises to a potential greater than 1.0 Volt above the power supply potential. A series resistor of 50Ω to 100Ω in the digital signal will, in most cases, eliminate this problem.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers have to charge for each conversion output, the more instantaneous digital current is required from the DV+ I/O and DGND I/O supply pins. These large charging current spikes can couple into the analog section and subsequently may degrade dynamic performance of the system. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem on the application system board. Buffering the digital data outputs may be necessary if the data bus being driven by the LM98513 is heavily loaded. Dynamic performance may also be improved by adding series resistors of 47Ω at each digital output.

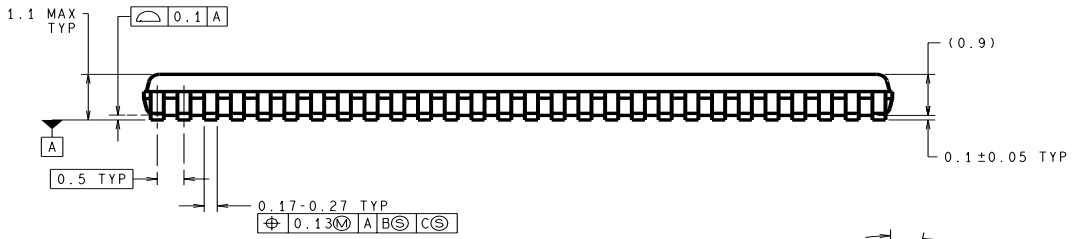
Driving the reference pins with devices that cannot source or sink the current required by the reference resistor ladder. As mentioned previously, any devices driving the reference resistor ladder must source sufficient current into the top of the ladder. Additionally, the device connected to the bottom of the ladder must be able to sink the necessary amount of current to keep the reference voltage(s) stable. If the reference resistor ladder voltages are not stable the converter output will not generate predictable output codes.

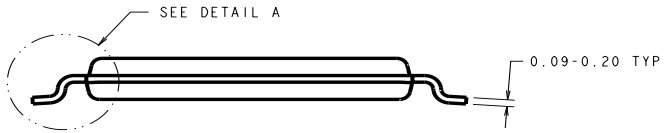
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
B	REDRAW ON PRO/E, ADD LAND PATTERN RECOMENDATION.	11323	02/16/96	MS/



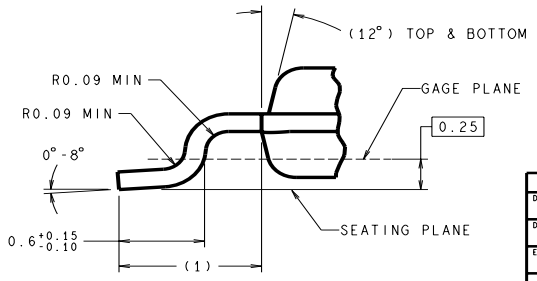


LAND PATTERN RECOMENDATION





DIMENSIONS ARE IN MILLIMETERS



DETAIL A
TYPICAL, SCALE: 40X

NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MO-153, VARIATION EE, DATED FEB, 1995.

APPROVALS	DATE
DRAWN MARTA SUCHY	02/16/96
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr., Santa Clara, CA 95052-8090

MOLDED TSSOP, JEDEC, 6.1mm BODY WIDTH, 56 LD, 0.50mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-MTD56	B

DO NOT SCALE DRAWING | SHEET 1 of 1

LM98513

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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