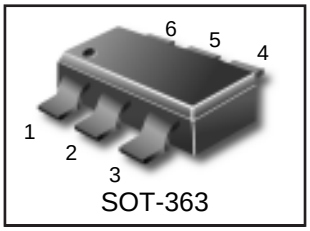
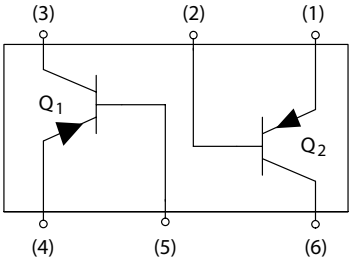
Dual Bias Resistor Transistors
PNP Silicon

LMBT3906DW1T1G

S-LMBT3906DW1T1G

The LMBT3906DW1T1G device is a spin–off of our popular SOT–23/SOT–323 three–leaded device. It is designed for general purpose amplifier applications and is housed in the SOT–363 six–leaded surface mount package. By putting two discrete devices in one package , this device is ideal for low–power surface mount applications where board space is at a premium.





●FEATURES

1）hFE, 100–300
2）Low VCE(sat), ≦0.4 V
3）Simplifies Circuit Design
4）Reduces Board Space
5）Reduces Component Count
6）We declare that the material of product compliant with RoHS requirements and Halogen Free.
7）S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

●DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LMBT3906DW1T1G	A2	3000/Tape&Reel
LMBT3906DW1T3G	A2	10000/Tape&Reel

●MAXIMUM RATINGS(Ta = 25℃)

Parameter	Symbol	Limits	Unit
Collector–Emitter Voltage	V_{CEO}	–40	Vdc
Collector–Base Voltage	V_{CBO}	–40	Vdc
Emitter–Base Voltage	V_{EBO}	–5	Vdc
Collector Current — Continuous	I_C	–200	mAdc

●THERMAL CHARACTERISTICS

Total Device Dissipation, (Note 1) @ T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction–to–Ambient	$R_{\Theta JA}$	833	℃/W
Junction and Storage temperature	T_J,T_{stg}	−55～+150	℃

1. Device mounted on FR4 glass epoxy printed circuit board using the minimum recommended footprint.

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●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

OFF CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector–Emitter Breakdown Voltage (Ic = –1.0 mAdc, I B = 0)	V(BR)CEO	–40	–	–	V
Collector–Base Breakdown Voltage (I C = –10 μAdc, I E = 0)	V(BR)CBO	–40	–	–	V
Emitter–Base Breakdown Voltage (I E = –10 μAdc, I C = 0)	V(BR)EBO	–5	–	–	V
Collector Cutoff Current (V CE = –30 Vdc, V EB =– 3.0Vdc)	ICEX	–	–	–50	nA
Base Cutoff Current (V CE = –30 Vdc, V EB = –3.0Vdc)	IBL	–	–	–50	nA

ON CHARACTERISTICS (Note 1.)

DC Current Gain	hFE				
(I C = –0.1 mAdc, V CE = –1.0 Vdc)		60	–	–	
(I C = –1.0 mAdc, V CE = –1.0 Vdc)		80	–	–	
(I C = –10 mAdc, V CE = –1.0 Vdc)		100	–	300	
(I C = –50 mAdc, V CE =– 1.0 Vdc)		60	–	–	
(I C = –100 mAdc, V CE =– 1.0 Vdc)		30	–	–	
Collector–Emitter Saturation Voltage(3)	VCE(sat)				V
(I C = –10 mAdc, I B = –1.0 mAdc)		–	–	–0.25	
(I C = –50mAdc, I B =– 5.0 mAdc)		–	–	–0.4	
Base–Emitter Saturation Voltage	VBE(sat)				V
(I C = –10 mAdc, I B = –1.0 mAdc)		–0.65	–	–0.85	
(I C = –50mAdc, I B =– 5.0 mAdc)		–	–	–0.95	

SMALL–SIGNAL CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Current–Gain — Bandwidth Product (I C = –10mAdc, V CE= –20Vdc, f = 100MHz)	fT	250	–	–	MHz
Output Capacitance (V CB = –5.0 Vdc, I E = 0, f = 1.0 MHz)	Cobo	–	–	4.5	pF
Input Capacitance (V EB = –0.5 Vdc, I C = 0, f = 1.0 MHz)	Cibo	–	–	10	pF
Input Impedance (V CE=– 10 Vdc, I C = –1.0 mAdc, f = 1.0 kHz)	hie	2	–	12	k Ω
Voltage Feedback Ratio (V CE= –10 Vdc, I C = –1.0 mAdc, f = 1.0 kHz)	hre	0.1	–	10	X 10^{-4}
Small–Signal Current Gain (V CE=–10 Vdc, I C =– 1.0 mAdc, f = 1.0 kHz)	hfe	100	–	400	
Output Admittance (V CE=–10 Vdc, I C =–1.0 mAdc, f = 1.0 kHz)	hoe	3	–	60	μmhos
Noise Figure (VCE=–5V, IC=–100μA, RS=1.0kΩ , f =1.0kHz)	NF	–	–	4	dB

3. Pulse Test: Pulse Width <300 μs, Duty Cycle <2.0%.

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●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

SWITCHING CHARACTERISTICS

Delay Time	(V_{CC} = –3.0 Vdc, V_{BE}= 0.5 Vdc,I_C = –10 mAdc, I_{B1} =– 1.0 mAdc)	t_d	–	–	35	ns
Rise Time		t_r	–	–	35	
Storage Time	(V_{CC} =– 3.0 Vdc, I_C = –10 mAdc,I_{B1} = I_{B2} = –1.0 mAdc)	t_s	–	–	225	
Fall Time		t_f	–	–	75	

Electrical Characteristics Curves

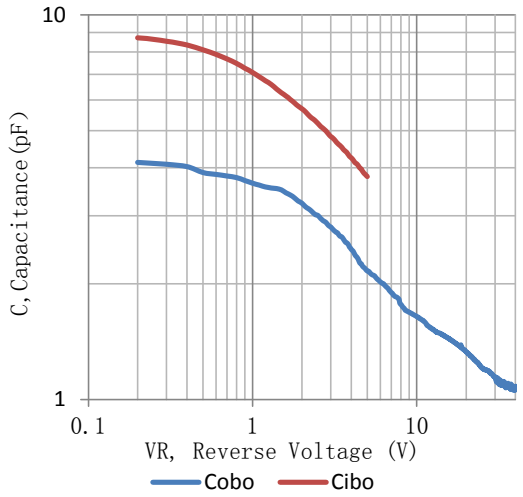

Figure 1. Capacitance

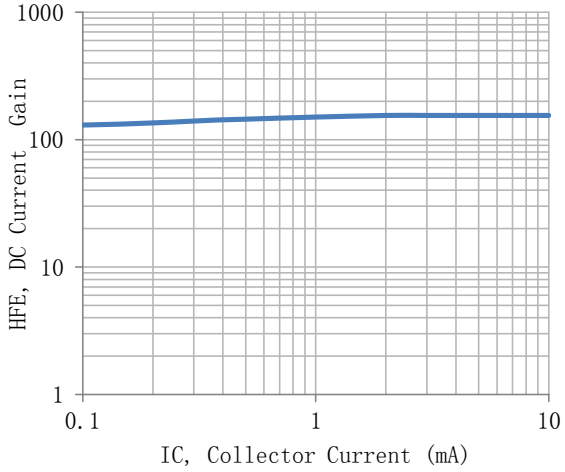

Figure 2. Current Gain

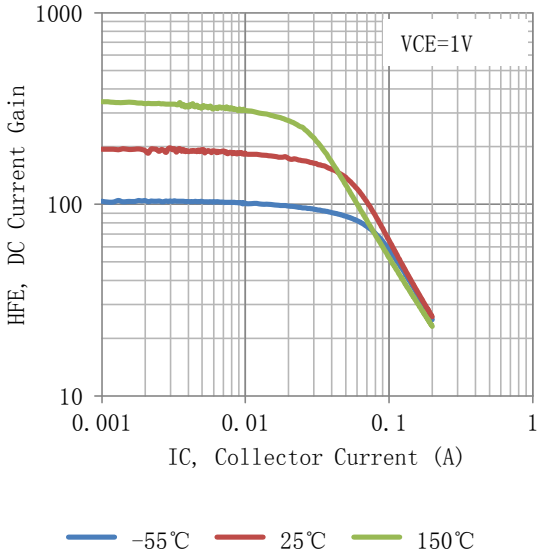

Figure 3. DC Current Gain

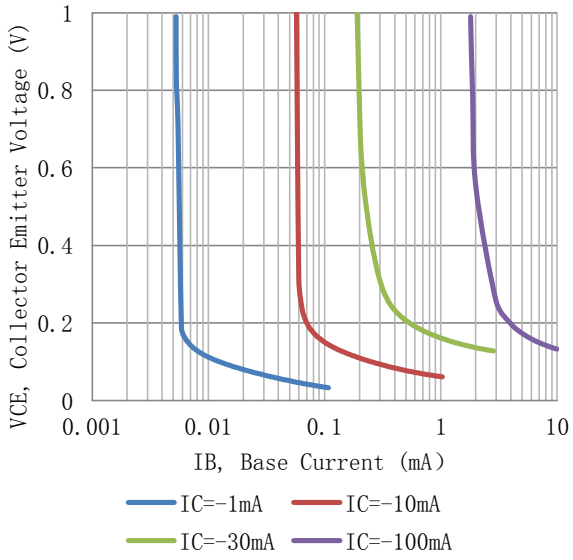

Figure 4. Collector Saturation Region

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Electrical Characteristics Curves

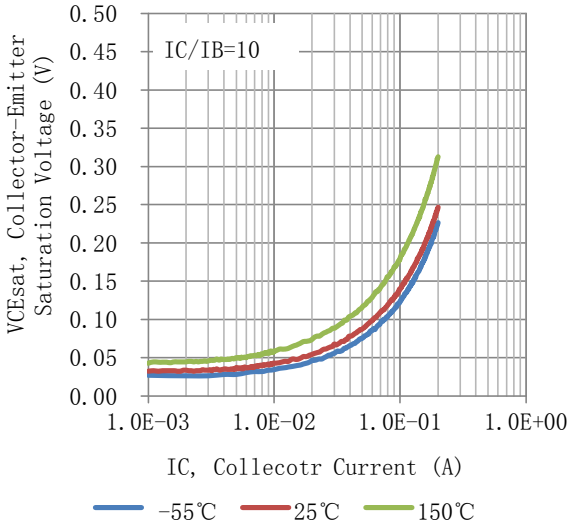

Figure 5. Collector Emitter Saturation Voltage vs. Collector Current

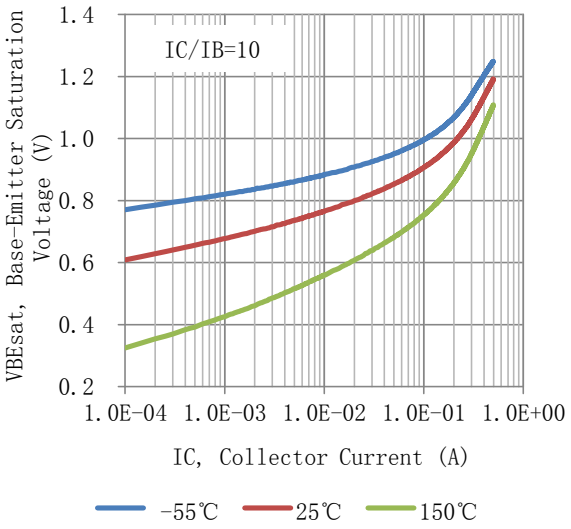

Figure 6. Base Emitter Saturation Voltage vs. Collector Current

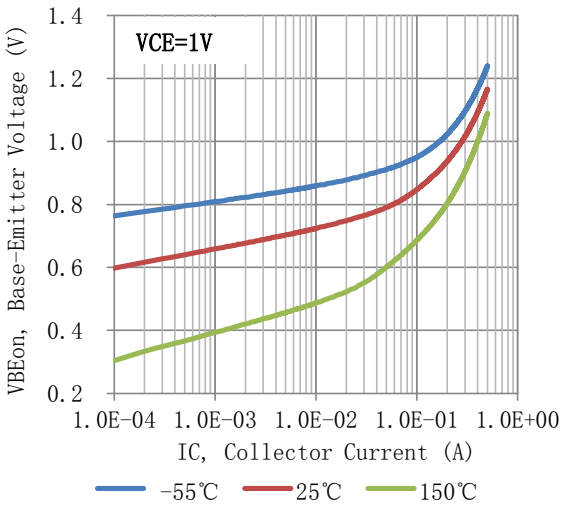

Figure 7. Base Emitter Voltage vs. Collector Current

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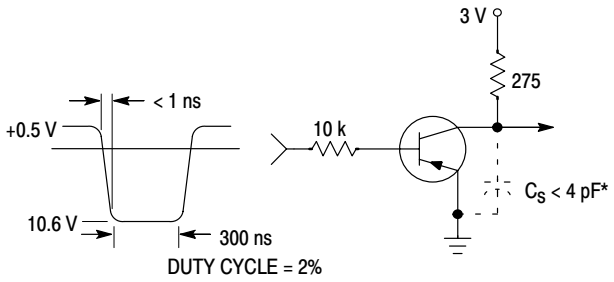

Figure 8. Delay and Rise Time Equivalent Test

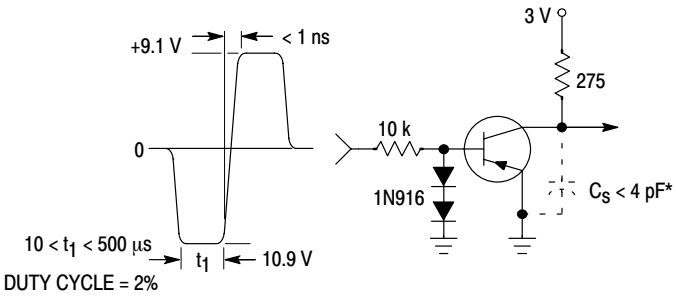

Figure 9. Storage and Fall Time Equivalent Test

* Total shunt capacitance of test jig and connectors

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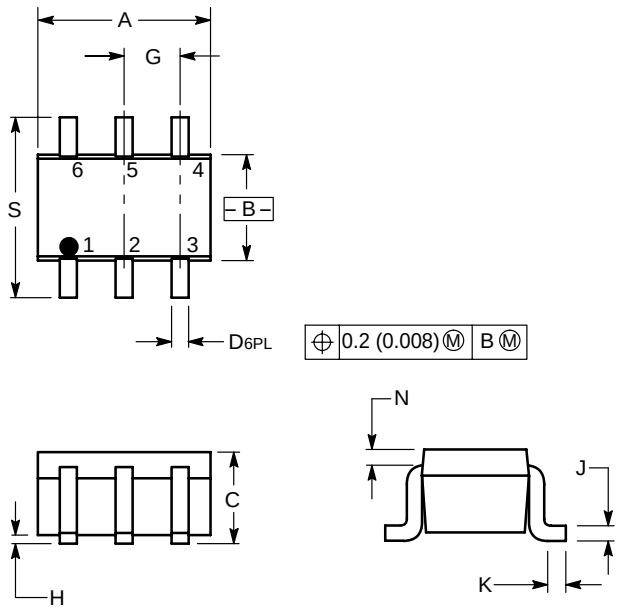

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2