LMC6462 Dual/LMC6464 Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

Check for Samples: LMC6462, LMC6464

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Ultra Low Supply Current 20 µA/Amplifier**
- **Ensured Characteristics at 3V and 5V**
- **Rail-to-Rail Input Common-Mode Voltage Range**
- **Rail-to-Rail Output Swing**
  - **(within 10 mV of rail, V_S = 5V and R_L = 25 kΩ)**
- **Low Input Current 150 fA**
- **Low Input Offset Voltage 0.25 mV**

APPLICATIONS

- **Battery Operated Circuits**
- **Transducer Interface Circuits**
- **Portable Communication Devices**
- **Medical Applications**
- **Battery Monitoring**

DESCRIPTION

The LMC6462/4 is a micropower version of the popular LMC6482/4, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6462/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, ensured for loads down to 25 kΩ, assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6462/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6462/4, with ensured specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60 µW per amplifier (at V_S = 3V) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.

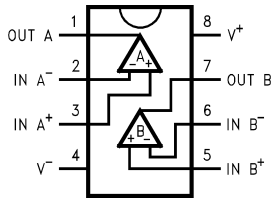


Figure 1. 8-Pin PDIP/SOIC – Top View (See Package Number P or D)

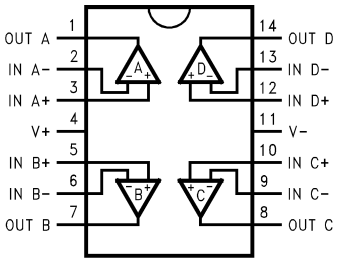


Figure 2. 14-Pin PDIP/SOIC – Top View (See Package Number NFF0014A or D)

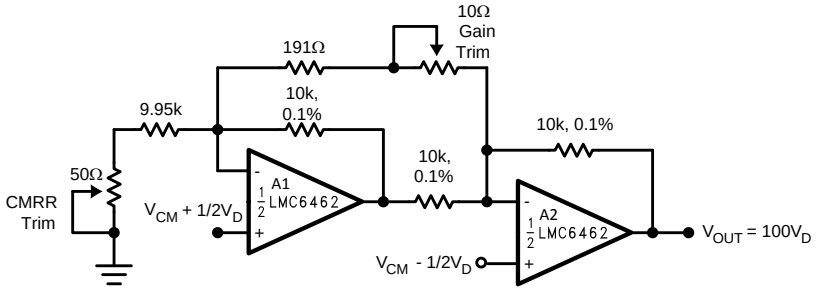


Figure 3. Low-Power Two-Op-Amp Instrumentation Amplifier

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

ESD Tolerance(4)	2.0 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin(5)	±5 mA
Current at Output Pin(6)(7)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature(8)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) For specified Military Temperature Range parameters see RETSMC6462/4X.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.
(5) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(6) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(7) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(8) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings

Supply Voltage		$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	LMC6462AM, LMC6464AM	$-55°C \le T_J \le +125°C$
	LMC6462AI, LMC6464AI	$-40°C \le T_J \le +85°C$
	LMC6462BI, LMC6464BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	P Package, 8-Pin PDIP	115°C/W
	D Package, 8-Pin SOIC	193°C/W
	NFF Package, 14-Pin PDIP	81°C/W
	D Package, 14-Pin SOIC	126°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC6462AI LMC6464AI Limit(2)	LMC6462BI LMC6464BI Limit(2)	LMC6462AM LMC6464AM Limit(2)	Units
V_{OS}	Input Offset Voltage		0.25	0.5 **1.2**	3.0 **3.7**	0.5 **1.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.5				µV/°C
I_B	Input Current	See(3)	0.15	**10**	**10**	**200**	pA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ[1]	LMC6462AI LMC6464AI Limit[2]	LMC6462BI LMC6464BI Limit[2]	LMC6462AM LMC6464AM Limit[2]	Units
I_{OS}	Input Offset Current	See[3]		0.075	**5**	**5**	**100**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 15.0V, V^+ = 15V		85	70 **67**	65 **62**	70 **65**	dB min
		0V ≤ V_{CM} ≤ 5.0V V^+ = 5V		85	70 **67**	65 **62**	70 **65**	
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V, V^- = 0V, V_O = 2.5V		85	70 **67**	65 **62**	70 **65**	dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤ −15V, V^+ = 0V, V_O = −2.5V		85	70 **67**	65 **62**	70 **65**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB		−0.2	−0.10 **0.00**	−0.10 **0.00**	−0.10 **0.00**	V max
				5.30	5.25 **5.00**	5.25 **5.00**	5.25 **5.00**	V min
		V^+ = 15V For CMRR ≥ 50 dB		−0.2	−0.15 **0.00**	−0.15 **0.00**	−0.15 **0.00**	V max
				15.30	15.25 **15.00**	15.25 **15.00**	15.25 **15.00**	V min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ[4]	Sourcing	3000				V/mV min
			Sinking	400				V/mV min
		R_L = 25 kΩ[4]	Sourcing	2500				V/mV min
			Sinking	200				V/mV min
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$		4.995	4.990 **4.980**	4.950 **4.925**	4.990 **4.970**	V min
				0.005	0.010 **0.020**	0.050 **0.075**	0.010 **0.030**	V max
		V^+ = 5V R_L = 25 kΩ to $V^+/2$		4.990	4.975 **4.965**	4.950 **4.850**	4.975 **4.955**	V min
				0.010	0.020 **0.035**	0.050 **0.150**	0.020 **0.045**	V max
		V^+ = 15V R_L = 100 kΩ to $V^+/2$		14.990	14.975 **14.965**	14.950 **14.925**	14.975 **14.955**	V min
				0.010	0.025 **0.035**	0.050 **0.075**	0.025 **0.050**	V max
		V^+ = 15V R_L = 25 kΩ to $V^+/2$		14.965	14.900 **14.850**	14.850 **14.800**	14.900 **14.800**	V min
				0.025	0.050 **0.150**	0.100 **0.200**	0.050 **0.200**	V max

(4) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC6462AI LMC6464AI Limit(2)	LMC6462BI LMC6464BI Limit(2)	LMC6462AM LMC6464AM Limit(2)	Units
I_{SC}	Output Short Circuit Current V+ = 5V	Sourcing, V_O = 0V	27	19 **15**	19 **15**	19 **15**	mA min
		Sinking, V_O = 5V	27	22 **17**	22 **17**	22 **17**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	38	24 **17**	24 **17**	24 **17**	mA min
		Sinking, V_O = 12V(5)	75	55 **45**	55 **45**	55 **45**	mA min
I_S	Supply Current	Dual, LMC6462 V^+ = +5V, $V_O = V^+/2$	40	55 **70**	55 **70**	55 **75**	µA max
		Quad, LMC6464 V^+ = +5V, $V_O = V^+/2$	80	110 **140**	110 **140**	110 **150**	µA max
		Dual, LMC6462 V^+ = +15V, $V_O = V^+/2$	50	60 **70**	60 **70**	60 **75**	µA max
		Quad, LMC6464 V^+ = +15V, $V_O = V^+/2$	90	120 **140**	120 **140**	120 **150**	µA max

(5) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC6462AI LMC6464AI Limit(2)	LMC6462BI LMC6464BI Limit(2)	LMC6462AM LMC6464AM Limit(2)	Units
SR	Slew Rate	See(3)	28	15 **8**	15 **8**	15 **8**	V/ms min
GBW	Gain-Bandwidth Product	V^+ = 15V	50				kHz
φ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	See(4)	130				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	80				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				pA/$\sqrt{Hz}$

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.
(4) Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

3V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ[1]	LMC6462AI LMC6464AI Limit[2]	LMC6462BI LMC6464BI Limit[2]	LMC6462AM LMC6464AM Limit[2]	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	2.0 **3.0**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Current	See[3]	0.15	**10**	**10**	**200**	pA
I_{OS}	Input Offset Current	See[3]	0.075	**5**	**5**	**100**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	60	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	60	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.10	0.0	0.0	0.0	V max
			3.0	3.0	3.0	3.0	V min
V_O	Output Swing	R_L = 25 kΩ to $V^+/2$	2.95	2.9	2.9	2.9	V min
			0.15	0.1	0.1	0.1	V max
I_S	Supply Current	Dual, LMC6462 $V_O = V^+/2$	40	55 **70**	55 **70**	55 **70**	µA
		Quad, LMC6464 $V_O = V^+/2$	80	110 **140**	110 **140**	110 **140**	µA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

3V AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ[1]	LMC6462AI LMC6464AI Limit[2]	LMC6462BI LMC6464BI Limit[2]	LMC6462AM LMC6464AM Limit[2]	Units
SR	Slew Rate	See[3]	23				V/ms
GBW	Gain-Bandwidth Product		50				kHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Typical Performance Characteristics

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

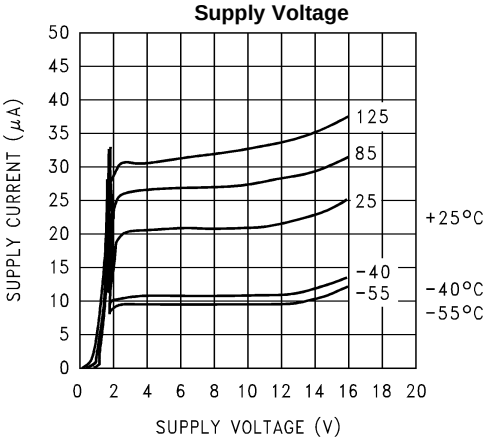


Figure 4.

Sourcing Current vs. Output Voltage

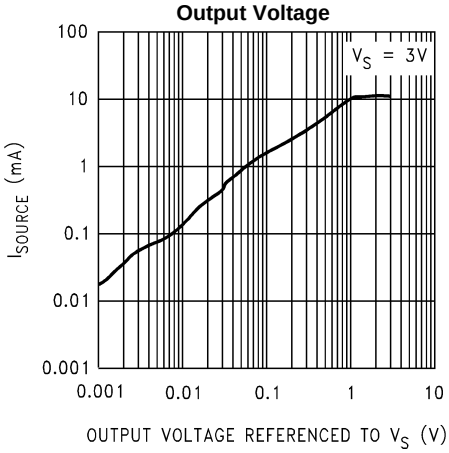


Figure 5.

Sourcing Current vs. Output Voltage

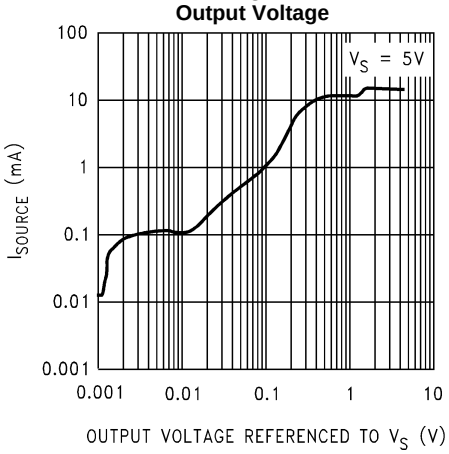


Figure 6.

Sourcing Current vs. Output Voltage

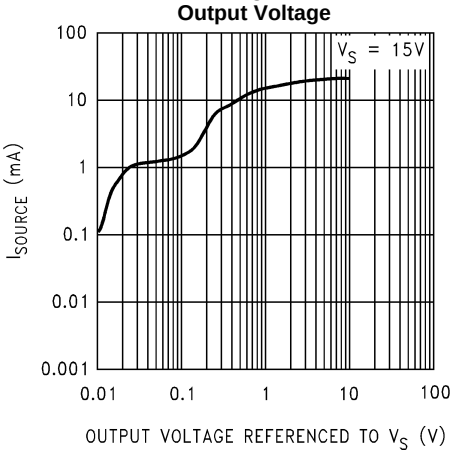


Figure 7.

Sinking Current vs. Output Voltage

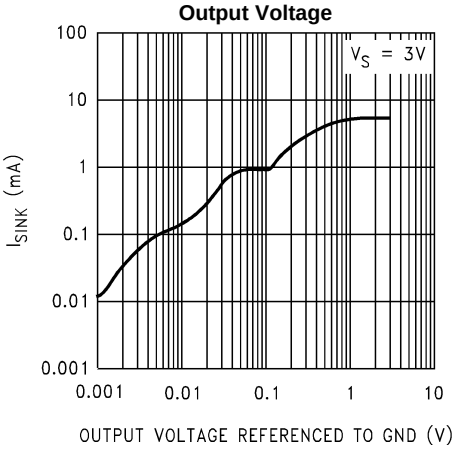


Figure 8.

Sinking Current vs. Output Voltage

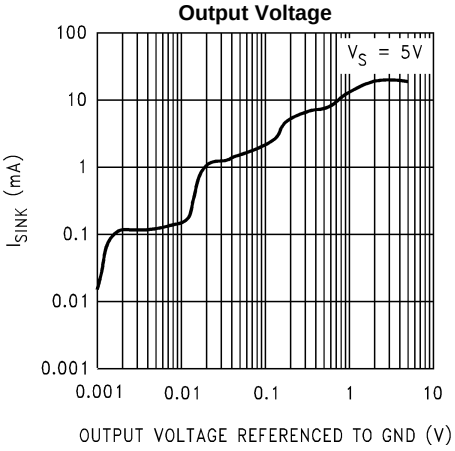


Figure 9.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Sinking Current vs. Output Voltage

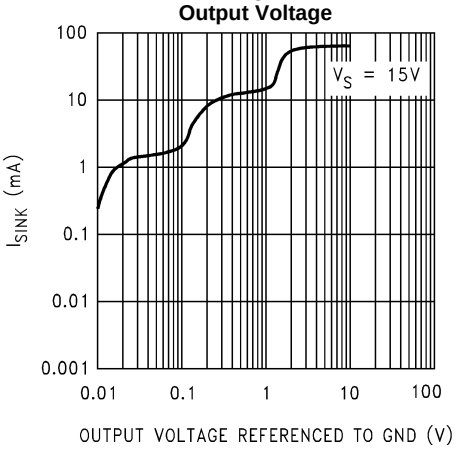


Figure 10.

Input Voltage Noise vs Frequency

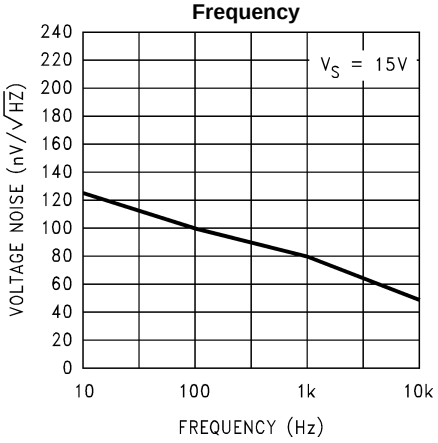


Figure 11.

Input Voltage Noise vs. Input Voltage

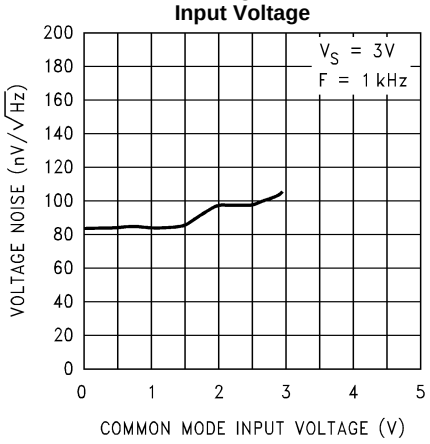


Figure 12.

Input Voltage Noise vs. Input Voltage

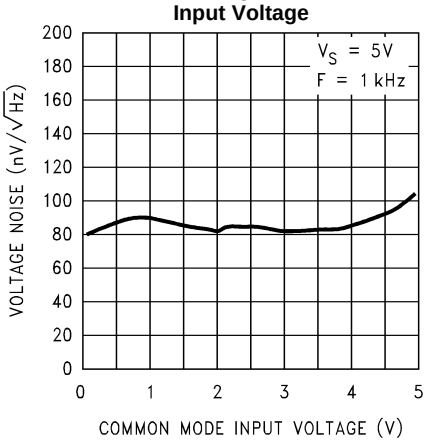


Figure 13.

Input Voltage Noise vs. Input Voltage

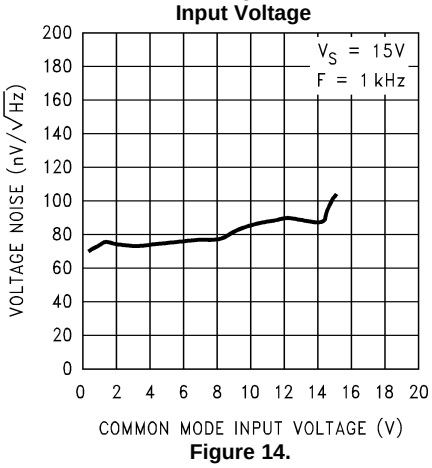


Figure 14.

ΔV_{OS} vs CMR

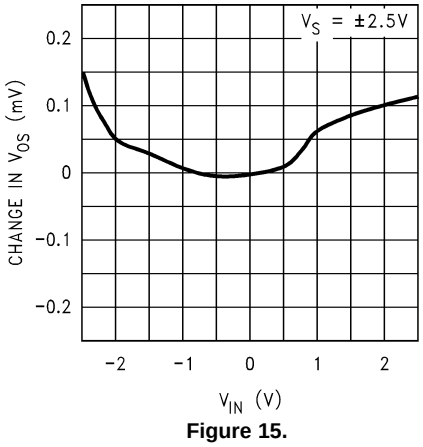


Figure 15.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage vs. Output Voltage

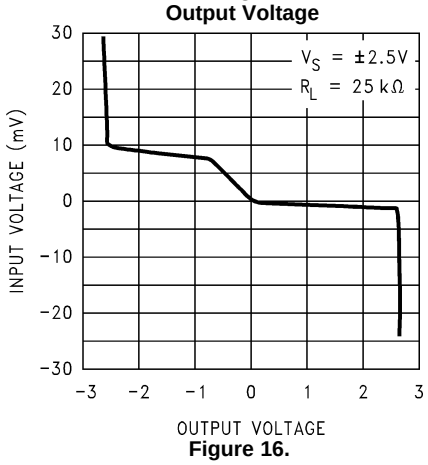


Figure 16.

Open Loop Frequency Response

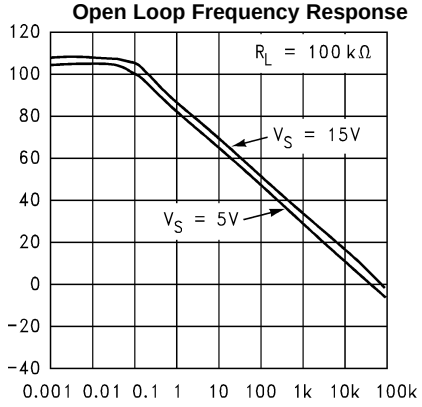


Figure 17.

Open Loop Frequency Response vs. Temperature

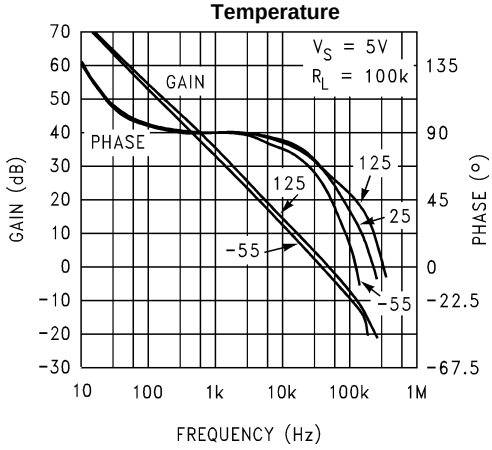


Figure 18.

Gain and Phase vs. Capacitive Load

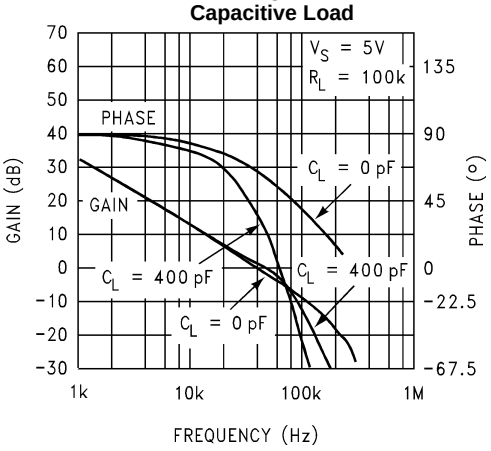


Figure 19.

Slew Rate vs. Supply Voltage

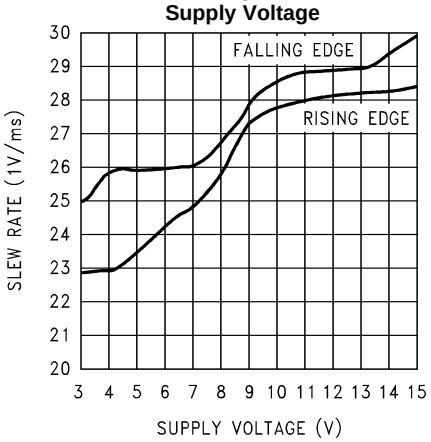


Figure 20.

Non-Inverting Large Signal Pulse Response

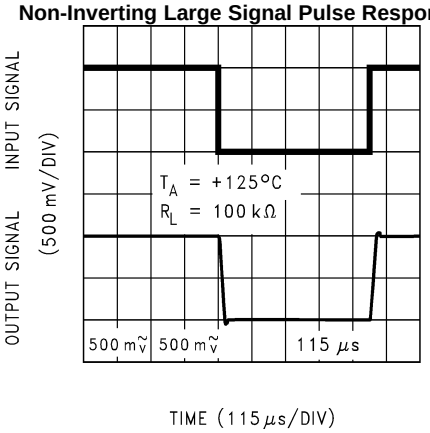
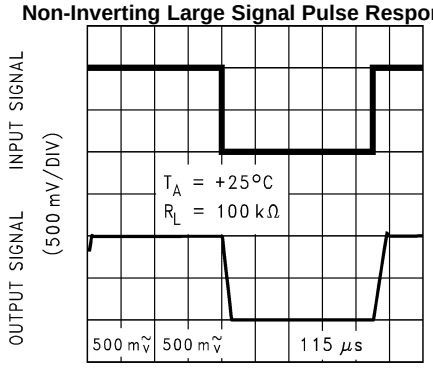


Figure 21.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

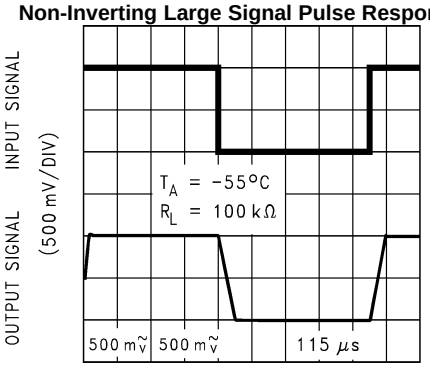
Non-Inverting Large Signal Pulse Response



TIME (115 μs/DIV)

Figure 22.

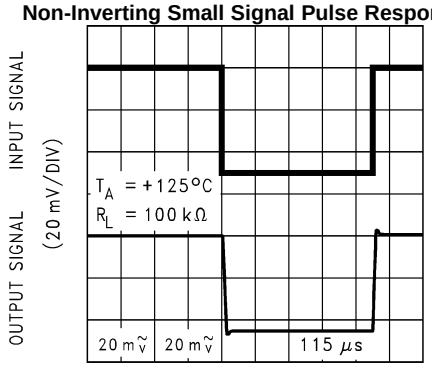
Non-Inverting Large Signal Pulse Response



TIME (115 μs/DIV)

Figure 23.

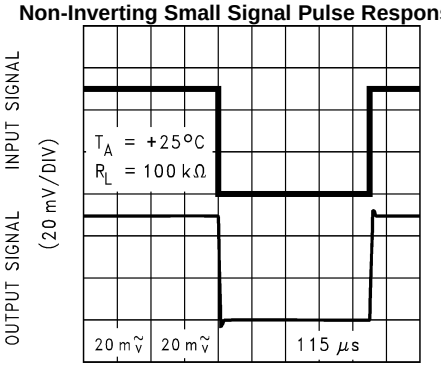
Non-Inverting Small Signal Pulse Response



TIME (115 μs/DIV)

Figure 24.

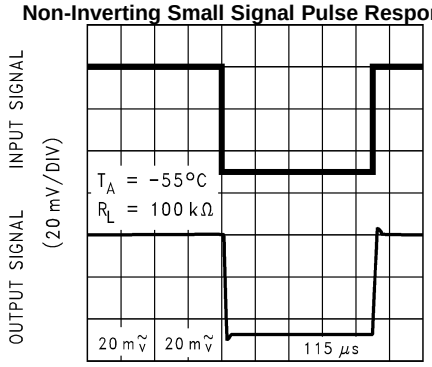
Non-Inverting Small Signal Pulse Response



TIME (115 μs/DIV)

Figure 25.

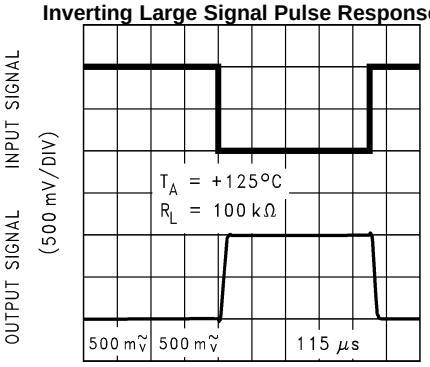
Non-Inverting Small Signal Pulse Response



TIME (115 μs/DIV)

Figure 26.

Inverting Large Signal Pulse Response



TIME (115 μs/DIV)

Figure 27.

Typical Performance Characteristics (continued)

V_S = +5V, Single Supply, T_A = 25°C unless otherwise specified

Inverting Large Signal Pulse Response

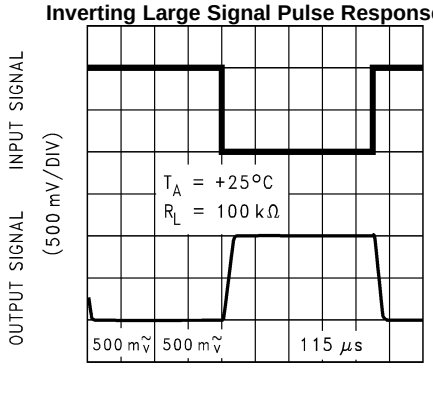


Figure 28.

Inverting Large Signal Pulse Response

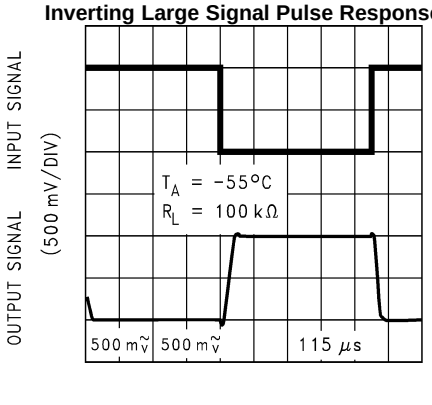


Figure 29.

Inverting Small Signal Pulse Response

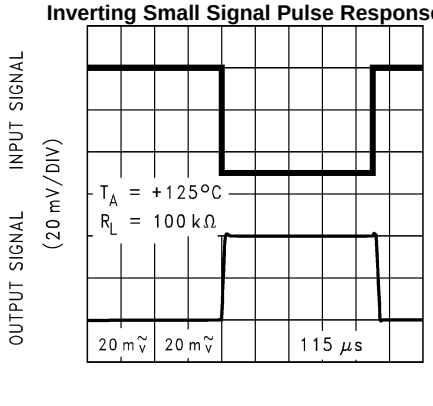


Figure 30.

Inverting Small Signal Pulse Response

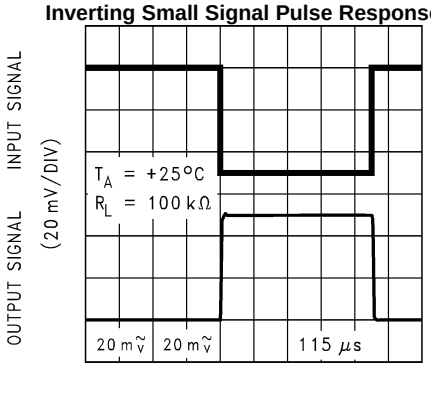


Figure 31.

Inverting Small Signal Pulse Response

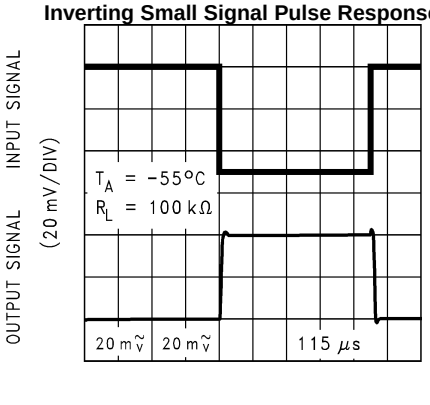


Figure 32.

APPLICATION INFORMATION

Input Common-Mode Voltage Range

The LMC6462/4 has a rail-to-rail input common-mode voltage range. Figure 33 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

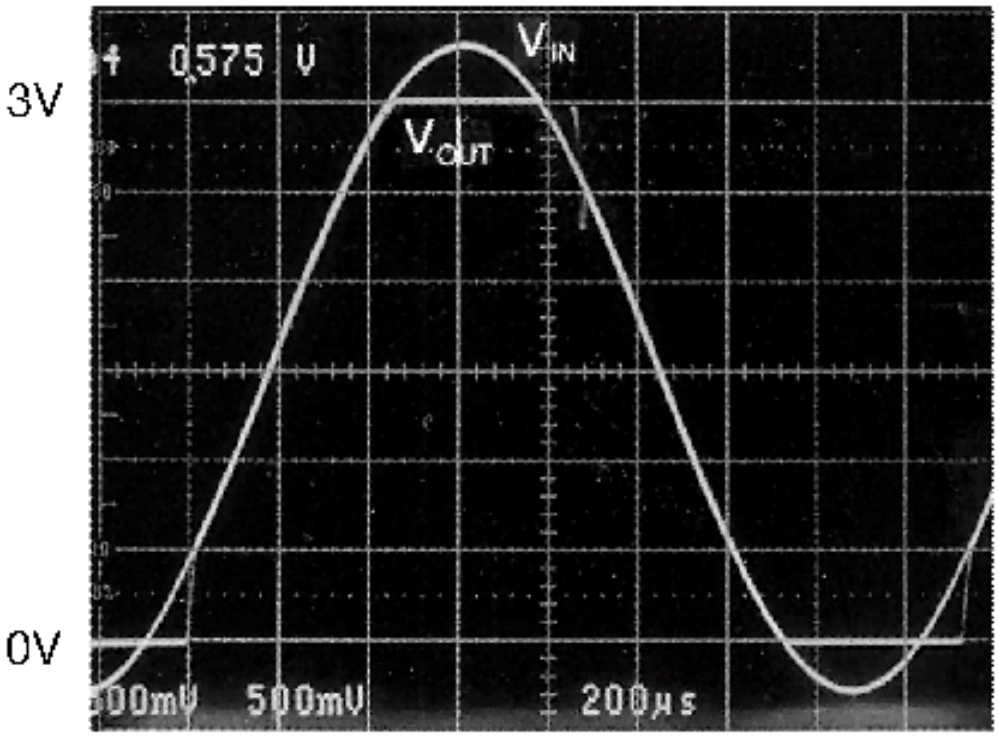


Figure 33. An Input Voltage Signal Exceeds the LMC6462/4 Power Supply Voltage with No Output Phase Inversion

The absolute maximum input voltage at V^+ = 3V is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 34, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to ±5 mA, with an input resistor, as shown in Figure 35.

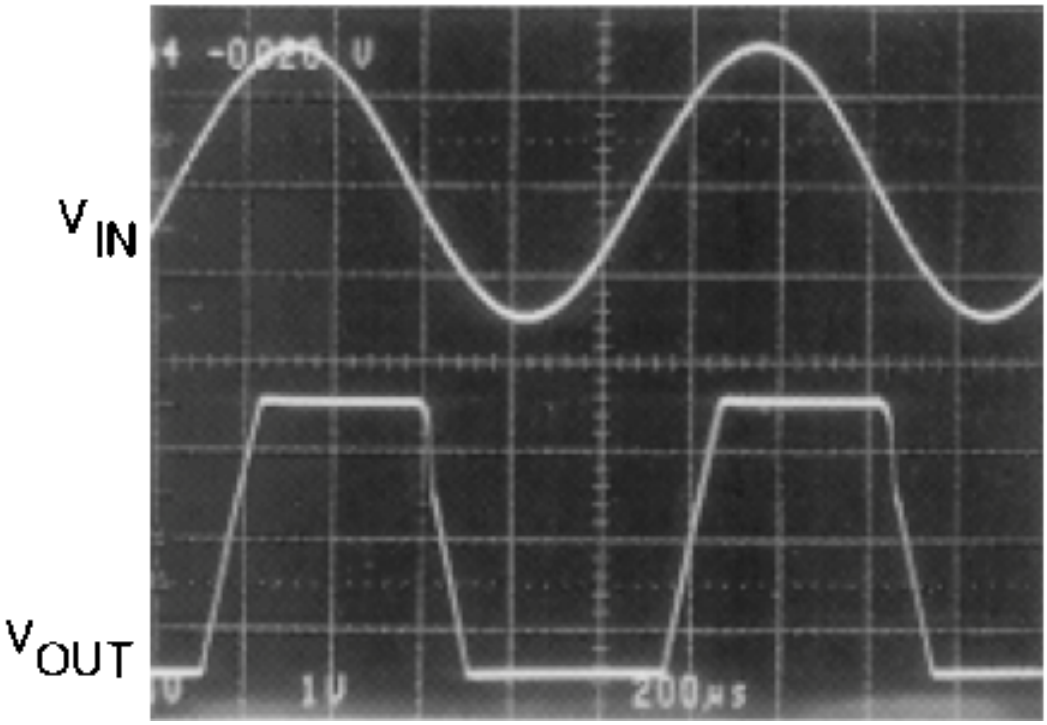


Figure 34. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in Figure 35 Causing No Phase Inversion Due to R_I

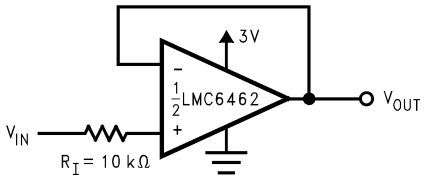


Figure 35. Input Current Protection for Voltages Exceeding the Supply Voltage

Rail-to-Rail Output

The approximated output resistance of the LMC6462/4 is 180Ω sourcing, and 130Ω sinking at V_S = 3V, and 110Ω sourcing and 83Ω sinking at V_S = 5V. The maximum output swing can be estimated as a function of load using the calculated output resistance.

Capacitive Load Tolerance

The LMC6462/4 can typically drive a 200 pF load with V_S = 5V at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 36. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

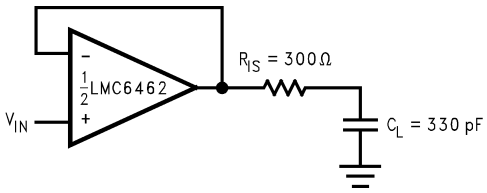


Figure 36. Resistive Isolation of a 300 pF Capacitive Load

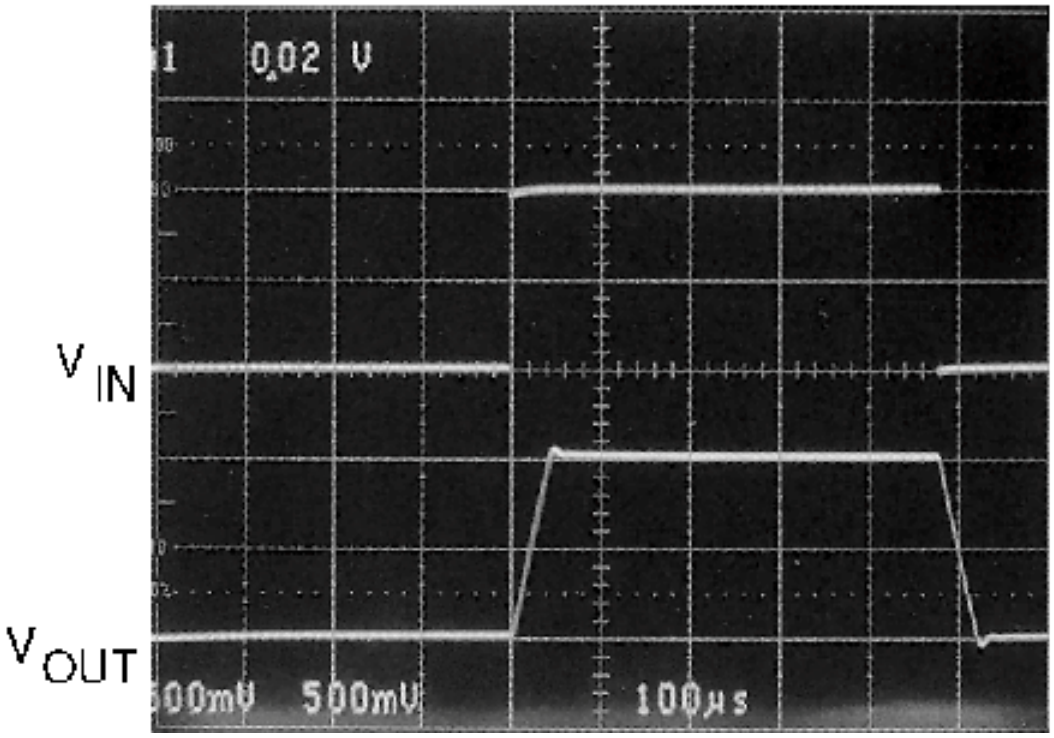


Figure 37. Pulse Response of the LMC6462 Circuit Shown in Figure 36

Figure 37 displays the pulse response of the LMC6462/4 circuit in Figure 36.

Another circuit, shown in Figure 38, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in Figure 36 because it provides DC accuracy as well as AC stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.

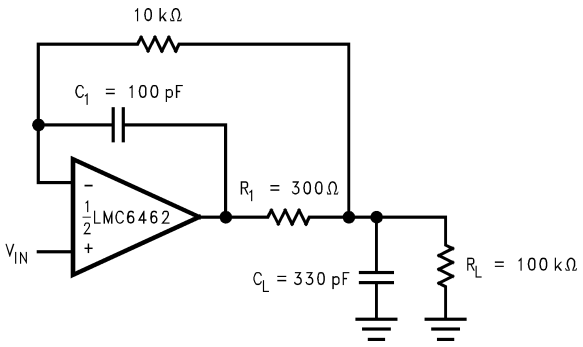


Figure 38. LMC6462 Non-Inverting Amplifier, Compensated to Handle a 300 pF Capacitive and 100 kΩ Resistive Load

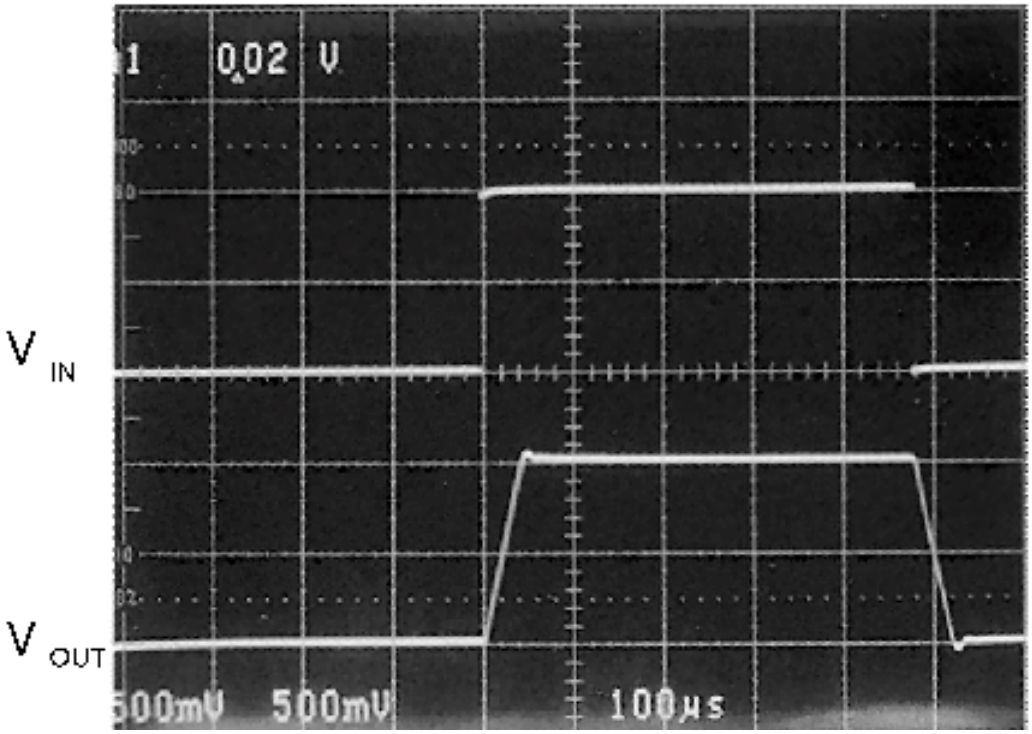


Figure 39. Pulse Response of LMC6462 Circuit in Figure 38

The pulse response of the circuit shown in Figure 38 is shown in Figure 39

Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6462/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

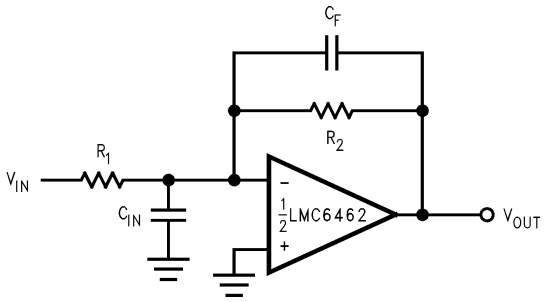


Figure 40. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 40), C_F, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_F \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 41 and Figure 42. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

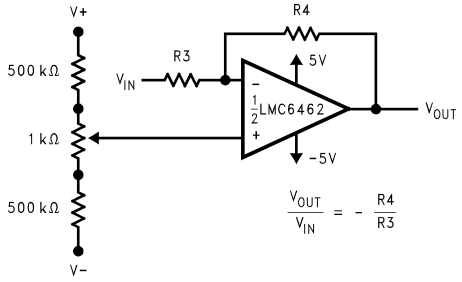


Figure 41. Inverting Configuration Offset Voltage Adjustment

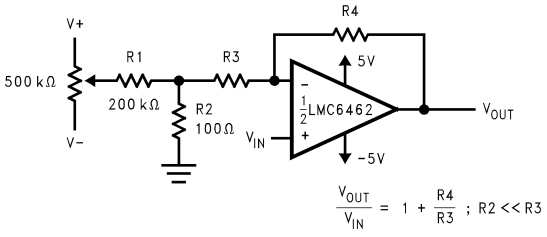


Figure 42. Non-Inverting Configuration Offset Voltage Adjustment

SPICE Macromodel

A Spice macromodel is available for the LMC6462/4. This model includes a simulation of:

- Input common-mode voltage range

- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact the Texas Instruments Customer Response Center to obtain an operational amplifier Spice model library disk

Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6462/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6462's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 43. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 30 times degradation from the LMC6462/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 44 through Figure 46 for typical connections of guard rings for standard op-amp configurations.

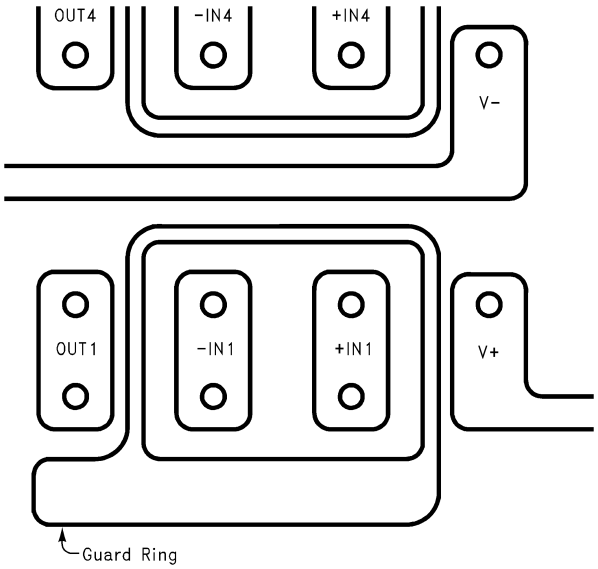


Figure 43. Example of Guard Ring in P.C. Board Layout

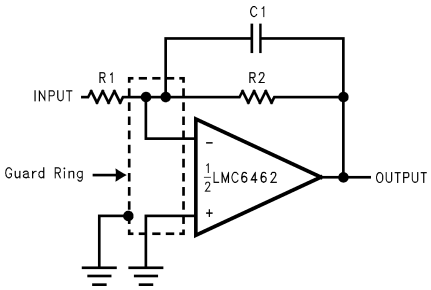


Figure 44. Typical Connections of Guard Rings – Inverting Amplifier

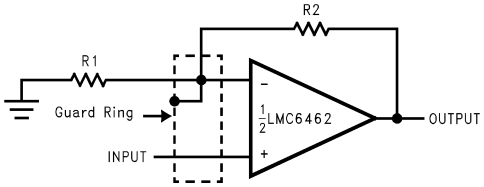


Figure 45. Typical Connections of Guard Rings – Non-Inverting Amplifier

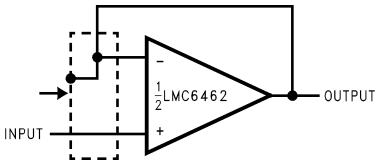
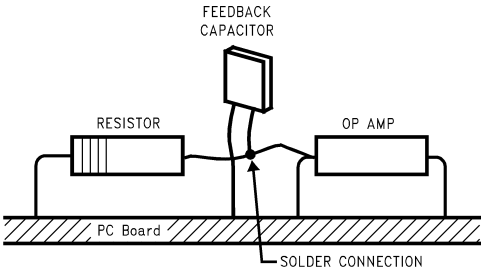


Figure 46. Typical Connections of Guard Rings – Follower

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 47.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 47. Air Wiring

Instrumentation Circuits

The LMC6464 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6464 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6464 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_G to set the differential gain of the three op-amp instrumentation circuit in Figure 48. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

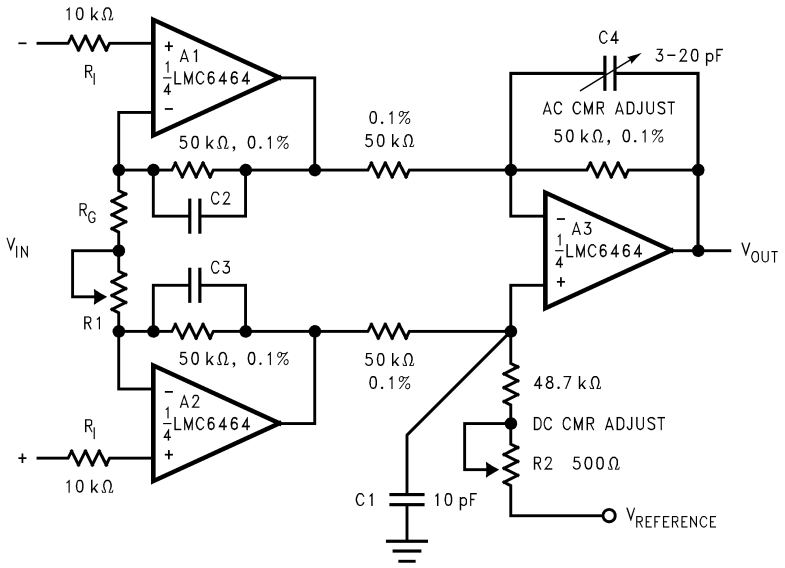


Figure 48. Low Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 49. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

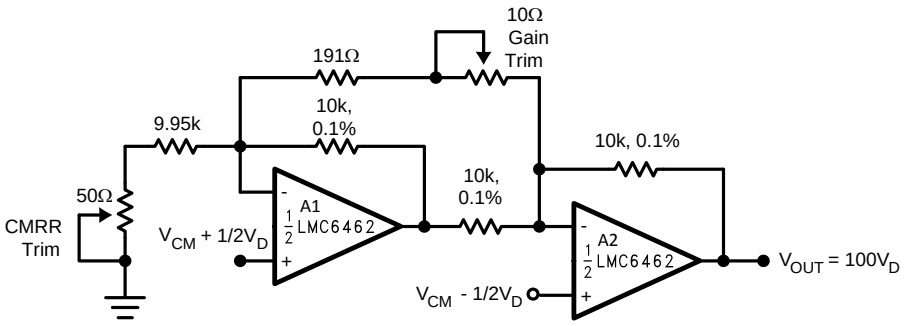


Figure 49. Low-Power Two-Op-Amp Instrumentation Amplifier

TYPICAL SINGLE-SUPPLY APPLICATIONS

Transducer Interface Circuits

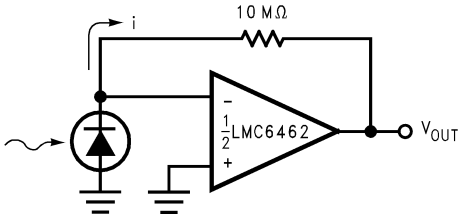


Figure 50. Photo Detector Circuit

Photocells can be used in portable light measuring instruments. The LMC6462, which can be operated off a battery, is an excellent choice for this circuit because of its very low input current and offset voltage.

LMC6462 as a Comparator

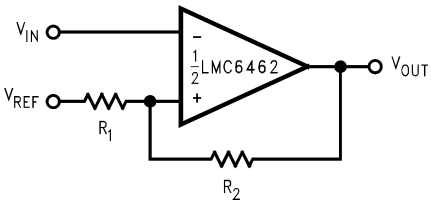


Figure 51. Comparator with Hysteresis

Figure 51 shows the application of the LMC6462 as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC6462 can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

Half-Wave and Full-Wave Rectifiers

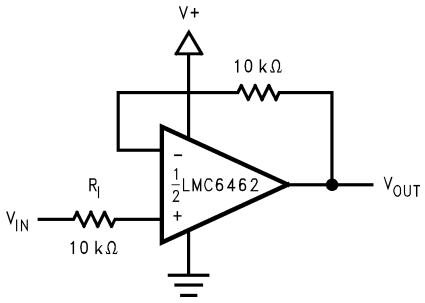


Figure 52. Half-Wave Rectifier with Input Current Protection (R_I)

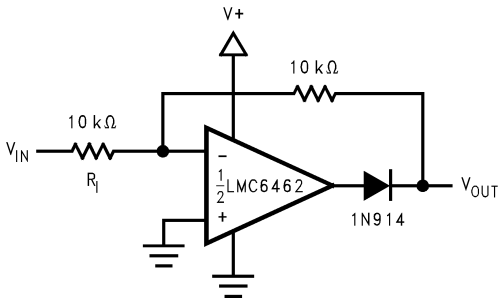


Figure 53. Full-Wave Rectifier with Input Current Protection (R_I)

In Figure 52 Figure 53, R_I limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

Precision Current Source

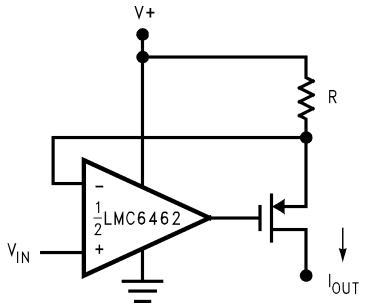


Figure 54. Precision Current Source

The output current I_{OUT} is given by:

$$I_{OUT} = \left(\frac{V^+ - V_{IN}}{R}\right) \quad (3)$$

Oscillators

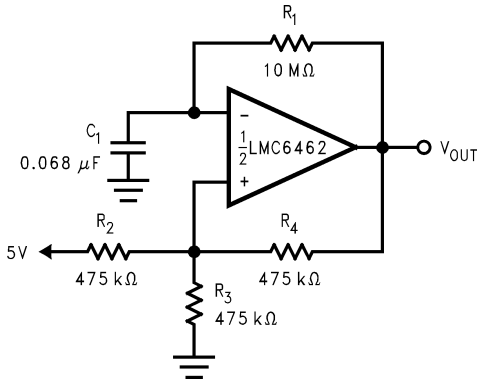


Figure 55. 1 Hz Square-Wave Oscillator

For single supply 5V operation, the output of the circuit will swing from 0V to 5V. The voltage divider set up R_2, R_3 and R_4 will cause the non-inverting input of the LMC6462 to move from 1.67V (⅓ of 5V) to 3.33V (⅔ of 5V). This voltage behaves as the threshold voltage.

R_1 and C_1 determine the time constant of the circuit. The frequency of oscillation, f_{OSC} is

$$\left(\frac{1}{2\Delta t}\right) \quad (4)$$

where Δt is the time the amplifier input takes to move from 1.67V to 3.33V. The calculations are shown below.

$$1.67 = 5\left(1 - e^{-\frac{t_1}{\tau}}\right) \quad (5)$$

where τ = RC = 0.68 seconds

$\rightarrow t_1 = 0.27$ seconds.

and

$$3.33 = 5\left(1 - e^{-\frac{t_2}{\tau}}\right) \quad (6)$$

$\rightarrow t_2 = 0.75$ seconds

Then,

$$f_{OSC} = \left(\frac{1}{2\Delta t}\right) \quad (7)$$

$$= \frac{1}{2\,(0.75 - 0.27)} \quad (8)$$

= 1 Hz

Low Frequency Null

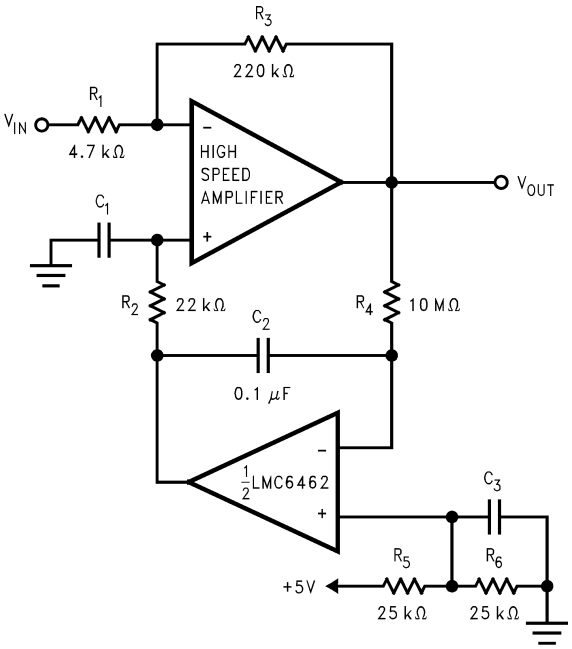


Figure 56. High Gain Amplifier with Low Frequency Null

Output offset voltage is the error introduced in the output voltage due to the inherent input offset voltage V_{OS}, of an amplifier.

Output Offset Voltage = (Input Offset Voltage) (Gain)

In the above configuration, the resistors R_5 and R_6 determine the nominal voltage around which the input signal, V_{IN} should be symmetrical. The high frequency component of the input signal V_{IN} will be unaffected while the low frequency component will be nulled since the DC level of the output will be the input offset voltage of the LMC6462 plus the bias voltage. This implies that the output offset voltage due to the top amplifier will be eliminated.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6462AIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Call TI	-40 to 85	LMC64 62AIM	
LMC6462AIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62AIM	Samples
LMC6462AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62AIM	Samples
LMC6462AIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 85	LMC6462 AIN	Samples
LMC6462BIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62BIM	Samples
LMC6462BIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62BIM	Samples
LMC6462BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 85	LMC6462 BIN	Samples
LMC6464AIM	NRND	SOIC	D	14	55	Non-RoHS & Green	Call TI	Call TI	-40 to 85	LMC6464 AIM	
LMC6464AIM/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 AIM	Samples
LMC6464AIMX	NRND	SOIC	D	14	2500	Non-RoHS & Green	Call TI	Call TI	-40 to 85	LMC6464 AIM	
LMC6464AIMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 AIM	Samples
LMC6464BIM	NRND	SOIC	D	14	55	Non-RoHS & Green	Call TI	Call TI	-40 to 85	LMC6464 BIM	
LMC6464BIM/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 BIM	Samples
LMC6464BIMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 BIM	Samples
LMC6464BIN/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	Call TI | SN	Level-1-NA-UNLIM	-40 to 85	LMC6464BIN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

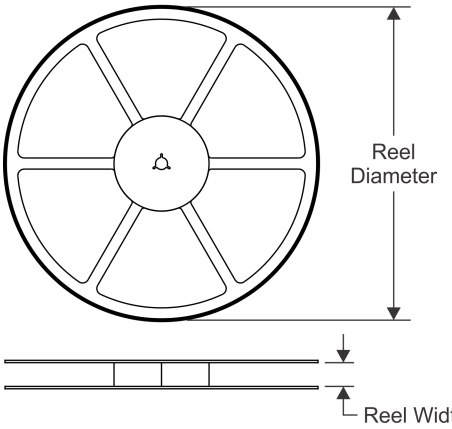
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

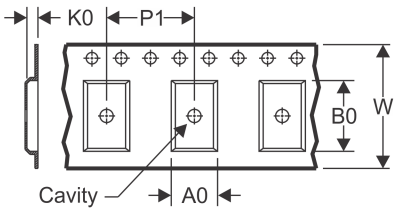
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

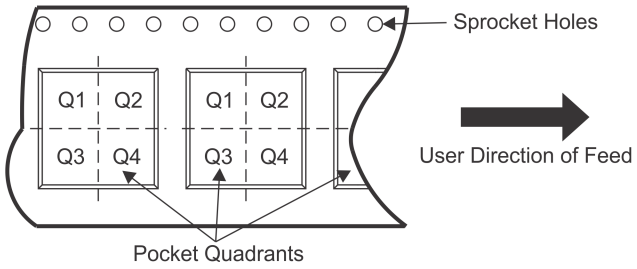


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

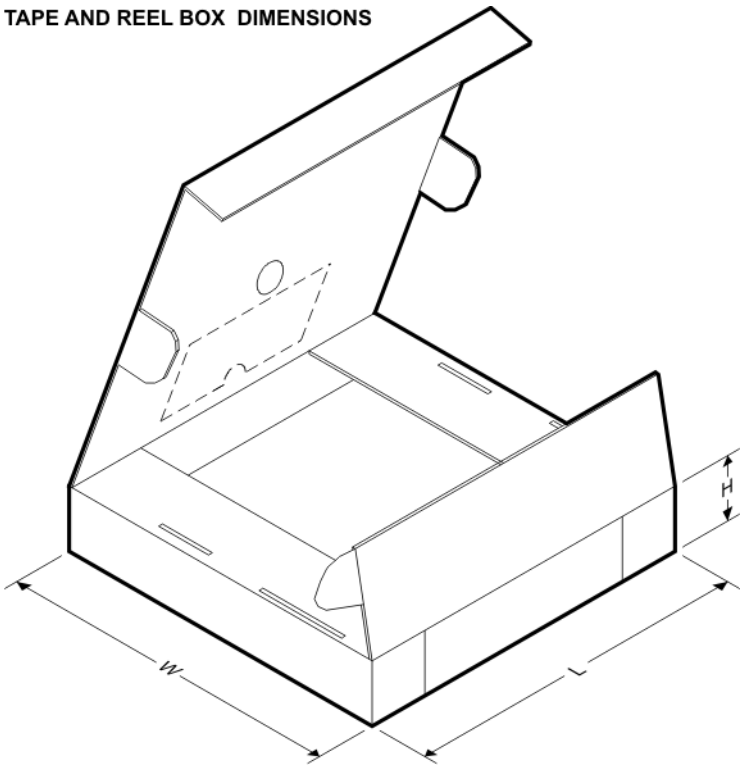
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6462AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6462BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6464AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6464BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

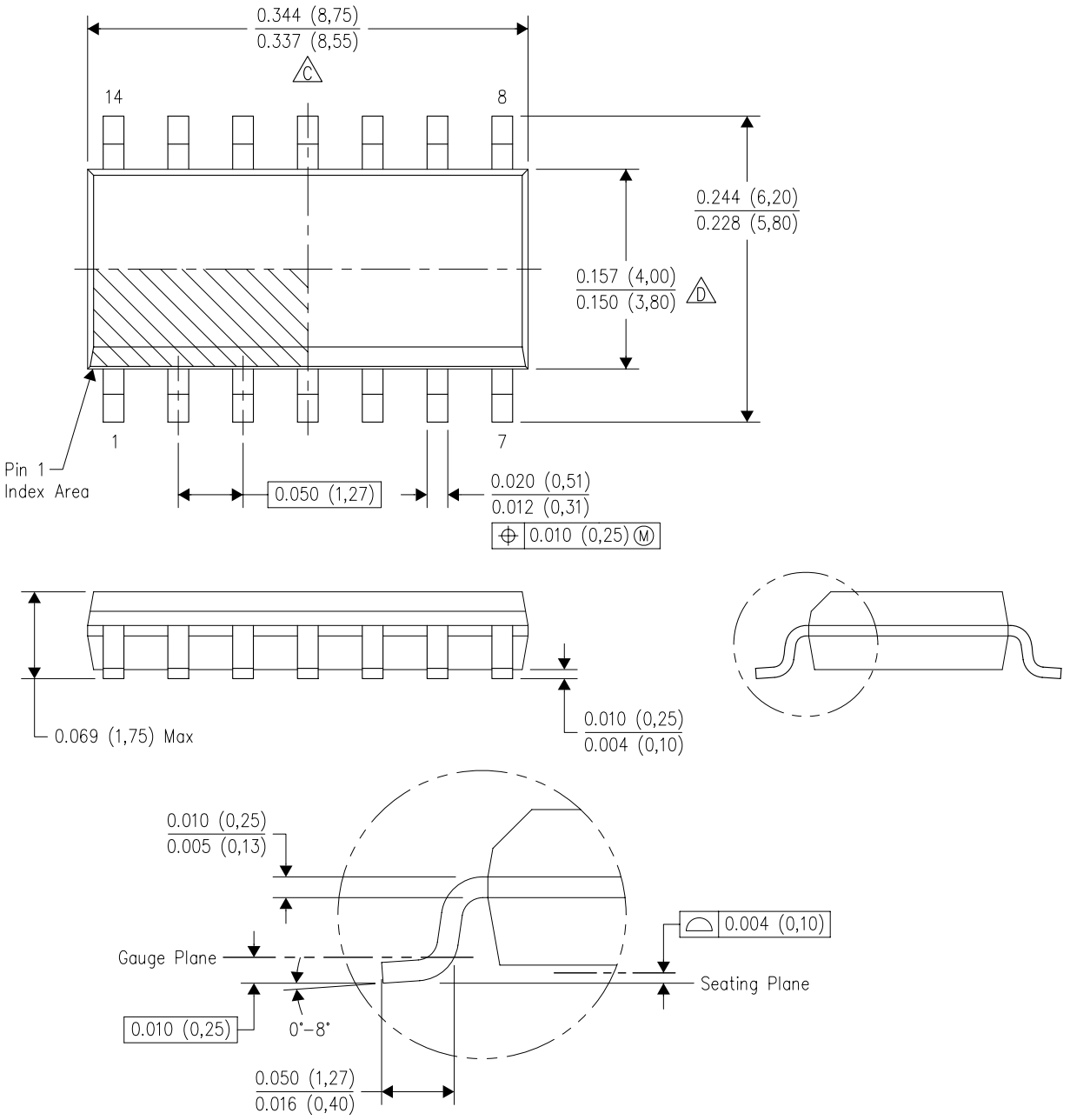
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6462AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6462BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6464AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6464BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

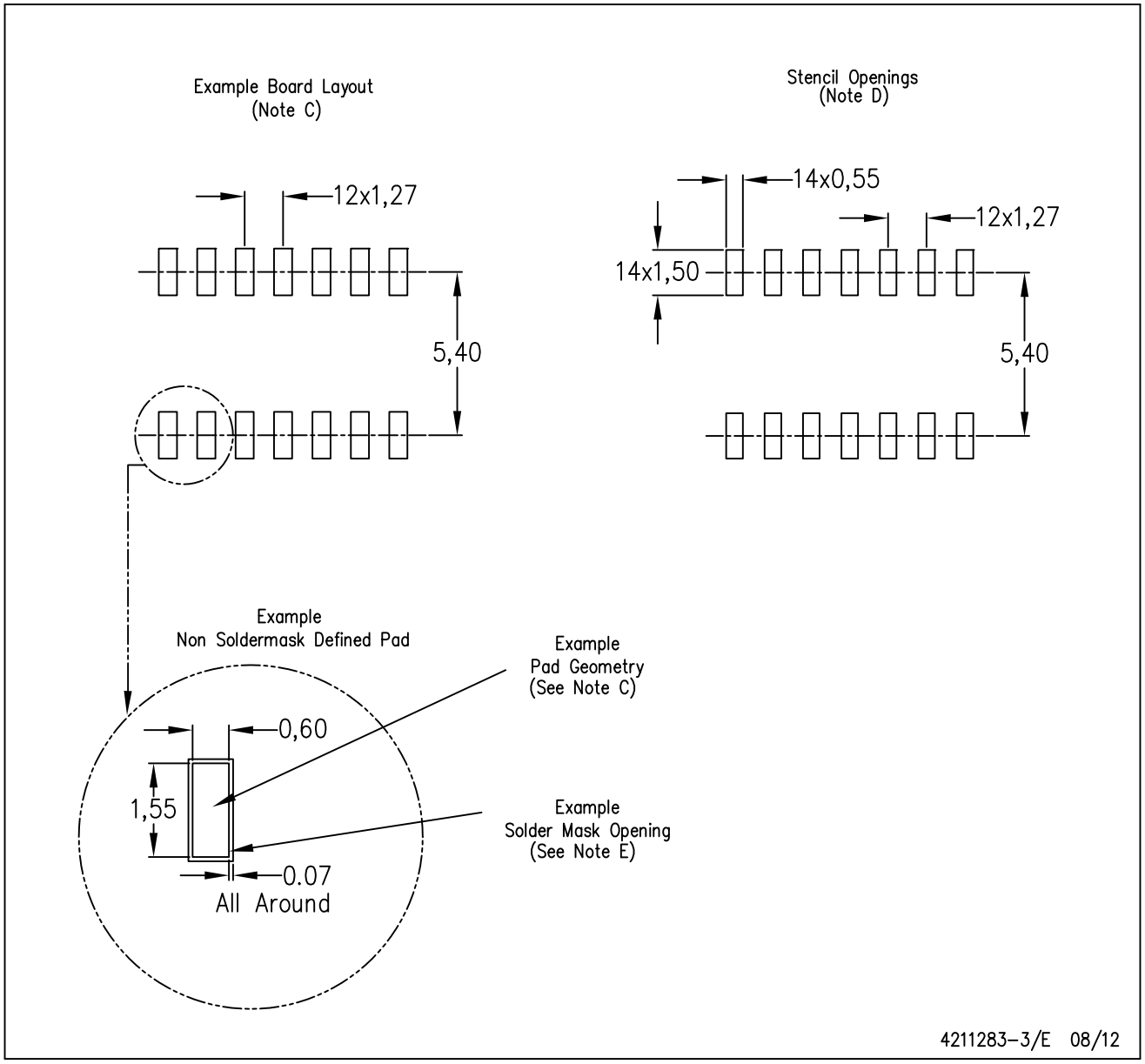
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



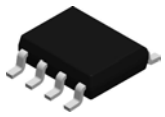
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

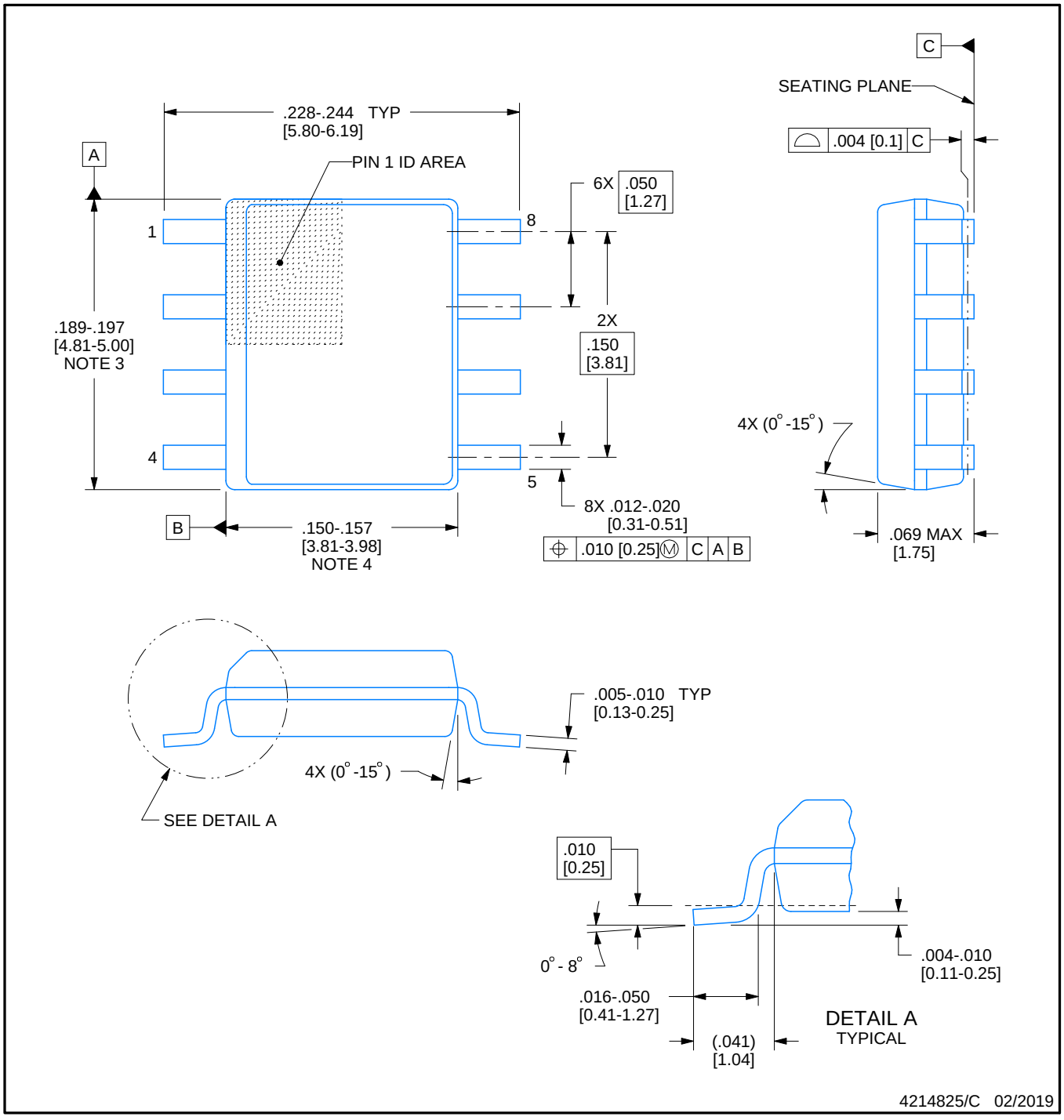


PACKAGE OUTLINE

D0008A

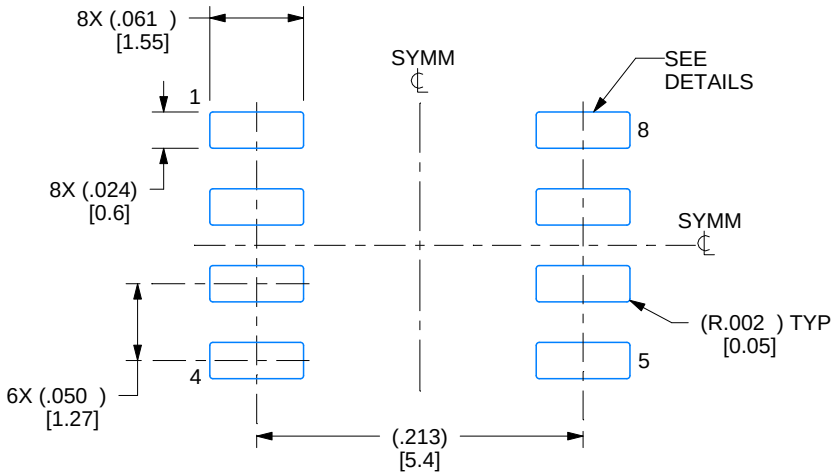
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

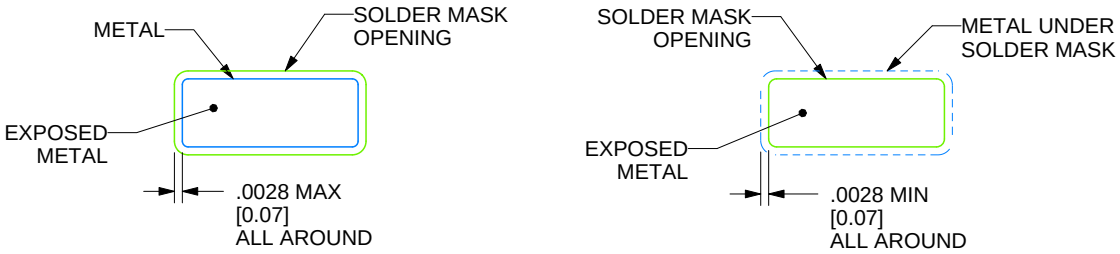


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

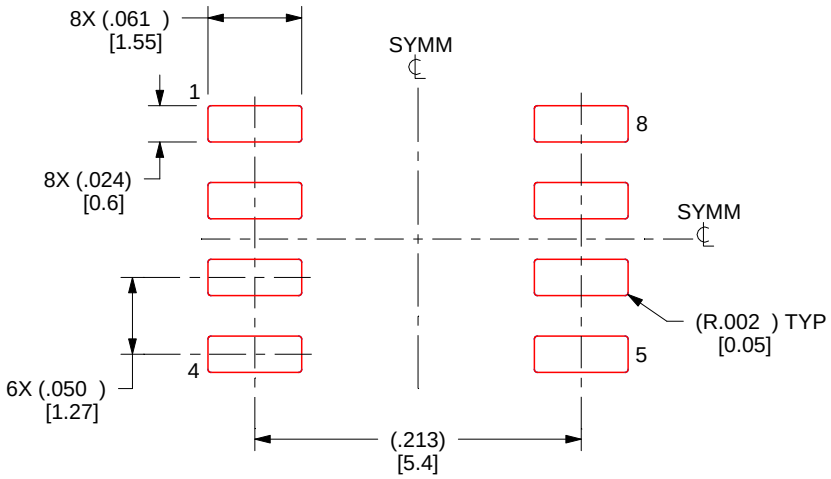
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



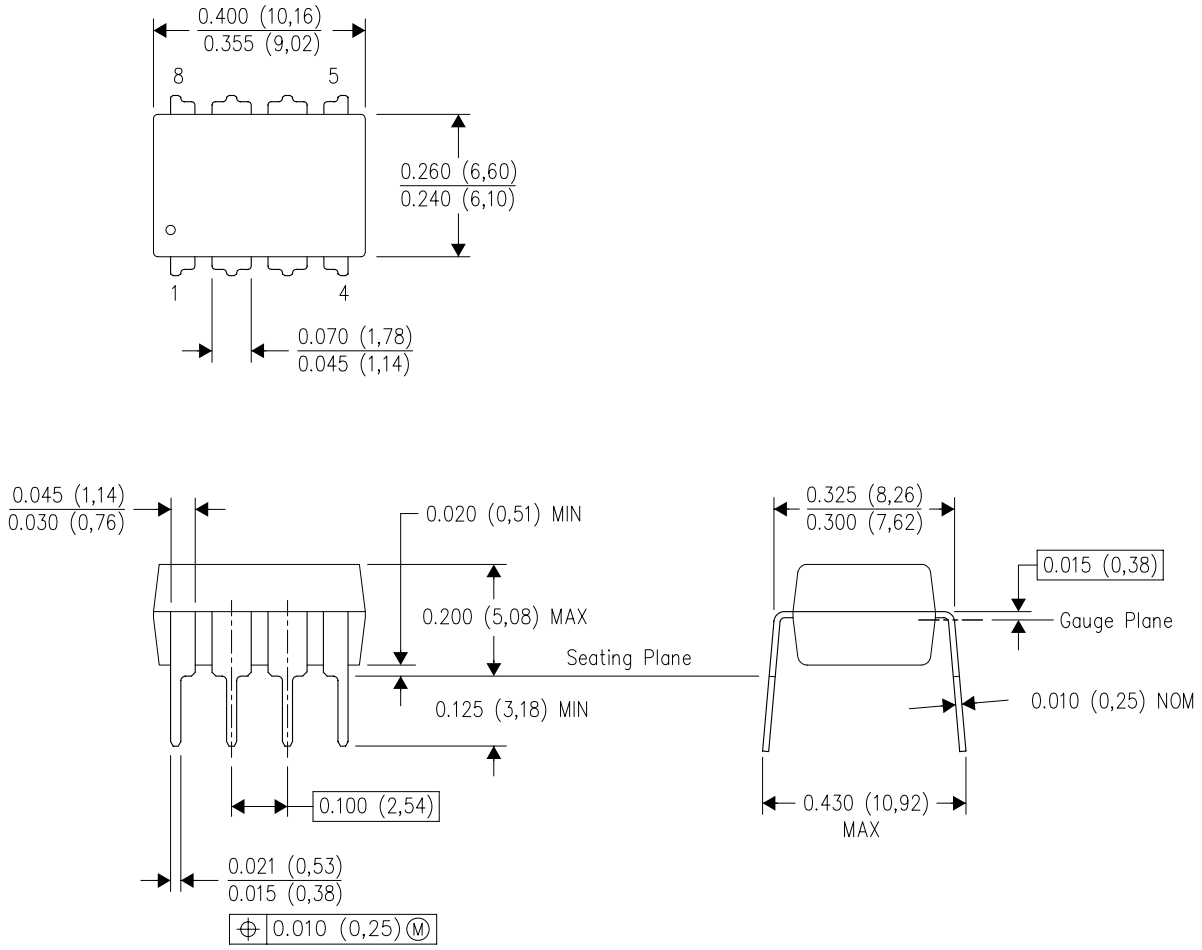
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

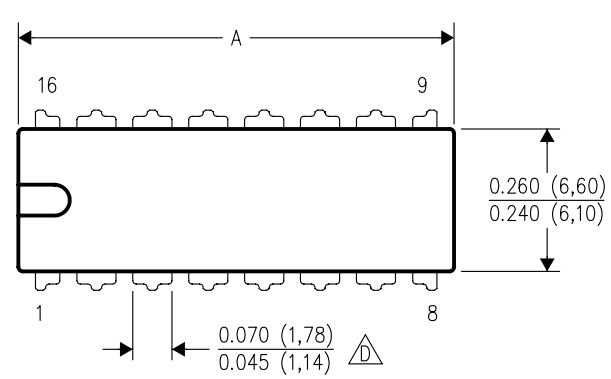


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

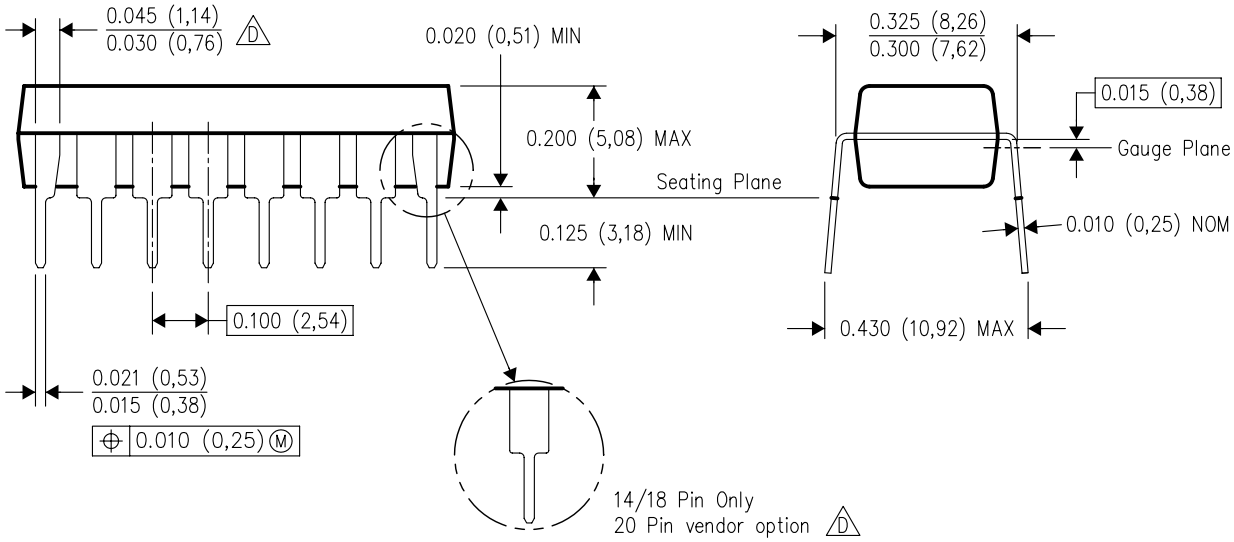
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265