LMC6482QML CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

Check for Samples: LMC6482QML

FEATURES

(Typical unless otherwise noted)

- **Rail-to-Rail Input Common-Mode Voltage Range (Ensured Over Temperature)**
- **Rail-to-Rail Output Swing (within 20mV of supply rail, 100KΩ load)**
- **Ensured 5V and 15V Performance**
- **Excellent CMRR and PSRR: 82dB**
- **Ultra Low Input Current: 20fA**
- **High Voltage Gain (R_L = 500KΩ): 130dB**
- **Specified for 2KΩ and 600Ω loads**

APPLICATIONS

- **Data Acquisition Systems**
- **Transducer Amplifiers**
- **Hand-held Analytic Instruments**
- **Medical Instrumentation**
- **Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source**
- **Improved Replacement for TLC272, TLC277**

DESCRIPTION

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

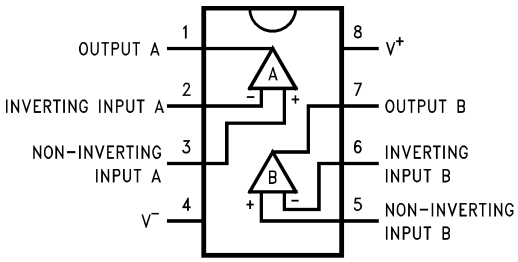
It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is ensured for loads down to 600Ω.

Ensured low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

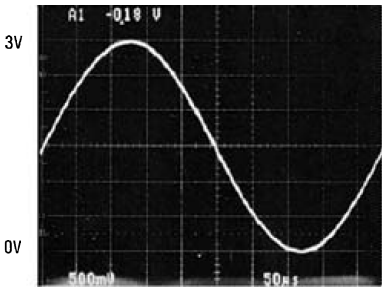
See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

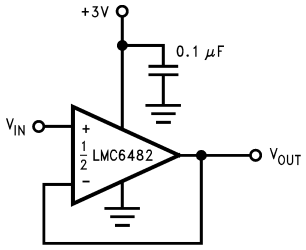
Connection Diagram



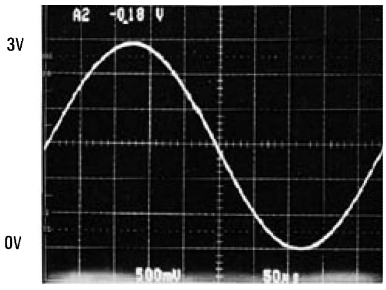
3V Single Supply Buffer Circuit

Rail-To-Rail Input





Rail-To-Rail Output



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage ($V^+ - V^-$)			16V
Differential Input Voltage			± Supply Voltage
Voltage at Input/Output Pin			(V^+) + 0.3V, (V^-) − 0.3V
Current at Input Pin(2)			±5 mA
Current at Output Pin(3)(4)			±30 mA
Current at Power Supply Pin			40 mA
Maximum Junction Temperature (T_{Jmax})(5)(3)			150°C
Power Dissipation(5)			160mW
Storage Temperature Range			−65°C ≤ T_A ≤ +150°C
Thermal Resistance(6)	θ_{JA}	8LD Ceramic DIP (Still Air)	117°C/W
		8LD Ceramic DIP (500LF/Min Air Flow)	62.0°C/W
	θ_{JC}	8LD Ceramic DIP	16.0°C/W
		Lead Temp. (Soldering, 10 sec.)	260°C
ESD Tolerance(7)			1.5KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(3) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(6) All numbers apply for packages soldered directly into a PC board.
(7) Human body model, 1.5 KΩ in series with 100 pF.

Recommended Operating Range(1)

Supply Voltage	3.0V ≤ V^+ ≤ 15.5V
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25

Quality Conformance Inspection (continued)

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LMC6482 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				0.75	mV	1
					1.35	mV	2, 3
I_{IB}	Input Bias Current				25	pA	1
					100	pA	2, 3
I_{IO}	Input Offset Current				25	pA	1
					100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$ $V^+ = 15V$		65		dB	1
				62		dB	2, 3
		$0V \le V_{CM} \le 5.0V$		65		dB	1
				62		dB	2, 3
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		65		dB	1
				62		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	$-15V \le V^- \le -5V$ $V_O = -2.5V$, $V^+ = 0V$		65		dB	1
				62		dB	2, 3
V_{CM}	Input Common Mode Voltage Range	$5V \le V_{CM} \le 15V$ For CMRR ≥ 50dB		V^++0.25	-0.25	V	1
				V^+	0.0	V	2, 3
I_{SC}	Output Short Circuit Current	Sourcing $V_O = 0V$		16		mA	1
				12		mA	2, 3
		Sinking $V_O = 5V$		11		mA	1
				9.0		mA	2, 3
		$V^+ = 15V$ Sourcing, $V_O = 0V$		28		mA	1
				22		mA	2, 3
		$V^+ = 15V$ Sinking, $V_O = 12V$	See (1)	30		mA	1
			See (1)	24		mA	2, 3
I_{CC}	Supply Current	Both Amps			1.4	mA	1
					1.8	mA	2, 3
		Both Amps $V^+ = +15V$			1.6	mA	1
					2.0	mA	2, 3
V_O	Output Swing	$V^+ = 5V$ $R_L = 2K\Omega$ to $V^+/2$		4.8	0.18	V	4
				4.7	0.24	V	5, 6
		$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$		4.5	0.50	V	4
				4.24	0.65	V	5, 6
		$V^+ = 15V$ $R_L = 2K\Omega$ to $V^+/2$		14.4	0.32	V	4
				14.2	0.45	V	5, 6
		$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$		13.4	1.00	V	4
				13.0	1.30	V	5, 6

(1) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

LMC6482 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
A_V	Large Signal Voltage Gain	R_L = 2KΩ Sourcing	See (2)	140		V/mV	4
			See (2)	84		V/mV	5, 6
		R_L = 2KΩ Sinking	See (2)	35		V/mV	4
			See (2)	20		V/mV	5, 6
		R_L = 600Ω Sourcing	See (2)	80		V/mV	4
			See (2)	48		V/mV	5, 6
		R_L = 600Ω Sinking	See (2)	18		V/mV	4
			See (2)	13		V/mV	5, 6

(2) $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

LMC6482 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate		See (1)	0.9		V/µS	4
			See (1)	0.6		V/µS	5, 6
GBW	Gain Bandwidth	$V^+ = 15V$ Set up for non-inverting		1.25		MHz	4
				1.15		MHz	5, 6

(1) $V^+ = 15V$. Connected as Voltage Follower with 10V step input, 2.5V to 12.5V for +slew, and 12.5V to 2.5V for −slew.. Number specified is the slower of either the positive or negative slew rates.

Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

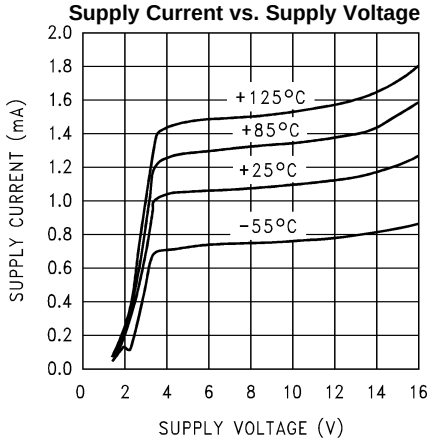


Figure 1.

Input Current vs. Temperature

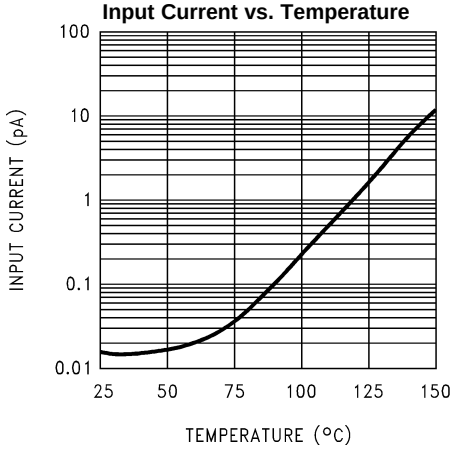


Figure 2.

Sourcing Current vs. Output Voltage

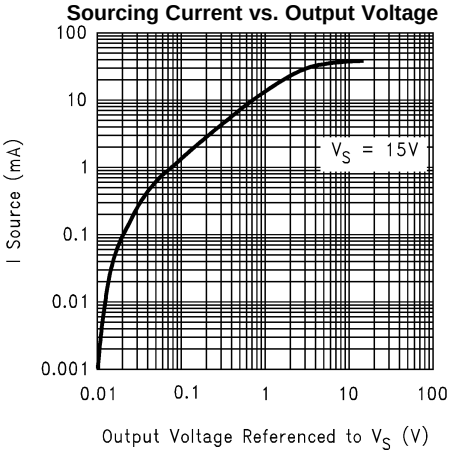


Figure 3.

Sourcing Current vs. Output Voltage

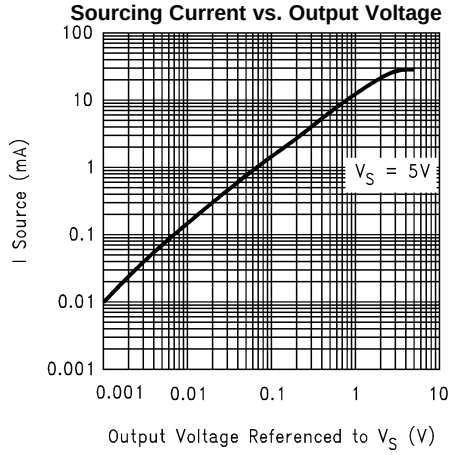


Figure 4.

Sourcing Current vs. Output Voltage

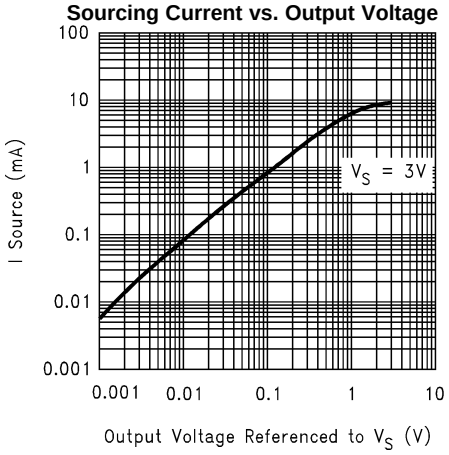


Figure 5.

Sinking Current vs. Output Voltage

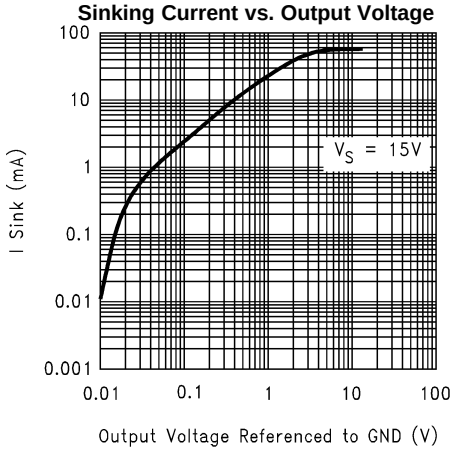


Figure 6.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Sinking Current vs. Output Voltage

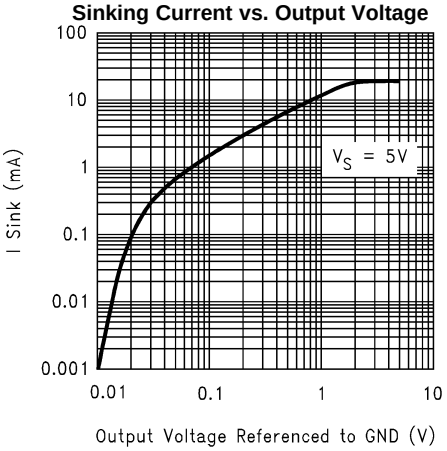


Figure 7.

Sinking Current vs. Output Voltage

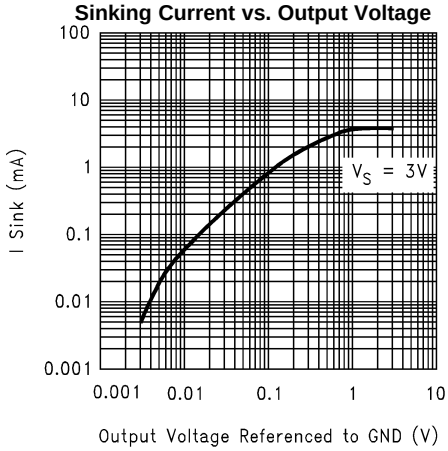


Figure 8.

Output Voltage Swing vs. Supply Voltage

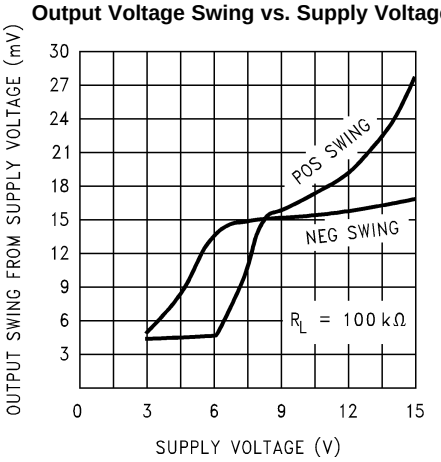


Figure 9.

Input Voltage Noise vs. Frequency

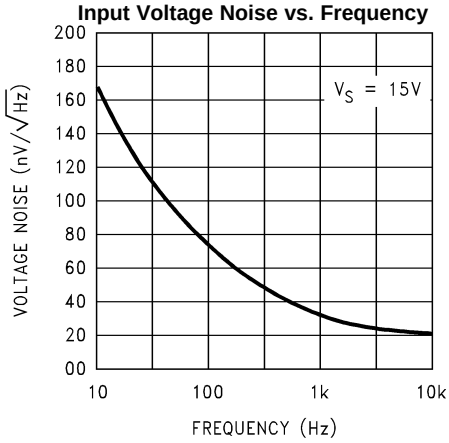


Figure 10.

Input Voltage Noise vs. Input Voltage

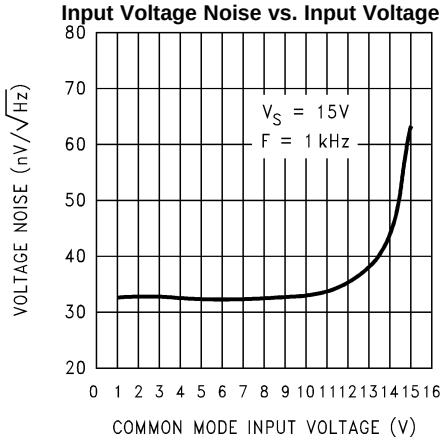


Figure 11.

Input Voltage Noise vs. Input Voltage

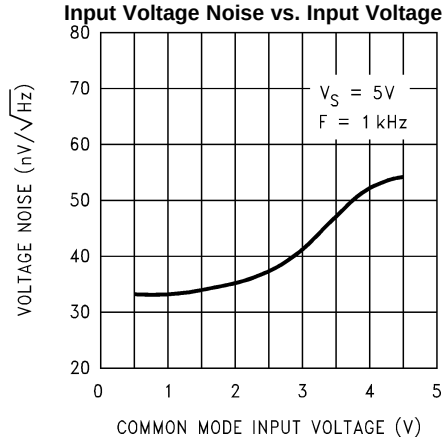


Figure 12.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage Noise vs. Input Voltage

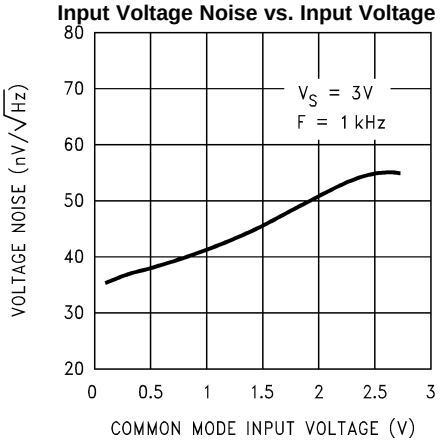


Figure 13.

Crosstalk Rejection vs. Frequency

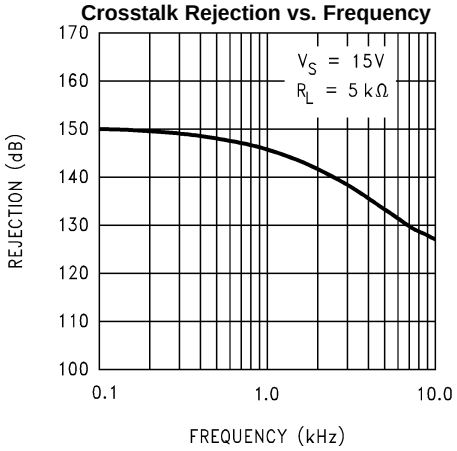


Figure 14.

Crosstalk Rejection vs. Frequency

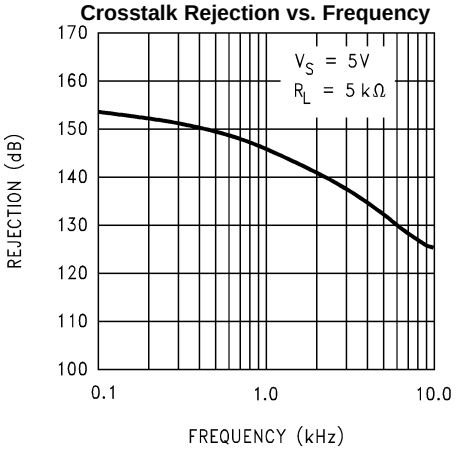


Figure 15.

Positive PSRR vs. Frequency

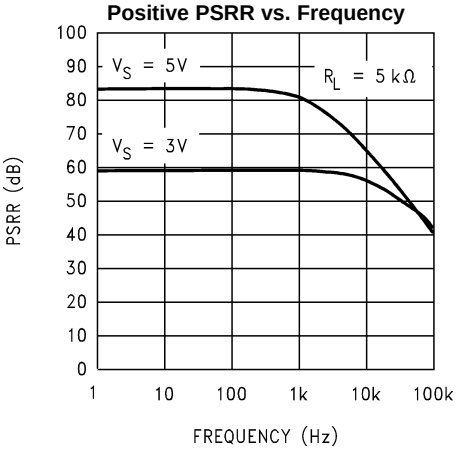


Figure 16.

Negative PSRR vs. Frequency

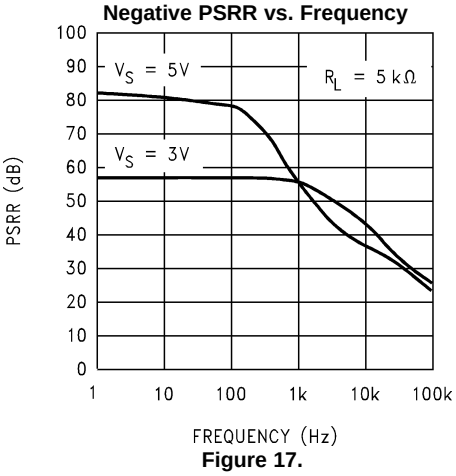


Figure 17.

CMRR vs. Frequency

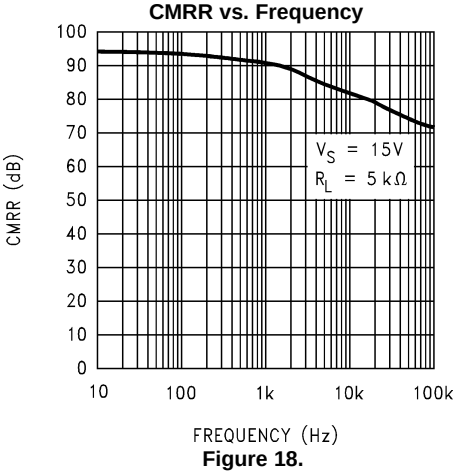


Figure 18.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

CMRR vs. Input Voltage

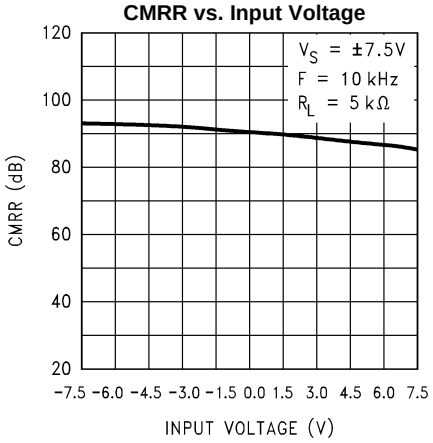


Figure 19.

CMRR vs. Input Voltage

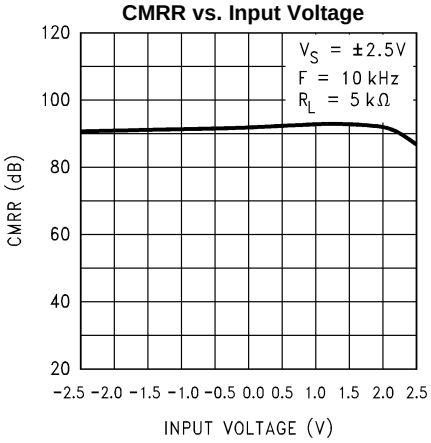


Figure 20.

CMRR vs. Input Voltage

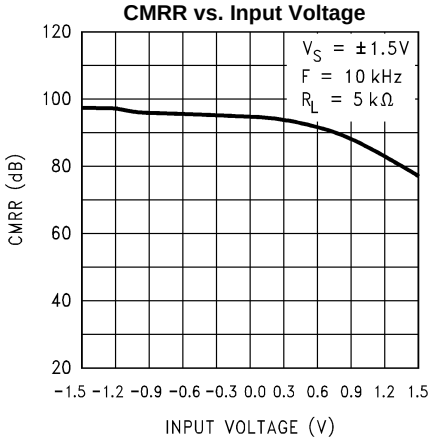


Figure 21.

ΔV_{OS} vs. CMR

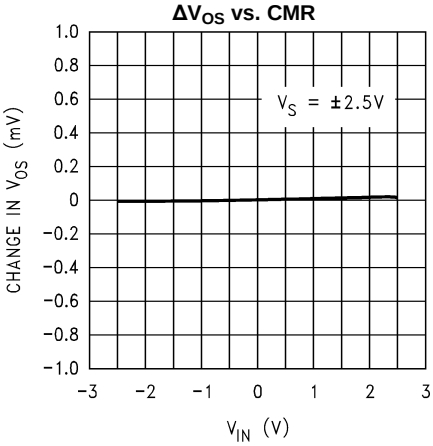


Figure 22.

ΔV_{OS} vs. CMR

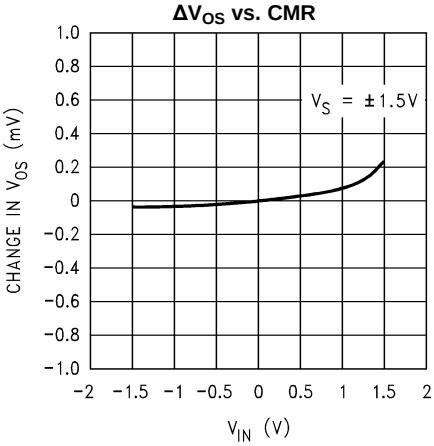


Figure 23.

Input Voltage vs. Output Voltage

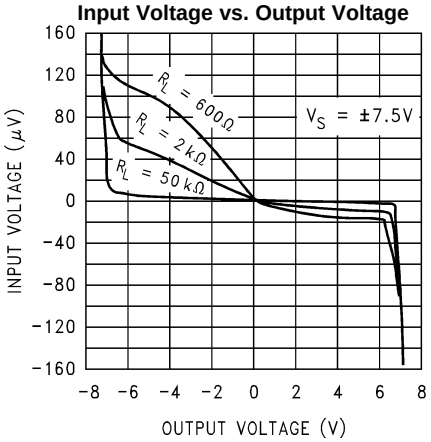


Figure 24.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage vs. Output Voltage

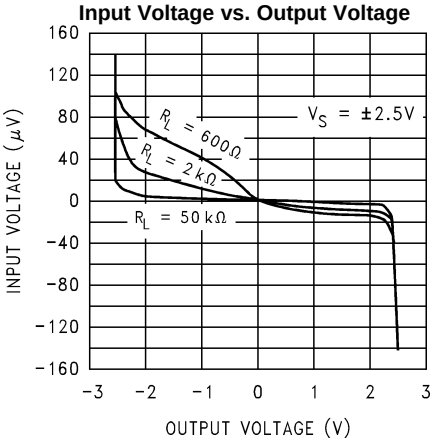


Figure 25.

Open Loop Frequency Response

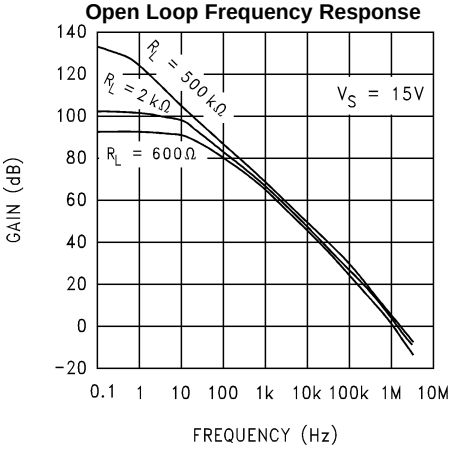


Figure 26.

Open Loop Frequency Response

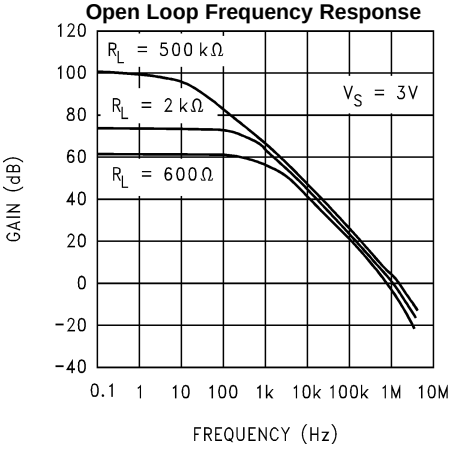


Figure 27.

Open Loop Frequency Response vs. Temperature

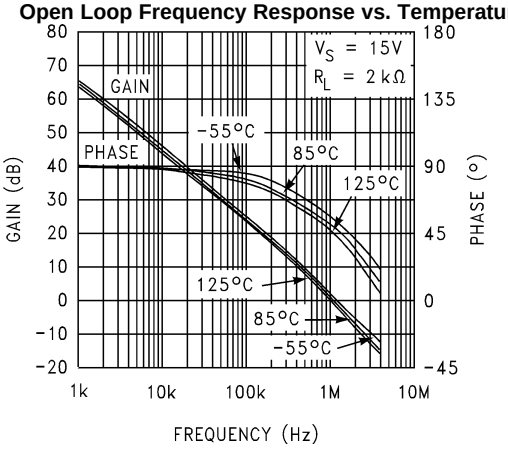


Figure 28.

Maximum Output Swing vs. Frequency

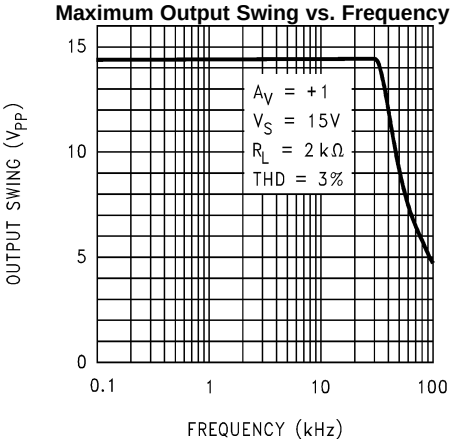


Figure 29.

Gain and Phase vs. Capacitive Load

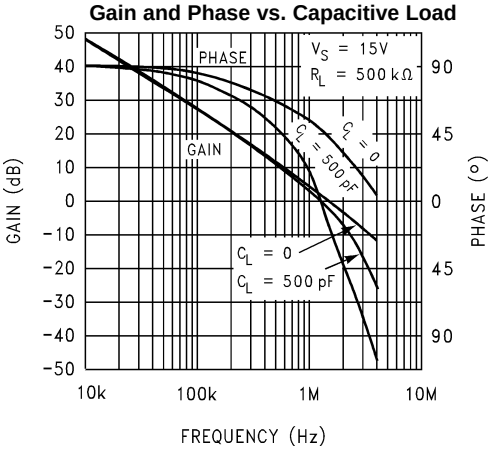


Figure 30.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Gain and Phase vs. Capacitive Load

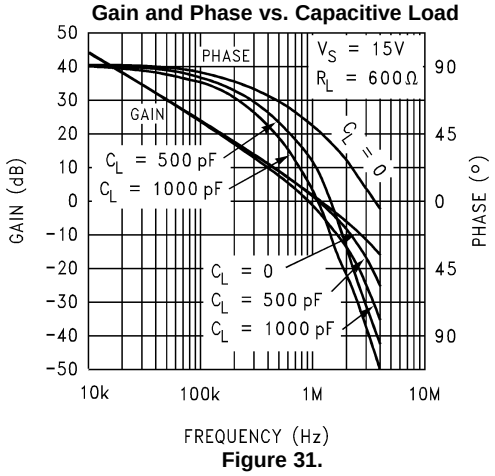


Figure 31.

Open Loop Output Impedance vs. Frequency

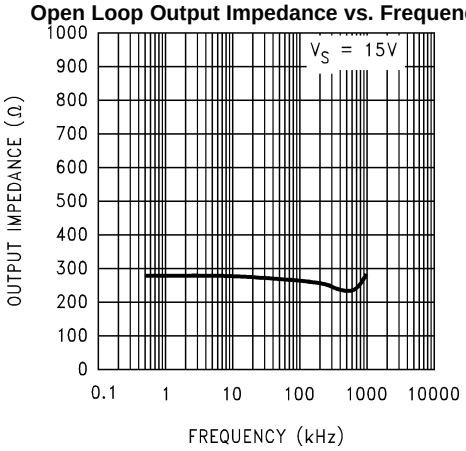


Figure 32.

Open Loop Output Impedance vs. Frequency

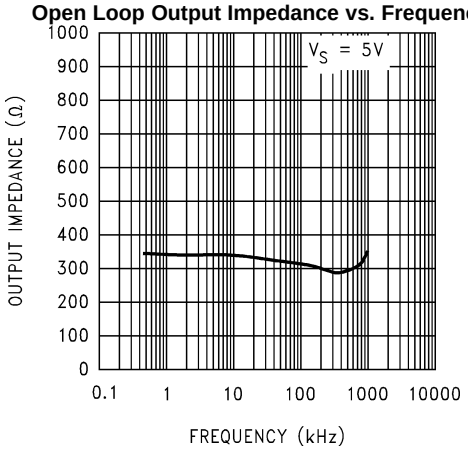


Figure 33.

Slew Rate vs. Supply Voltage

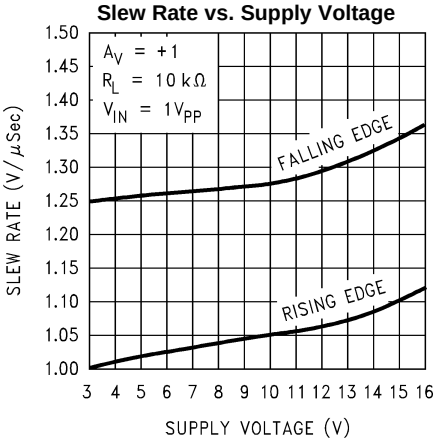


Figure 34.

Non-Inverting Large Signal Pulse Response

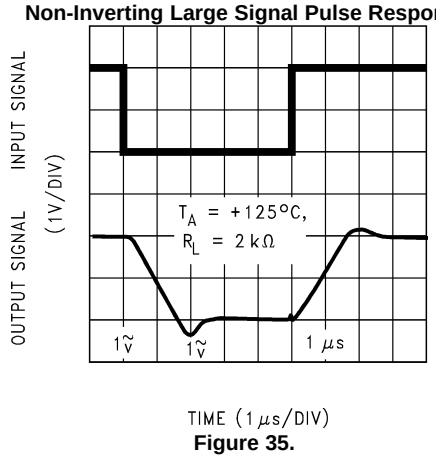


Figure 35.

Non-Inverting Large Signal Pulse Response

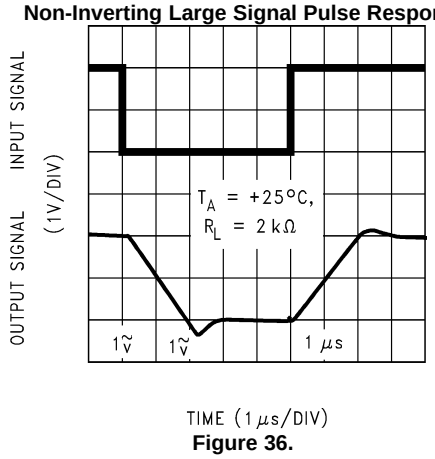


Figure 36.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Non-Inverting Large Signal Pulse Response

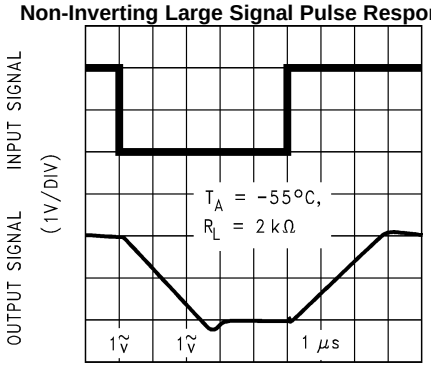


Figure 37.

Non-Inverting Small Signal Pulse Response

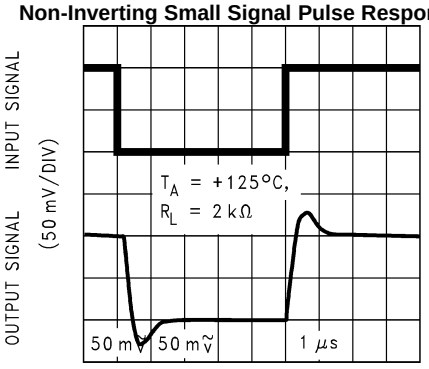


Figure 38.

Non-Inverting Small Signal Pulse Response

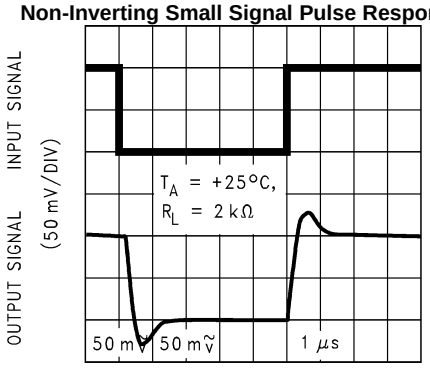


Figure 39.

Non-Inverting Small Signal Pulse Response

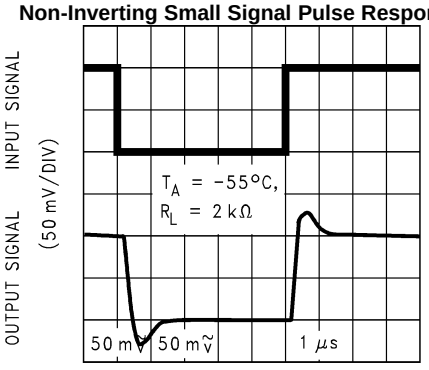


Figure 40.

Inverting Large Signal Pulse Response

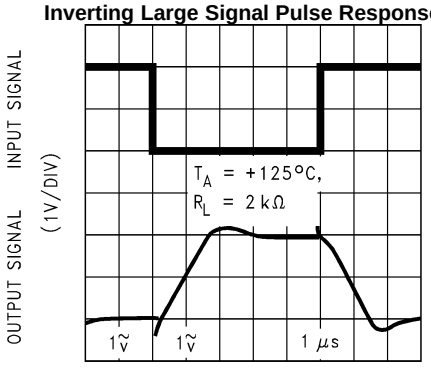


Figure 41.

Inverting Large Signal Pulse Response

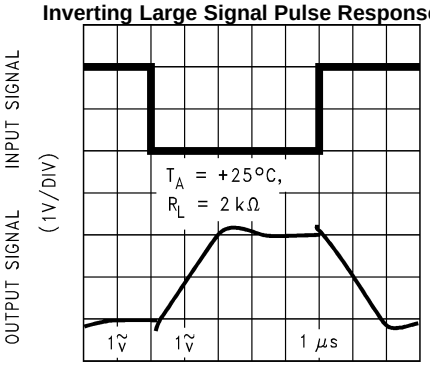


Figure 42.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Inverting Large Signal Pulse Response

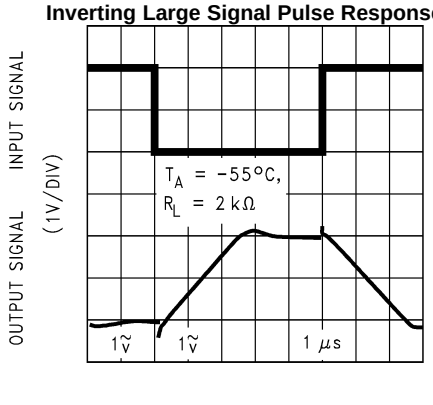


Figure 43.

Inverting Small Signal Pulse Response

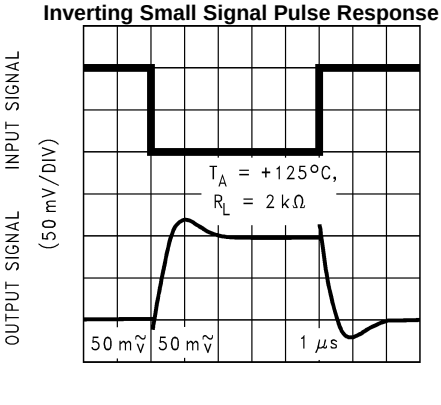


Figure 44.

Inverting Small Signal Pulse Response

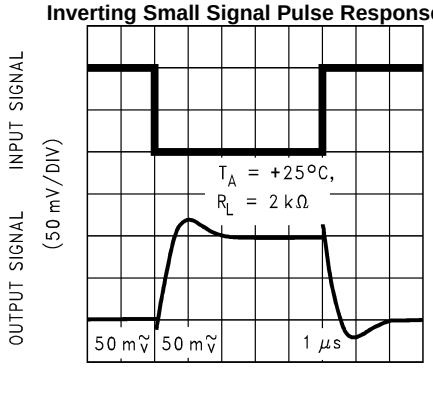


Figure 45.

Inverting Small Signal Pulse Response

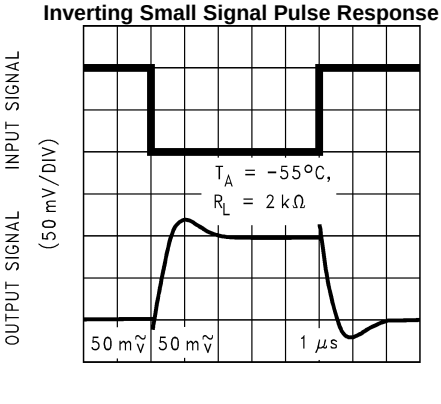


Figure 46.

Stability vs. Capacitive Load

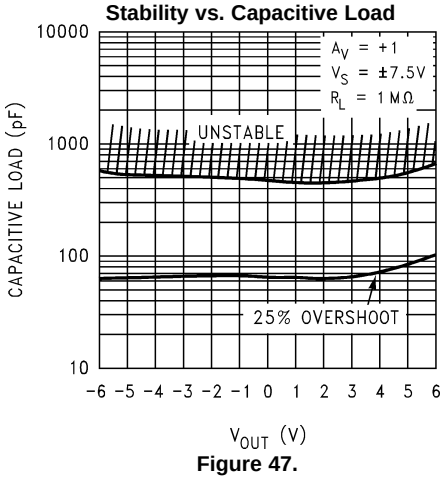


Figure 47.

Stability vs. Capacitive Load

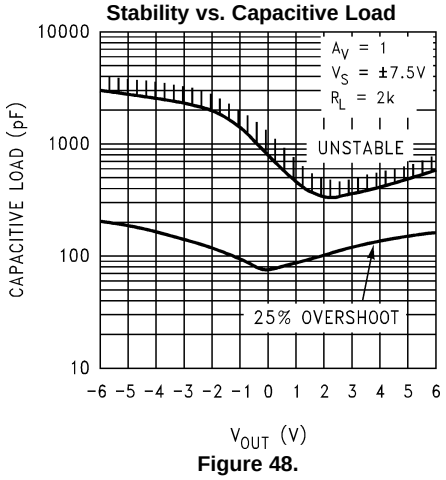


Figure 48.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Stability vs. Capacitive Load

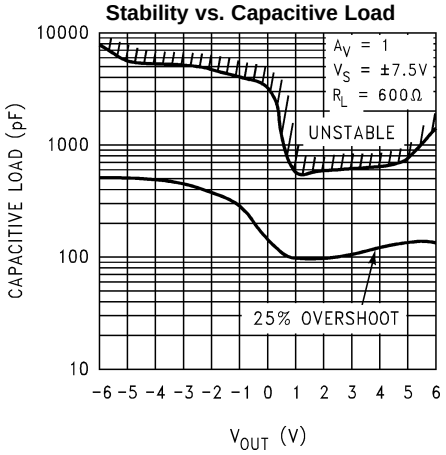


Figure 49.

Stability vs. Capacitive Load

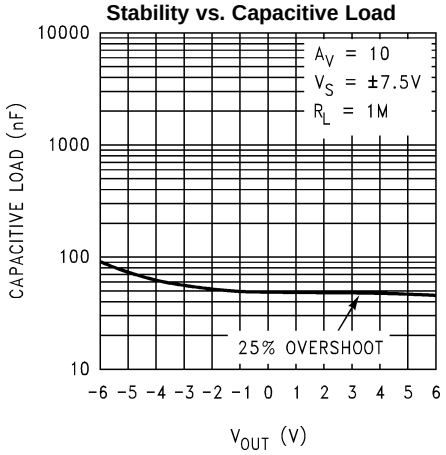


Figure 50.

Stability vs. Capacitive Load

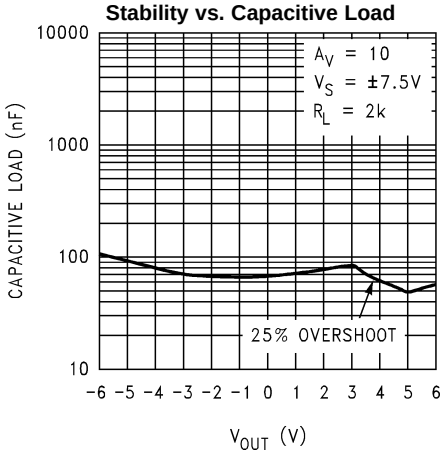


Figure 51.

Stability vs. Capacitive Load

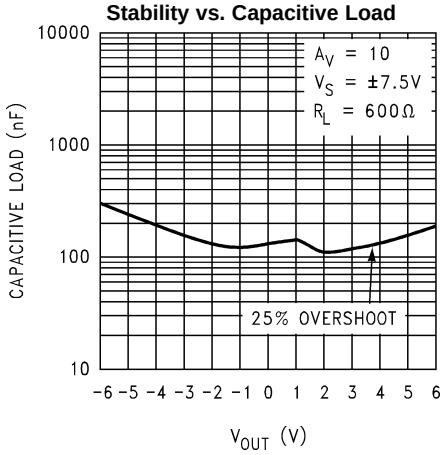


Figure 52.

APPLICATION INFORMATION

AMPLIFIER TOPOLOGY

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

INPUT COMMON-MODE VOLTAGE RANGE

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 53 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

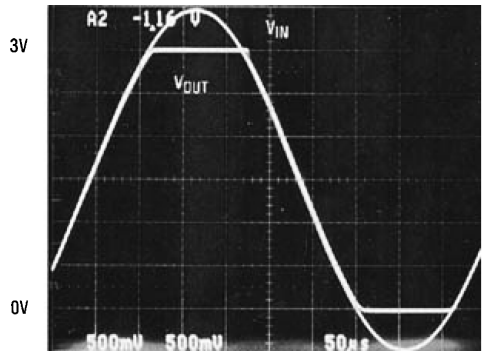


Figure 53. An Input Voltage Signal Exceeds the LMC6482 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 54, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

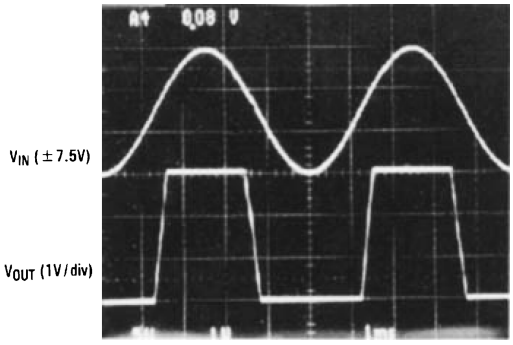


Figure 54. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in Figure 55 Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor (R_I) as shown in Figure 55.

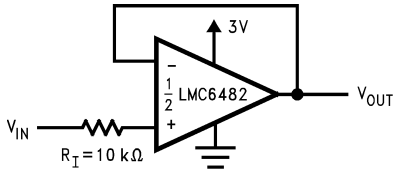


Figure 55. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

RAIL-TO-RAIL OUTPUT

The approximated output resistance of the LMC6482 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 80Ω sinking at Vs = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

CAPACITIVE LOAD TOLERANCE

The LMC6482 can typically directly drive a 100pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 56. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

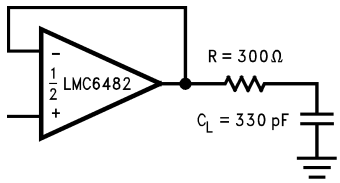


Figure 56. Resistive Isolation of a 330pF Capacitive Load

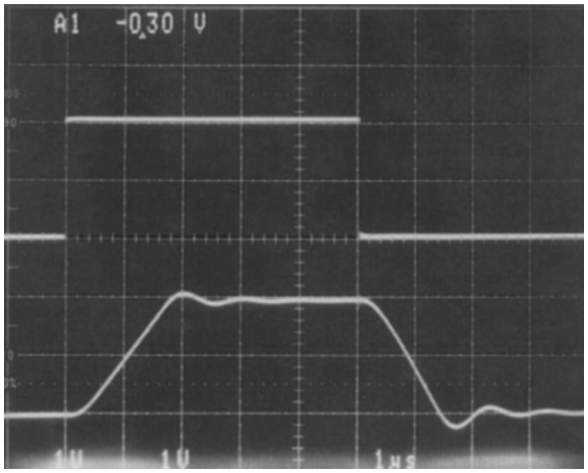


Figure 57. Pulse Response of the LMC6482 Circuit in Figure 56

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in Figure 58.

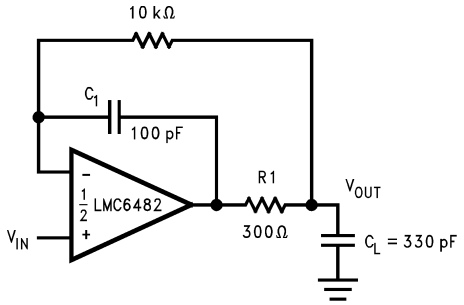


Figure 58. LMC6482 Noninverting Amplifier, Compensated to Handle a 330pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 59.

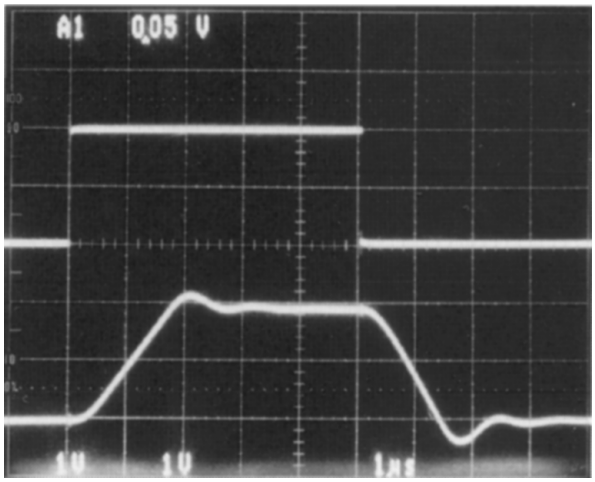


Figure 59. Pulse Response of LMC6482 Circuit in Figure 58

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

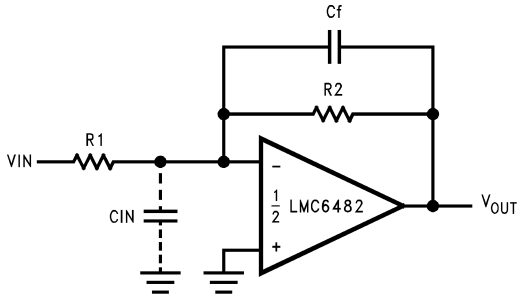


Figure 60. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 60), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_I \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 61. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05pA of leakage current. See Figure 62 for typical connections of guard rings for standard op-amp configurations.

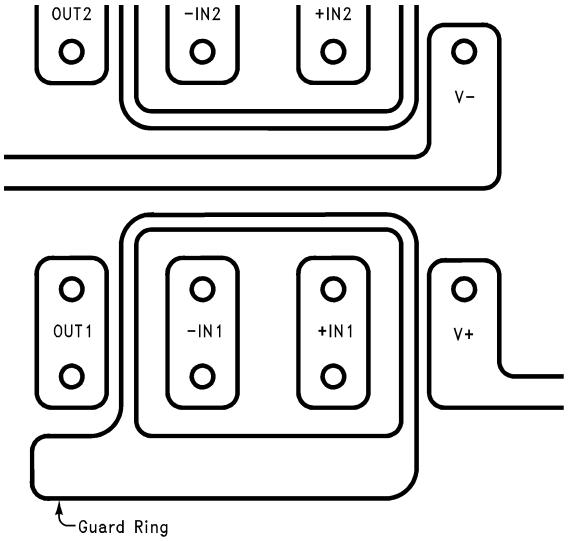


Figure 61. Example of Guard Ring in P.C. Board Layout

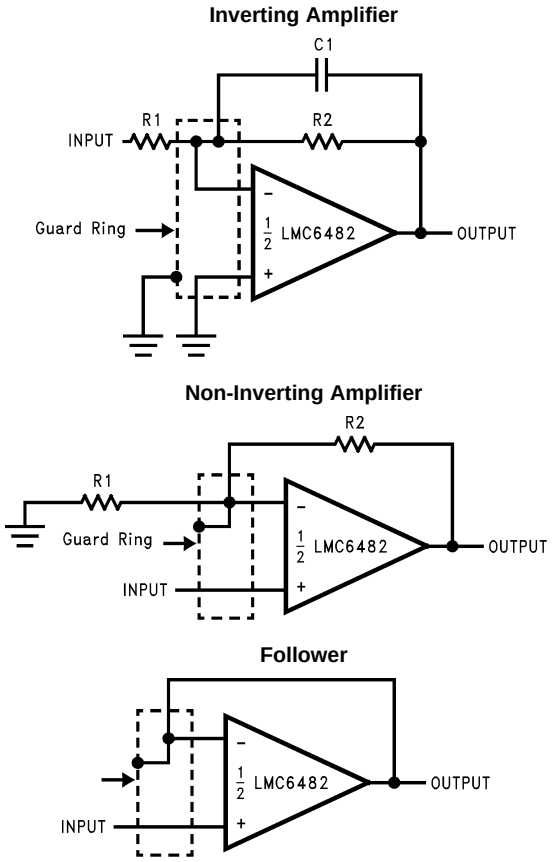
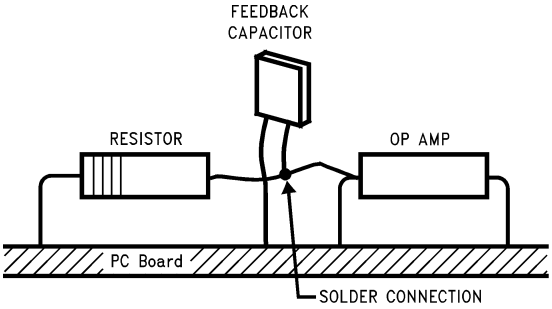


Figure 62. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 63.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 63. Air Wiring

OFFSET VOLTAGE ADJUSTMENT

Offset voltage adjustment circuits are illustrated in Figure 64 Figure 65. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

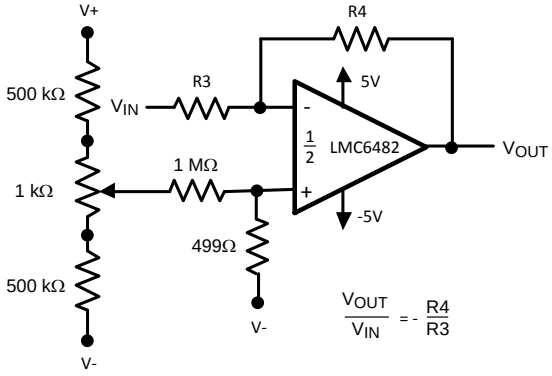


Figure 64. Inverting Configuration Offset Voltage Adjustment

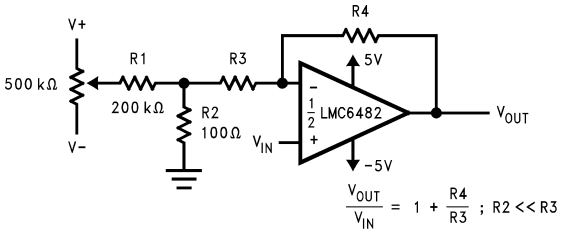


Figure 65. Non-Inverting Configuration Offset Voltage Adjustment

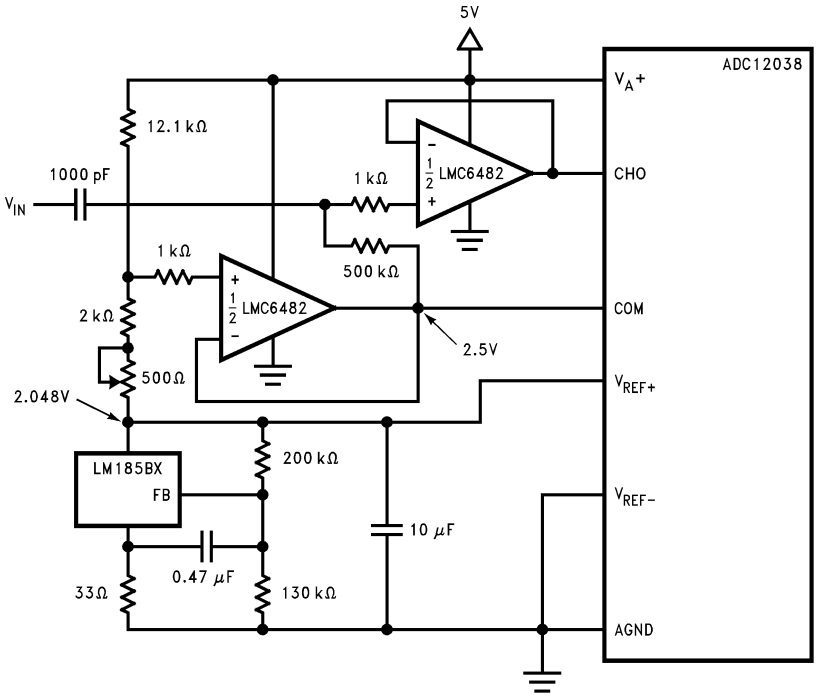
UPGRADING APPLICATIONS

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482's features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

DATA ACQUISITION SYSTEMS

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 66). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



Operating from the same Supply Voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy.

Figure 66. Buffering the ADC12038 with the LMC6482

INSTRUMENTATION CIRCUITS

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in Figure 67. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

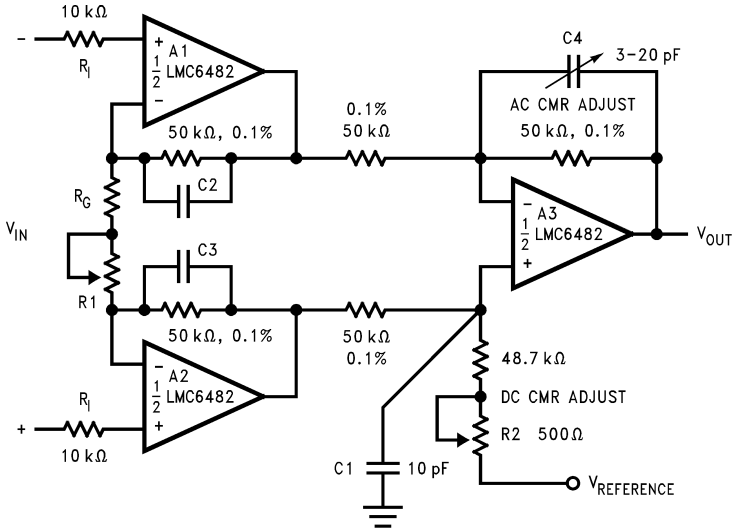


Figure 67. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 68. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

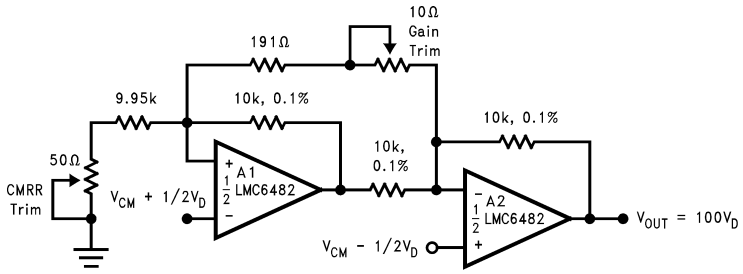


Figure 68. Low-Power Two-Op-Amp Instrumentation Amplifier

SPICE MACROMODEL

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

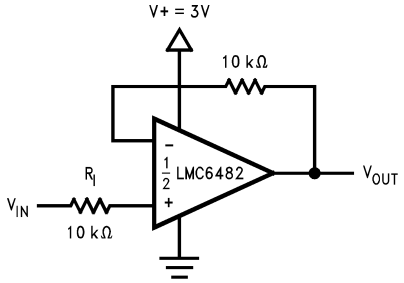


Figure 69. Half-Wave Rectifier with Input Current Protection (RI)

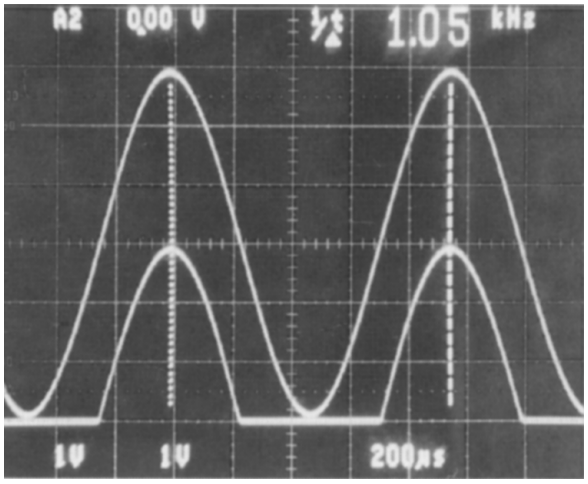


Figure 70. Half-Wave Rectifier Waveform

The circuit in Figure 69 uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 71.

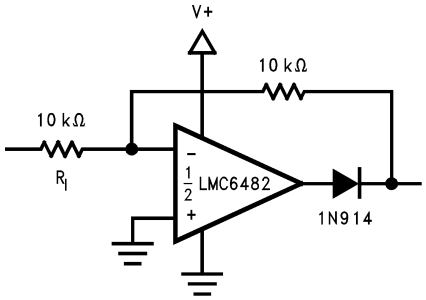


Figure 71. Full Wave Rectifier with Input Current Protection (R_I)

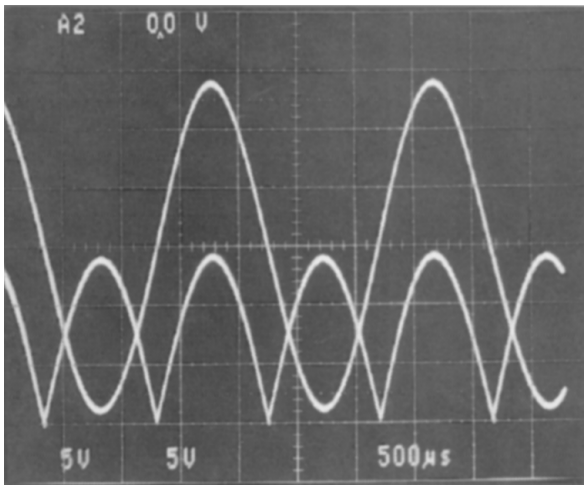


Figure 72. Full Wave Rectifier Waveform

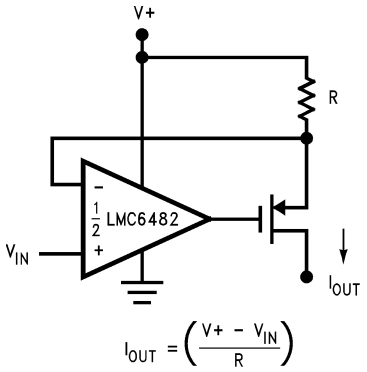


Figure 73. Large Compliance Range Current Source

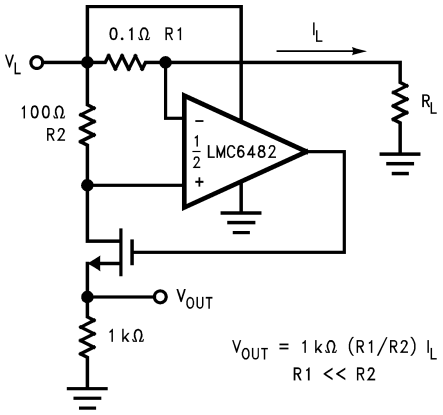


Figure 74. Positive Supply Current Sense

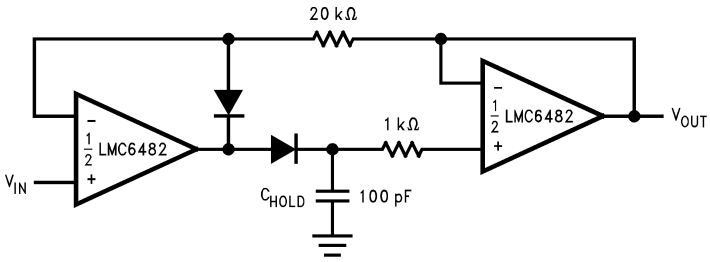


Figure 75. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In Figure 75 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

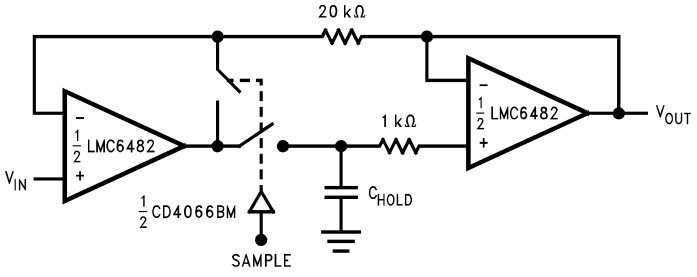
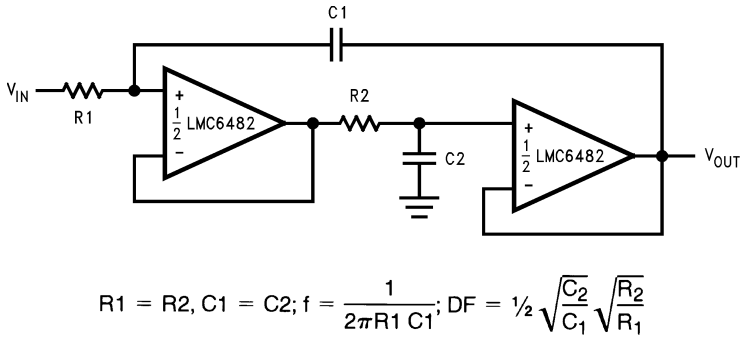


Figure 76. Rail-to-Rail Sample and Hold

The LMC6482's high CMRR (82dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



$$R1 = R2,\ C1 = C2;\ f = \frac{1}{2\pi R1\ C1};\ DF = \tfrac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

Figure 77. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in Figure 77 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

REVISION HISTORY

Released	Revision	Section	Changes
12/08/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. MNLMC6482AM-X Rev 0A0 will be archived.
03/27/2013	A	All	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9453401MPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Call TI	-55 to 125	LMC6482AMJ88 5962-94534 01MPA Q ACO 01MPA Q >T	Samples
LMC6482AMJ/883	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Call TI	-55 to 125	LMC6482AMJ88 5962-94534 01MPA Q ACO 01MPA Q >T	Samples
LMC6482M MD8	ACTIVE	DIESALE	Y	0	169	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

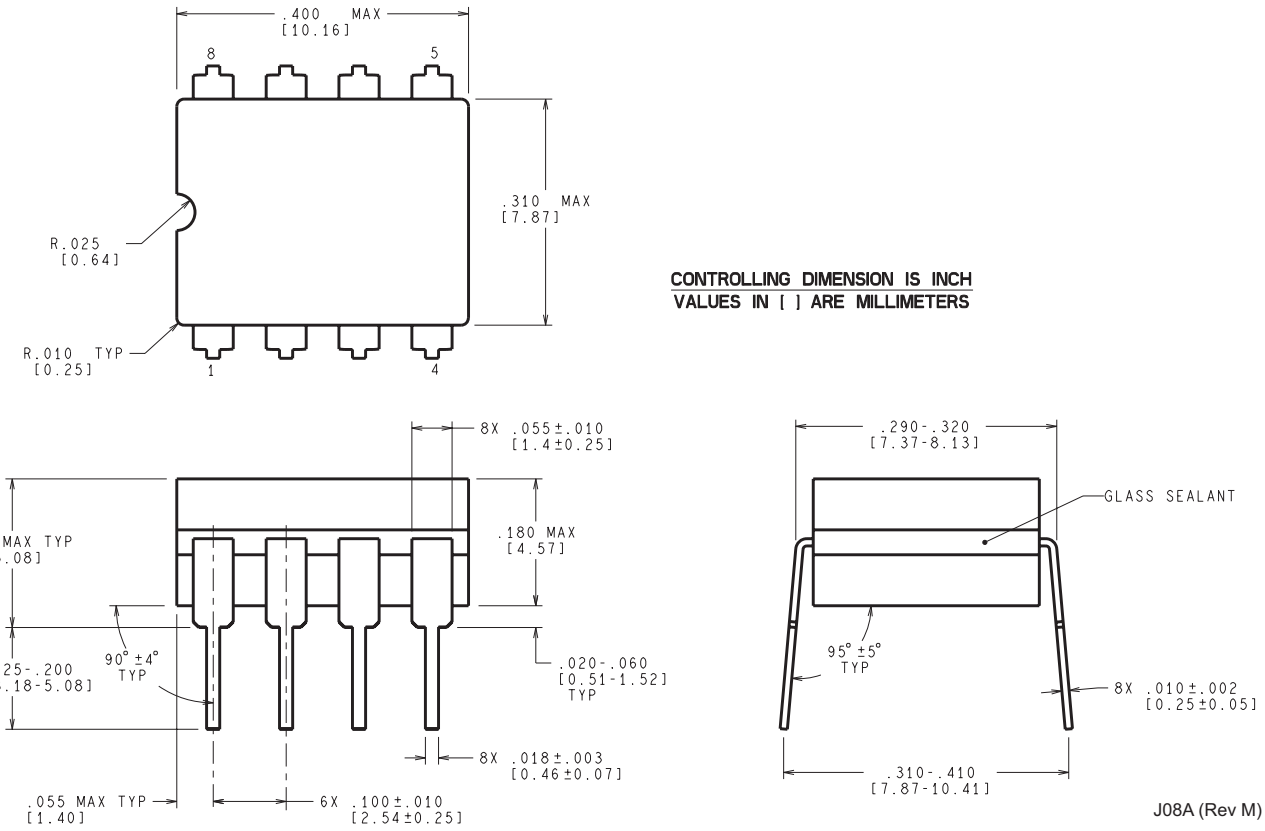
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265