National Semiconductor

ADVANCE INFORMATION
April 2007

LMH0340, LMH0040, LMH0070, LMH0050 3G, HD, SD, DVB-ASI SDI Serializer and Driver with LVDS Interface

General Description

The LMH0040 family of products provide a very simple 5:1 serializer and transmitter function, intended to be paired with an FPGA host which will format the data appropriately such that the output of the LMH0040 will be compliant with the output requirements of DVB-ASI, SMPTE 259M, and SMPTE 292M. The LMH0340 adds support for SMPTE 424M, the LMH0070 supports 270 Mbps operation only, and the LMH0050 requires an external cable driver. Throughout this document, if not explicitly stated, when the LMH0040 is referred to this includes all members of the family. The interface between the LMH0040 and the FPGA consists of a 5 bit wide LVDS bus, an LVDS clock and an SMBus interface. The product is packaged in a physically small 48 pin LLP package.

Key Specifications

- Output compliant with SMPTE 424M, SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Typical power dissipation: 420 mW
- Typical output jitter <53 ps (HD, 3G)

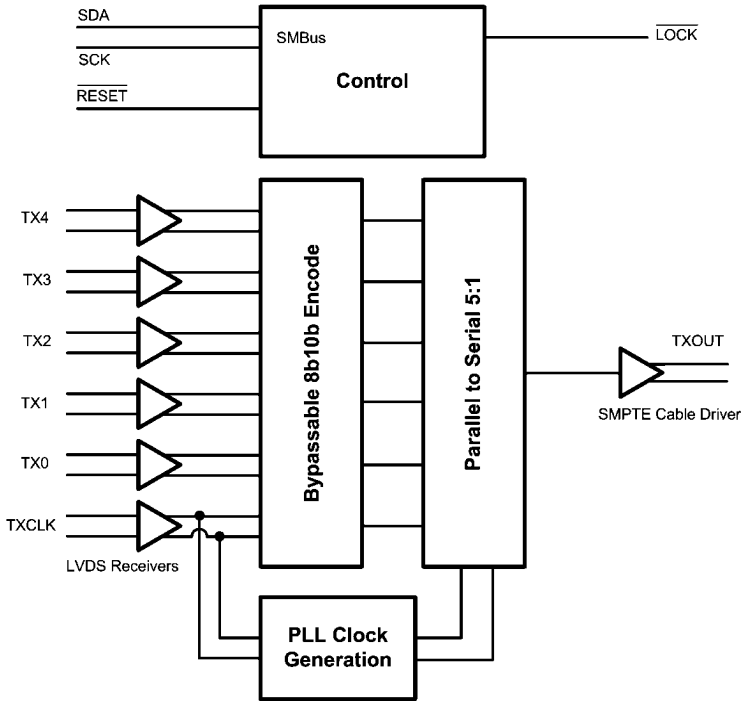
Features

- LVDS Interface
- No external VCO or clock required
- Integrated Variable output Cable Driver
- 3.3V SMBus configuration interface
- 48pin LLP package

Applications

- SDI interfaces for:
  - Video Cameras
  - DVRs
  - Video Switchers
  - Video Editing Systems

Block Diagram



LMH0340, LMH0040, LMH0070, LMH0050 3G, HD, SD, DVB-ASI SDI Serializer and Driver with LVDS Interface

TABLE 1. Feature Table

Device	SMPTE 424M Support	SMPTE 292M Support	SMPTE 259M Support	DVB-ASI Support	SMPTE Compliant cable driver
LMH0340	X	X	X	X	X
LMH0040		X	X	X	X
LMH0070			X	X	X
LMH0050		X	X	X	

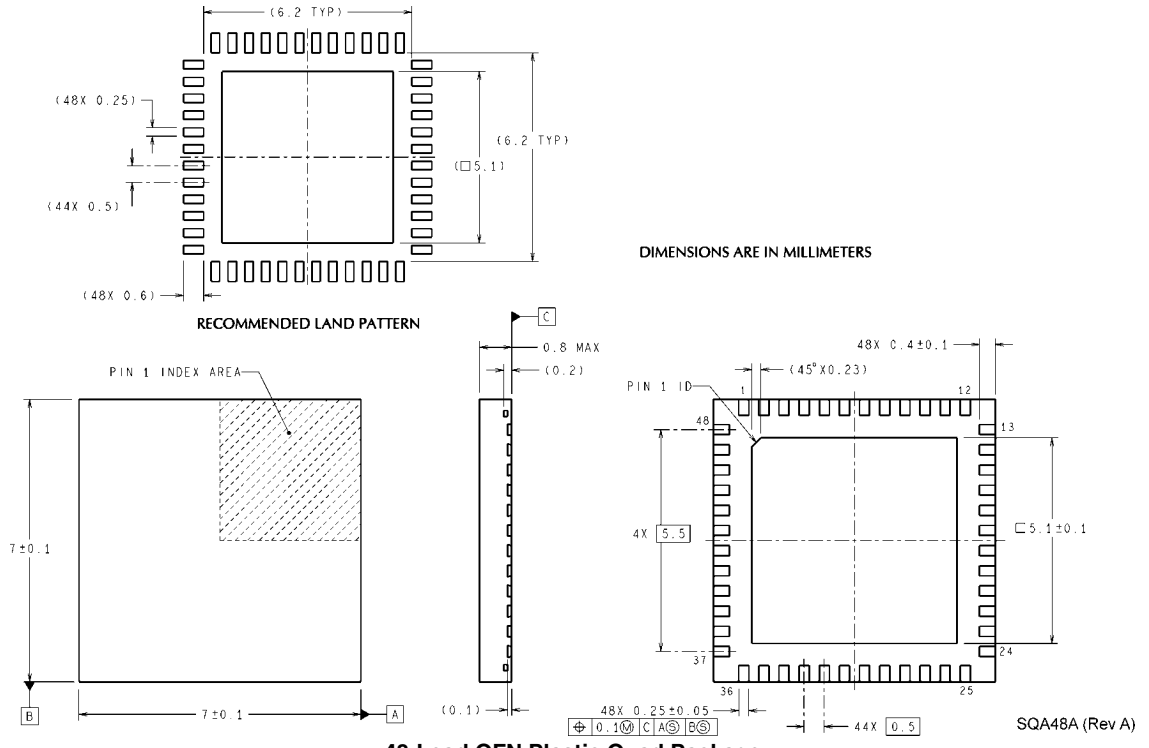
Device Operation

The LMH0040 serializer is used in digital video signal origination equipment. It is intended to be operated in conjunction with an FPGA host which preprocesses data for it, and then provides this data over the five bit wide datapath. Provided the host has properly formatted the data for the LMH0040, the output of the device will be compliant with DVB-ASI, SMPTE 259M-C, SMPTE 292M or SMPTE 424M depending upon the output mode selected.

DVB_ASI Mode

The LMH0040 has a special mode for DVB-ASI. In this mode, the input signal on TX4+/TX4- is treated as a data valid bit, if high, then the four bit nibbles from TX0–TX3 are taken to form an 8 bit word, which is then converted to a 10 bit code via an internal 8b10b encoder and this 10 bit word is serialized and driven on the output. The nibble taken in on the rising edge of the clock is the most significant nibble and the nibble taken in on the falling edge is the least significant nibble. If TX4+/TX4- is low, then the input on TX0–TX3 are ignored and the 10b idle character is inserted in the output stream.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead QFN Plastic Quad Package
NS Package Number LQA48A

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560