



# LMH1980

## Auto-Detecting SD/HD/PC Video Sync Separator

### General Description

The LMH1980 is an auto-detecting SD/HD/PC video sync separator ideal for use in a wide range of video applications, such as automotive LCD monitors, video capture & editing devices, surveillance & security equipment, and machine vision and inspection systems.

The LMH1980 accepts an analog video input signal with either bi-level or tri-level sync and automatically detects the video format, eliminating the need for external  $R_{SET}$  resistor adjustment required by other sync separators (e.g.: LM1881). The outputs provide timing signals in CMOS logic, including Composite, Horizontal, and Vertical Syncs, Burst/Back Porch Timing, and Odd/Even Field outputs. The  $\overline{HD}$  flag output (pin 5) provides a logic low signal only when a valid HD video input with tri-level sync is detected. The  $\overline{HD}$  flag can be used to disable an external switch-controlled SD chroma filter when HD video is detected, or enable it when SD video is detected. For non-standard video with bi-level sync and without vertical serration pulses, a default vertical sync pulse will be output and no horizontal sync pulses will be output during the vertical sync interval.

The LMH1980 is available in a space-saving 10-I<sub>d</sub>. Mini-SO Package (MSOP) and operates over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### Features

- Analog video sync separation for NTSC, PAL, 480I/P, 576I/P, 720P, 1080I/P/PsF, and many VESA-compatible timing formats
- Composite Video (CVBS), S-Video (Y/C), and Component Video ( $Y_{BPR}/GBR$ ) and PC Graphics (RGsB) interfaces
- SD/PC Bi-level sync & HD tri-level sync compatible
- Composite, Horizontal, and Vertical Sync outputs
- Burst/Back Porch Timing, Odd/Even Field, and HD Detect Flag outputs
- Automatic video format detection
- Fixed-level sync slicing for video inputs from 0.5 to 2  $V_{PP}$
- 3.3V to 5V supply operation

### Applications

- Consumer, Professional, Automotive & Industrial Video
- Video Capture, Editing, and Processing
- Genlock Circuits
- Surveillance & Security Video Systems
- Set-Top Boxes (STB) & Digital Video Recorders (DVR)
- LCD / Plasma Displays and Video Projectors
- Machine Vision and Inspection Systems
- Video Trigger Oscilloscopes and Waveform Monitors

### Connection Diagram

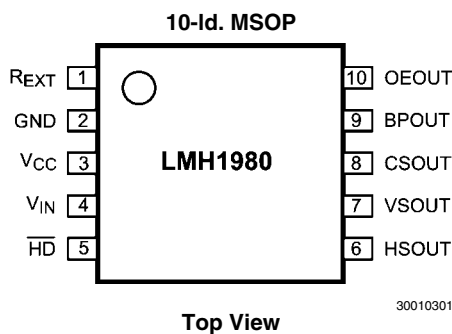


FIGURE 1. Pinout

### Pin Descriptions

Pin No.	Pin Name	Pin Description
1	$R_{EXT}$	Bias Current External Resistor
2	GND	Ground
3	$V_{CC}$	Supply Voltage
4	$V_{IN}$	Analog Video Input
5	$\overline{HD}$	HD Detect Flag Output
6	HSOUT	Horizontal Sync Output
7	VSOUT	Vertical Sync Output
8	CSOUT	Composite Sync Output
9	BPOUT	Burst/Back Porch Timing Output
10	OEOUT	Odd/Even Field Output

### Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
10-I <sub>d</sub> . MSOP	LMH1980MM	AL4A	1k Units Tape and Reel	MUB10A
	LMH1980MMX		3.5k Units Tape and Reel	

**Absolute Maximum Ratings** (Notes 1, 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)

Human Body Model 3.5 kV

Machine Model 350V

Supply Voltage,  $V_{CC}$  0V to 5.5VVideo Input,  $V_{IN}$   $-0.3V$  to  $V_{CC} + 0.3V$ Storage Temperature Range  $-65^{\circ}C$  to  $+150^{\circ}C$ Lead Temperature (soldering 10 sec.)  $300^{\circ}C$ Junction Temperature,  $T_{JMAX}$ (Note 3)  $+150^{\circ}C$ Thermal Resistance,  $\theta_{JA}$  (no airflow)  $120^{\circ}C/W$ **Operating Ratings** (Note 1)Temperature Range (Note 3)  $-40^{\circ}C$  to  $+85^{\circ}C$  $V_{CC}$  3.3V  $-10\%$  to 5V  $+10\%$ Input Amplitude,  $V_{IN-AMPL}$  140 mV to  $V_{CC} - V_{IN-CLAMP}$ **Electrical Characteristics** (Note 4)

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^{\circ}C$ ,  $V_{CC} = 3.3V$ ,  $R_{EXT} = 10\text{ k}\Omega$  1%,  $R_L = 10\text{ k}\Omega$ ,  $C_L < 10\text{ pF}$ .

**Boldface** limits apply at the temperature extremes. See Figure 2 for Test Circuit.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$I_{CC}$	Supply Current	No input signal	$V_{CC} = 3.3V$	10.5	12.5	mA
			$V_{CC} = 5V$	12.0	14.0	
<b>Video Input Specifications</b>						
$V_{IN-SYNC}$	Input Sync Amplitude	Amplitude from negative sync tip to video blanking level for SD/EDTV bi-level sync (Notes 8, 9)	0.14	0.30	0.60	$V_{PP}$
		Amplitude from negative to positive sync tips for HDTV tri-level sync (Notes 8, 10)	0.30	0.60	1.20	
$V_{IN-CLAMP}$	Input Sync Tip Clamp Level			0.7		V
$V_{IN-SLICE}$	Input Sync Slice Level	Slicing level above $V_{IN-CLAMP}$		70		mV
<b>Logic Output Specifications</b> (Note 12)						
$V_{OL}$	Output Logic 0	See output load conditions above	$V_{CC} = 3.3V$		0.3	V
			$V_{CC} = 5V$		0.5	
$V_{OH}$	Output Logic 1	See output load conditions above	$V_{CC} = 3.3V$	3.0		V
			$V_{CC} = 5V$	4.5		
$T_{SYNC-LOCK}$	Sync Lock Time	Time for the output signals to be correct after the video signal settles at $V_{IN}$ following a significant input change. See Start-Up Time section for more information		2		V periods
$T_{VSOUT}$	Vertical Sync Output Pulse Width	Serration Pulses in the Vertical Interval. See Figures 3, 4, 5, 6, 7, 8 for SDTV, EDTV & HDTV Vertical Interval Timing		3		H periods

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

**Note 2:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

**Note 3:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.

**Note 4:** Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .

**Note 5:** Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

**Note 6:** Limits are 100% production tested at  $25^{\circ}C$ . Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

**Note 7:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 8:**  $V_{IN-AMPL}$  plus  $V_{IN-CLAMP}$  should not exceed  $V_{CC}$ .

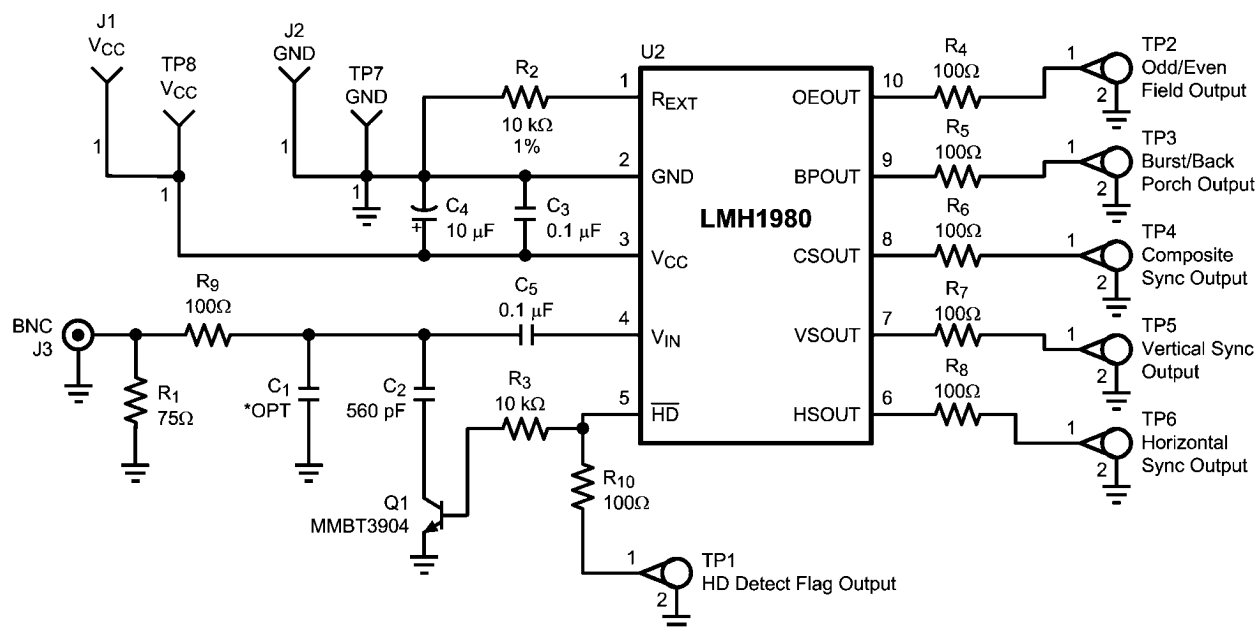
**Note 9:** Tested with 480I signal.

**Note 10:** Tested with 1080P signal.

**Note 11:** Maximum voltage offset (DC bounce) between 2 consecutive input sync tips must be less than 25 mV<sub>pp</sub>; otherwise, this may cause incorrect output signals to occur.

**Note 12:** Outputs are negative-polarity logic signals, except for Odd/Even Field.

## LMH1980 Test Circuit

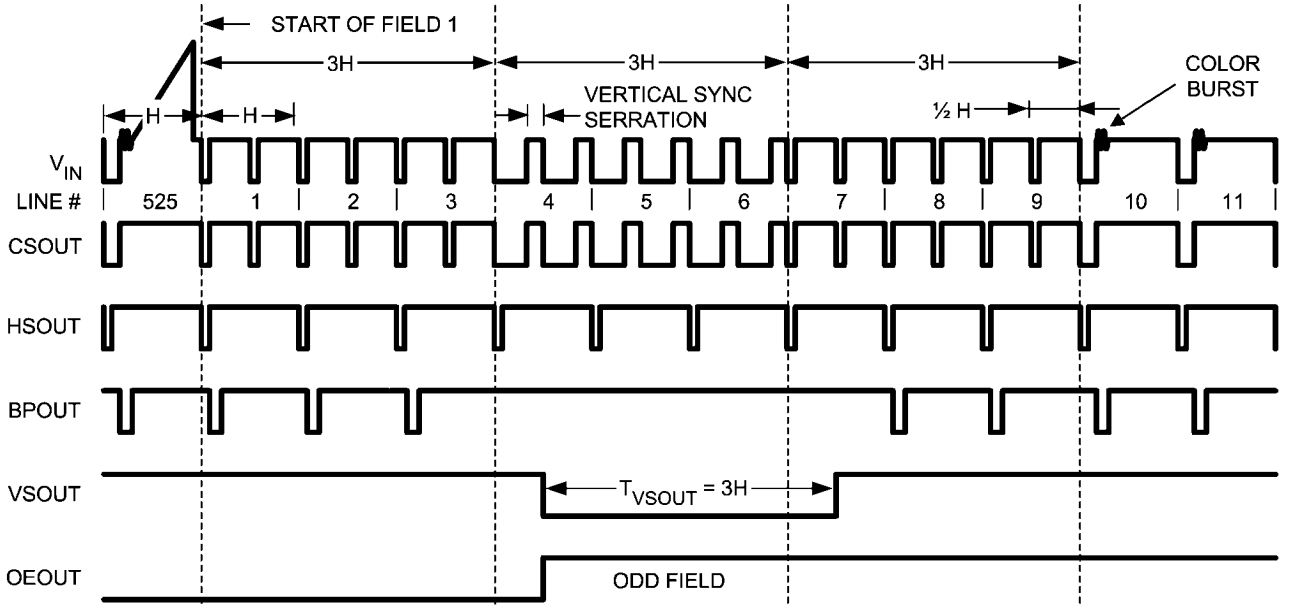


30010302

FIGURE 2. Test Circuit

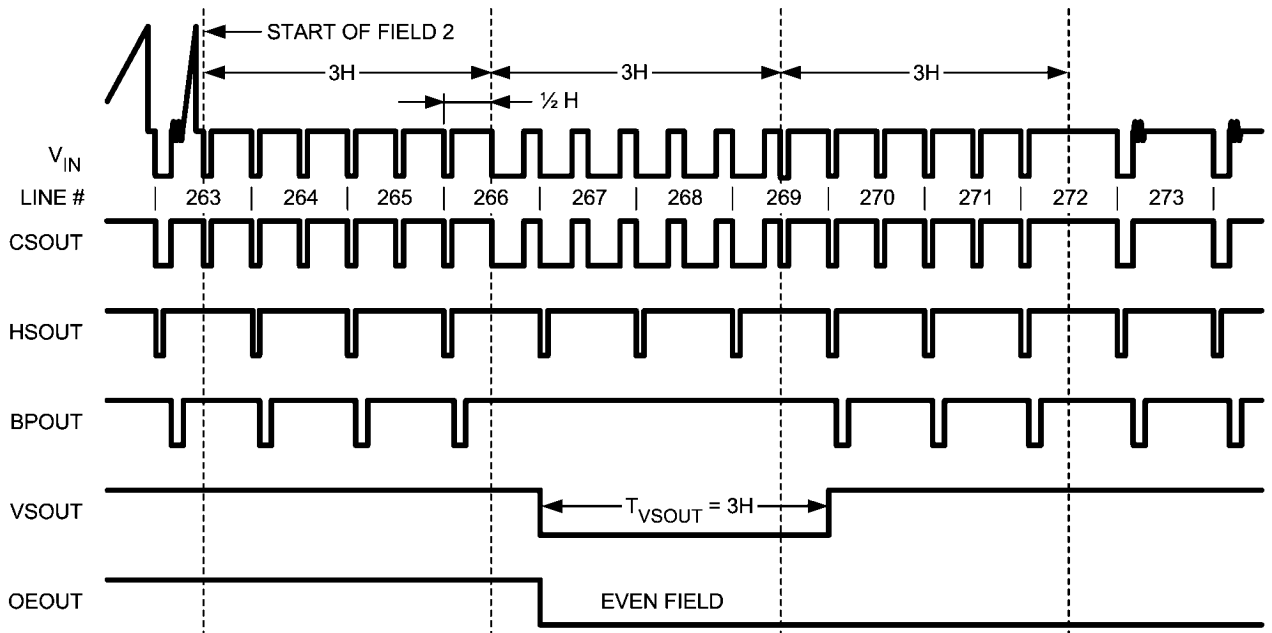
The LMH1980 test circuit is shown in *Figure 2*. The video generator should provide a clean, low-noise video input signal with minimal sync pulse overshoot over 75Ω coaxial cable, which should be impedance-matched with a 75Ω load termination resistor to prevent unwanted signal distortion. The output waveforms should be monitored using a low-capacitance probe on an oscilloscope with at least 500 MHz bandwidth. See the PCB LAYOUT CONSIDERATIONS section for more information about signal and supply trace routing and component placement. Also, refer to the “LMH1980 Evaluation Board Instruction Manual” Application Note (AN-1618).

### SDTV Vertical Interval Timing Diagrams (NTSC, PAL, 480I, 576I)



30010303

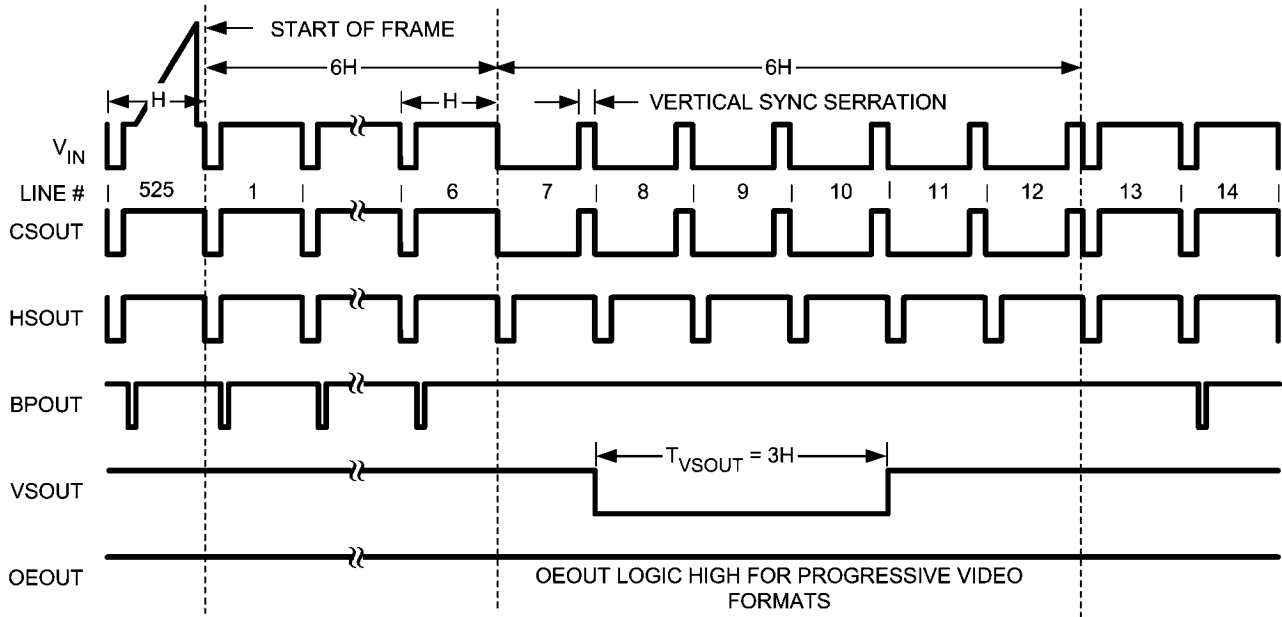
FIGURE 3. NTSC Odd Field Vertical Interval



30010304

FIGURE 4. NTSC Even Field Vertical Interval

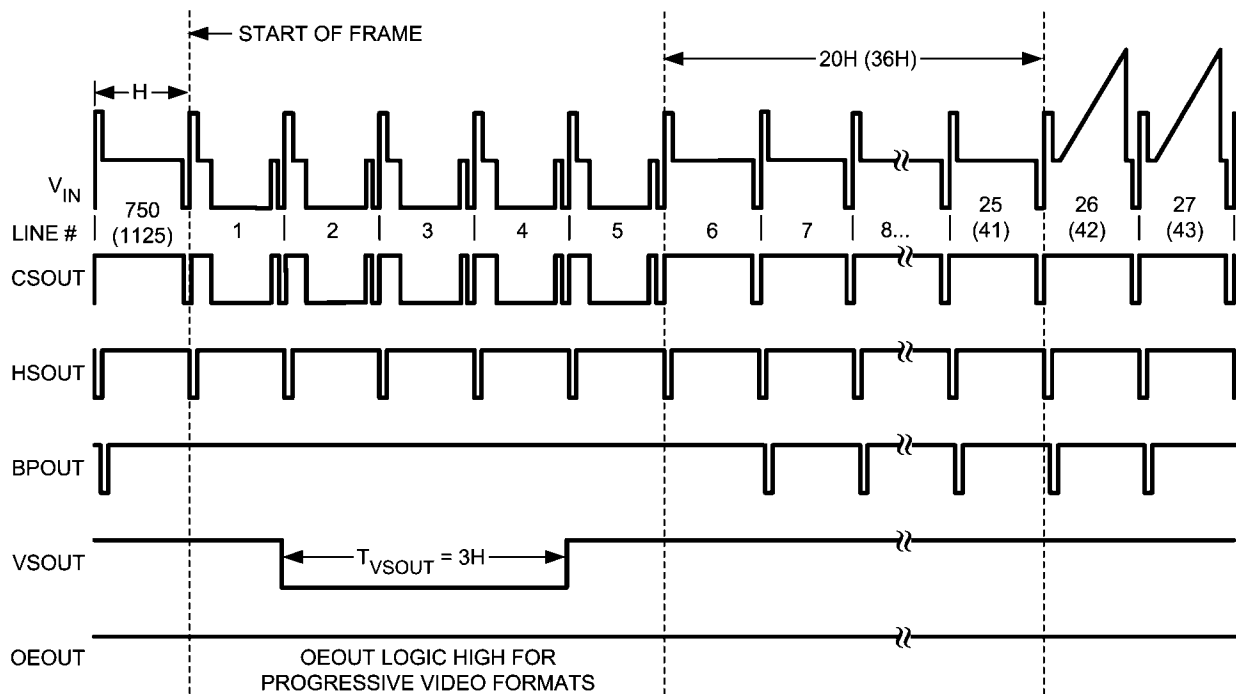
### EDTV Vertical Interval Timing Diagram (480P, 576P)



30010305

FIGURE 5. 480P Vertical Interval

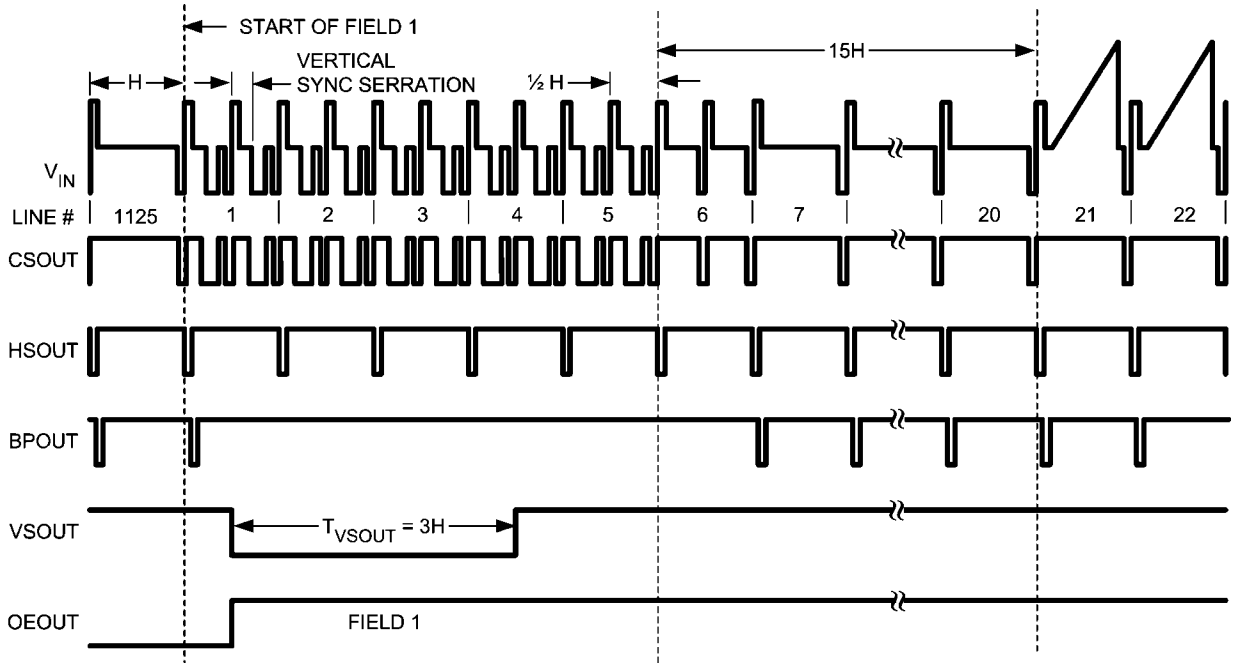
### HDTV Vertical Interval Timing Diagram (720P, 1080P)



30010314

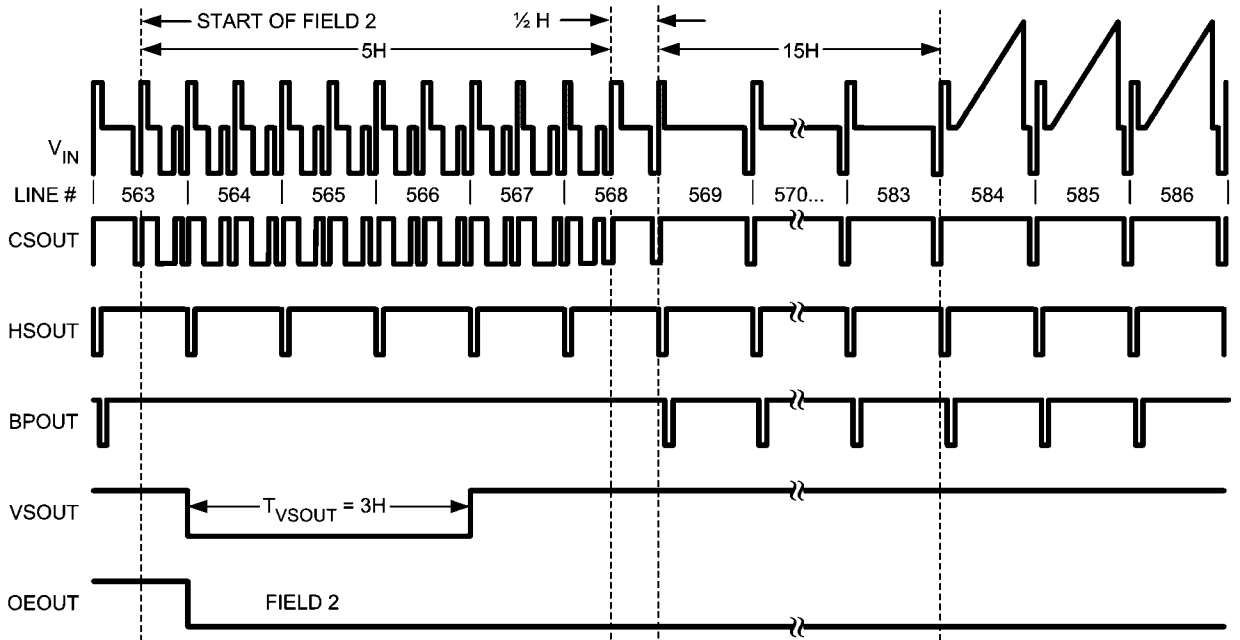
FIGURE 6. 720P (1080P) Vertical Interval

# HDTV Vertical Interval Timing Diagrams (1080I)



30010306

FIGURE 7. 1080I Field 1 Vertical Interval



30010307

FIGURE 8. 1080I Field 2 Vertical Interval

## SD/EDTV Horizontal Interval Timing Diagram

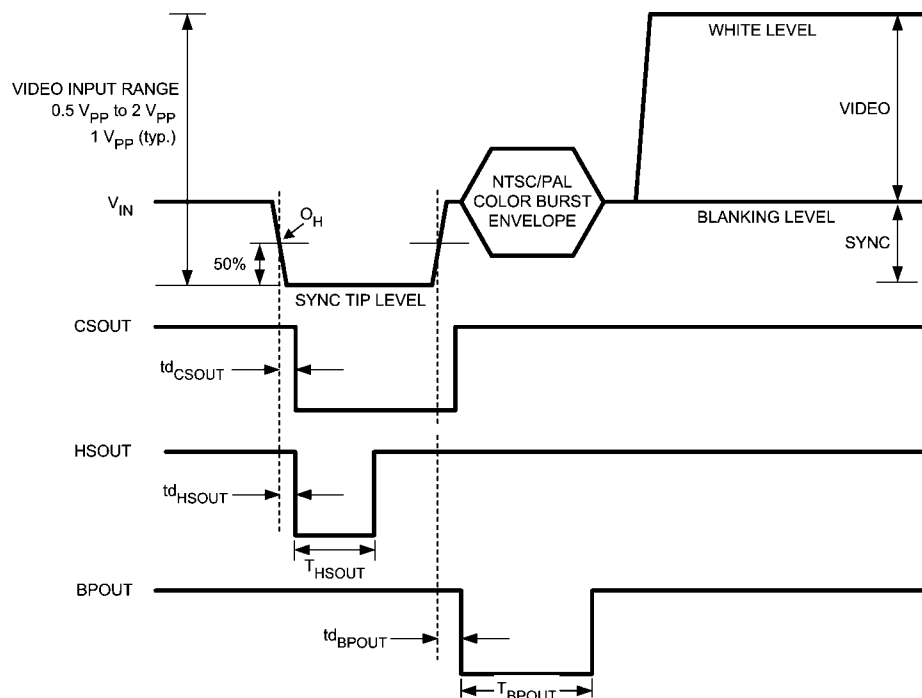


FIGURE 9. SD/EDTV Horizontal Interval with Bi-level Sync

### SDTV Horizontal Interval Timing Characteristics

$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ , No Input Filter, PAL Video Input from Tek TG700 Generator with AVG7 SD video module

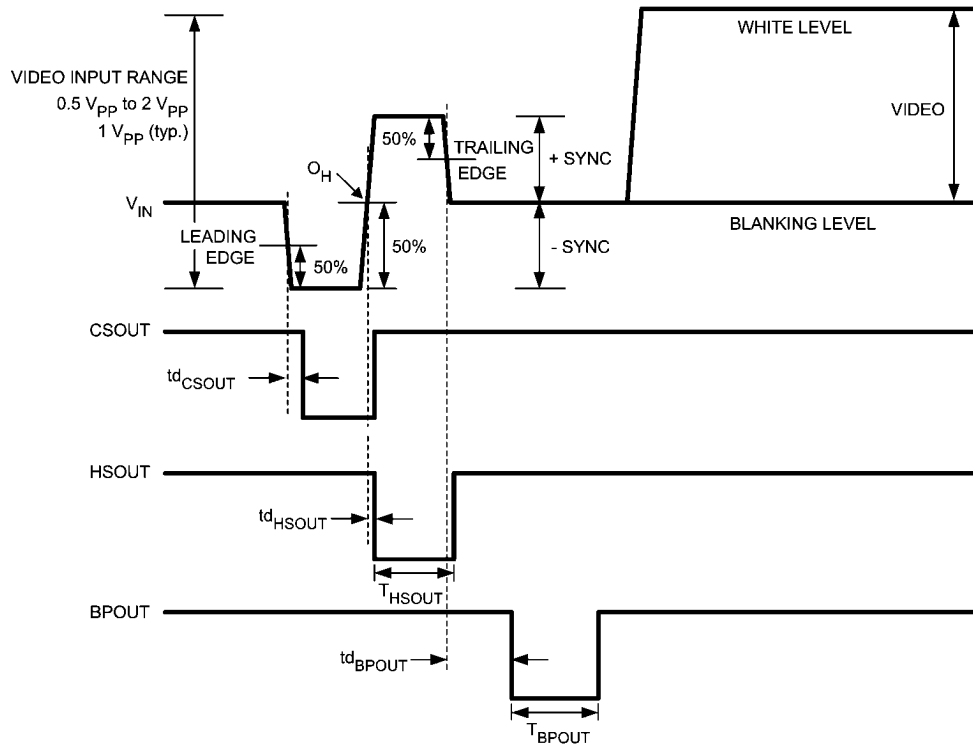
Symbol	Parameter	Conditions	Typ	Units
$t_{d_{CSOUT}}$	Composite Sync Output Propagation Delay from Input Sync Reference ( $O_H$ )	See Figure 9	525	ns
$t_{d_{HSOUT}}$	Horizontal Sync Output Propagation Delay from Input Sync Reference ( $O_H$ )	See Figure 9	530	ns
$t_{d_{BPOUT}}$	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9	400	ns
$T_{HSOUT}$	Horizontal Sync Output Pulse Width	See Figure 9	2.5	$\mu s$
$T_{BPOUT}$	Burst/Back Porch Timing Output Pulse Width	See Figure 9	3.0	$\mu s$

### EDTV Horizontal Interval Timing Characteristics

$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ , No Input Filter, 576P Video Input from Tek TG700 Generator with AVG7 SD module

Symbol	Parameter	Conditions	Typ	Units
$t_{d_{CSOUT}}$	Composite Sync Output Propagation Delay from Input Sync Reference ( $O_H$ )	See Figure 9	170	ns
$t_{d_{HSOUT}}$	Horizontal Sync Output Propagation Delay from Input Sync Reference ( $O_H$ )	See Figure 9	175	ns
$t_{d_{BPOUT}}$	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9	485	ns
$T_{HSOUT}$	Horizontal Sync Output Pulse Width	See Figure 9	2.3	$\mu s$
$T_{BPOUT}$	Burst/Back Porch Timing Output Pulse Width	See Figure 9	350	ns

# HDTV Horizontal Interval Timing Diagram



30010309

FIGURE 10. HDTV Horizontal Interval with Tri-level Sync

## HDTV Horizontal Interval Timing Characteristics

$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ , No Input Filter, 1080I Video Input from Tek TG700 Generator with AWVG7 HD module

Symbol	Parameter	Conditions	Typ	Units
$t_{d_{CSOUT}}$	Composite Sync Output Propagation Delay from Input Sync Leading Edge	See Figure 10	150	ns
$t_{d_{HSOUT}}$	Horizontal Sync Output Propagation Delay from Input Sync Reference ( $O_H$ )	See Figure 10	60	ns
$t_{d_{BPOUT}}$	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 10	450	ns
$T_{HSOUT}$	Horizontal Sync Output Pulse Width	See Figure 10	525	ns
$T_{BPOUT}$	Burst/Back Porch Timing Output Pulse Width	See Figure 10	350	ns



## Application Information

### GENERAL DESCRIPTION

The LMH1980 is designed to extract the timing information from various video formats with standard and non-standard vertical serration and output the syncs and relevant timing signals in CMOS logic. Its advanced features and easy application make it ideal for consumer, professional, and industrial video systems where sync timing needs to be extracted from SD, HD, and PC video signals. The device can operate from a supply voltage between 3.3V and 5V. The only required external components are bypass capacitors between the  $V_{CC}$  and GND pins, input coupling capacitor ( $C_{IN}$ ) from the signal source to the  $V_{IN}$  pin, and a fixed-value 1% precision resistor between the  $R_{EXT}$  and GND pins. Refer to the test circuit in *Figure 2*.

### $R_{EXT}$ Resistor

The precision external resistor ( $R_{EXT}$ ) establishes the internal bias current and precise reference voltage for the LMH1980. For optimal performance,  $R_{EXT}$  should be a 10 k $\Omega$  1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a  $R_{EXT}$  resistor with less precision may result in reduced performance (like worse performance, increased propagation delay variation, or reduced input sync amplitude range) against temperature, supply voltage, input signal, or part-to-part variations.

**Note:** The  $R_{EXT}$  resistor used with the LMH1980 serves a different function than the " $R_{SET}$  resistor" used with other previous sync separators, like the LM1881. For the LM1881, the  $R_{SET}$  value needed to be adjusted externally to support different input line rates. For the LMH1980, the  $R_{EXT}$  value is fixed, and the device automatically detects the input line rate to support various video formats without electrical or physical intervention.

### Automatic Format Detection and Switching

Automatic format detection eliminates the need for adjusting an external  $R_{SET}$  resistor or programming via a microcontroller. The device outputs will respond correctly to a switch in video format after a sufficient start-up time has been satisfied, usually within 1 to 2 fields of video. Unlike other sync separators, the LMH1980 does not require the power to be cycled in order to produce correct outputs after a significant change to the input signal. See the Start-up Time section for more details.

### Fixed-Level Sync Slicing

The LMH1980 uses fixed-level sync slicing for video inputs with an amplitude from  $0.5V_{PP}$  to  $2V_{PP}$ , which allows for proper sync separation even for improperly terminated or attenuated input signals. The fixed-level sync slicing threshold is nominally 70 mV above the clamped sync tip. This means that for a minimum video input signal amplitude of  $0.5V_{PP}$ , the slicing level is near the mid-point of the sync pulse amplitude. This slicing level is independent of the input signal amplitude; therefore, for a  $2V_{PP}$  input, the slicing level occurs at 12% of the sync pulse amplitude.

### INPUT CONSIDERATIONS

The LMH1980 supports sync separation for analog CVBS, Y (luma) from Y/C and  $Y_{PB}P_{R}$ , and G (sync on green) from GBR/RGsB, as specified in the following video standards.

- Composite Video (CVBS) and S-Video (Y/C):
  - SMPTE 170M (NTSC), ITU-R BT.470 (PAL)
- Component Video ( $Y_{PB}P_{R}$ /GBR):
  - SDTV: SMPTE 125M, SMPTE 267M, ITU-R BT.601 (480I, 576I)
  - EDTV: ITU-R BT.1358 (480P, 576P)
  - HDTV: SMPTE 296M (720P), SMPTE 274M (1080I/P), SMPTE RP 211 (1080PsF)
- PC Graphics (RGsB):
  - VESA Monitor Timing Standards and Guidelines Version 1.0, Revision 0.8
- Non-Standard Video:
  - Composite NTSC & PAL (or Component 480I & 576I) without vertical serration & equalization pulses (i.e.: from logical OR-ing of H & V signals)

### Input Termination

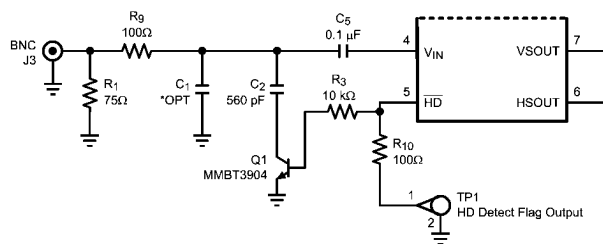
The video source should be load terminated with a 75 $\Omega$  resistor to ensure correct video signal amplitude and minimize signal distortion due to reflections. In extreme cases, the LMH1980 can handle non-terminated or double-terminated input conditions, assuming 1V<sub>PP</sub> signal amplitude for normally terminated video.

### Input Filtering

An external filter is recommended if the video signal has large chroma amplitude that extends near the sync tip and/or has considerable high-frequency noise, so they do not interfere with sync separation. A simple RC low-pass chroma filter with a series resistor ( $R_g$ ) and a filter capacitor ( $C_2$ ) to ground can be used to sufficiently attenuate chroma such that minimum peak of its amplitude is above the slicing level and also to improve the overall signal-to-noise ratio. To achieve the desired filter cutoff frequency, it's advised to vary  $C_2$  and keep  $R_g$  small (i.e.: 100 $\Omega$ ) to minimize sync tip clipping due to the voltage drop across  $R_g$ . Keep in mind that as the cutoff frequency decreases, the LMH1980 output propagation delays increase, which could affect the timing relationship between the sync and video signals.

In applications where the chroma filter needs to be disabled when HD video is input, it is possible to use a transistor switch (Q1) controlled by the  $\overline{HD}$  flag (pin 5) to open  $C_2$ 's connection to ground as shown in *Figure 11*. When a HD tri-level sync input signal is applied,  $\overline{HD}$  will output logic low (following a brief delay for auto format detection) and Q1 will turn off to disable the chroma filter, which is intended for SD composite video only. When a SD bi-level sync signal (i.e.: NTSC/PAL) is applied,  $\overline{HD}$  will output logic high and Q1 will turn on to enable the chroma filter.

**Important:** If the filter cutoff frequency ( $f_{CO}$ ) is set too low and HD video is applied, the filter can severely roll off and attenuate the input's high-bandwidth tri-level sync pulses such that the LMH1980 cannot detect a valid HD input signal. If the LMH1980 cannot detect a valid HD input, then the  $\overline{HD}$  flag will never change from logic high to low and the switch-controlled filter will never be disabled via Q1. In other words,  $f_{CO}$  should not be set too low that the filter impairs the LMH1980's ability to detect a valid HD input. The values of  $R_g$  and  $C_2$  shown in *Figure 11* give  $f_{CO}$ =2.79 MHz (about -4 dB at 3.58 MHz NTSC subcarrier frequency) without impairing HD video format detection.



30010318

**FIGURE 11. External Switch-Controlled Chroma Filter**

If a PC video input with bi-level sync is to be used,  $C_2$  should be removed to disable chroma filtering. This is necessary because  $\overline{HD}$  will output logic high (like in the SD video input case) and enable the filter. A chroma filter could severely band-limit a high-bandwidth PC video signal, which could roll-off and attenuate the sync pulses such that the LMH1980 cannot detect a valid input signal.

If some high-frequency noise filtering is needed for all video inputs, a small capacitor ( $C_1$ ) may be optionally used in parallel but outside of the transistor switch. When Q1 is turned on, then  $C_1$  and  $C_2$  will be connected in parallel ( $C_1+C_2$ )

### Input Coupling Capacitor

The input signal should be AC coupled to the  $V_{IN}$  (pin 4) of the LMH1980 with a properly chosen coupling capacitor,  $C_{IN}$ .

The primary consideration in choosing  $C_{IN}$  is whether the LMH1980 will interface with video sources using an AC-coupled output stage. If AC-coupled video sources are expected in the end-application, then it's recommended to choose a small  $C_{IN}$  value such as 0.01  $\mu\text{F}$  to avoid missing sync output pulses due to average picture level changes. It's important to note that video sources with an AC-coupled output will cause video-dependent jitter at the HSync output of the sync separator. When only DC-coupled video sources are expected, a larger value for  $C_{IN}$  may be used without concern for missing sync output pulses. A smaller  $C_{IN}$  value can be used to increase rejection of source AC hum components and also reduce start-up time regardless of the video source's output coupling type.

### START-UP TIME

When there is a significant change to the video input signal, such as sudden signal switching in, signal attenuation (i.e.: load termination added via loop through) or signal gain (i.e.: load termination removed), the quiescent operation of the LMH1980 will be disrupted. During this dynamic input condition, the LMH1980 outputs may not be correct but will recover to valid signals after a predictable start-up time, which consists of an adjustable input settling time and a predetermined "sync lock time".

### Input Settling Time and Coupling Capacitor Selection

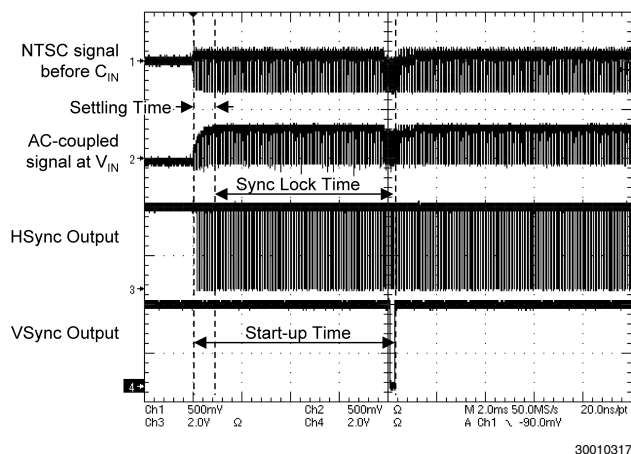
Following a significant input condition, the negative sync tip of the AC-coupled signal settles to the input clamp voltage as the coupling capacitor,  $C_{IN}$ , recovers a quiescent DC voltage via the dynamic clamp current through  $V_{IN}$ . Because  $C_{IN}$  determines the input settling time, its capacitance value is critical when minimizing overall start-up time. A smaller  $C_{IN}$  value yields shorter settling time at the expense of increased line droop voltage, whereas a larger one yields reduced line droop but longer settling time. Settling time is proportional to the value of  $C_{IN}$ , so doubling  $C_{IN}$  will also double the settling time.

### Sync Lock Time

In addition to settling time, the LMH1980 has a predetermined sync lock time,  $T_{\text{SYNC-LOCK}}$ , before the outputs are correct. Once the AC-coupled input has settled enough, the LMH1980 needs time to detect the valid video signal and apply fixed-level sync slicing before the output signals are correct.

For practical values of  $C_{IN}$ ,  $T_{\text{SYNC-LOCK}}$  is typically less than 1 or 2 video fields in duration starting from the 1st valid VSync output pulse to the valid HSync pulses beginning thereafter. VSync and HSync pulses are considered valid when they align correctly with the input's vertical and horizontal sync intervals.

It is recommended for the outputs to be applied to the system after the start-up time is satisfied and outputs are valid. For example, the oscilloscope screenshot in *Figure 12* shows a typical start-up time within 1 video field from when an NTSC signal is just applied to when the LMH1980 outputs are valid.



30010317

**FIGURE 12. Typical Start-Up Time for NTSC Input to LMH1980 ( $C_{IN} = 0.1 \mu\text{F}$ )**

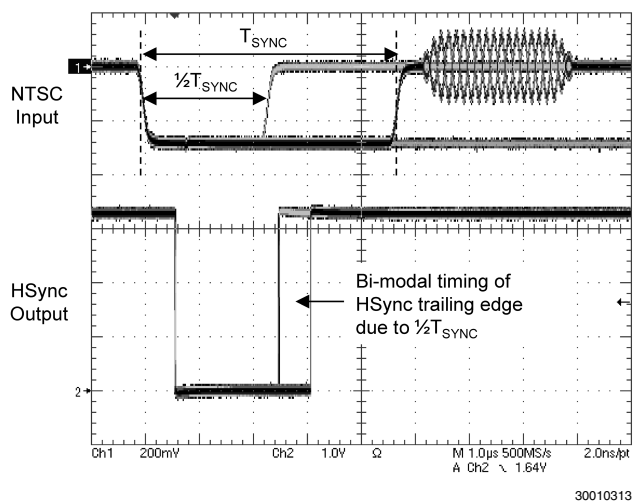
### LOGIC OUTPUTS

In the absence of a video input signal, the LMH1980 outputs are logic high except for the odd/even field, which is undefined and depends on its previous state, and the composite sync output.

### Horizontal Sync Output

HSOUT (pin 6) produces a negative-polarity horizontal sync signal, or HSync, extracted from the input signal. For bi-level and tri-level sync signals, HSync's negative-going leading edge is derived from the input's sync reference,  $O_H$ , with a propagation delay.

**Important:** The HSync output has good performance on its negative-going leading edge, so it should be used as the reference to a negative-edge triggered PLL input. If HSync is used as the reference to a positive-edge triggered PLL input, like in some FPGAs, the signal must be inverted first to produce a positive-polarity HSync signal (i.e.: positive-going leading edge) before the PLL input. HSync's trailing edge **should not** be used as the reference to a PLL because for a NTSC/PAL input, the input's half-width pulses ( $\frac{1}{2}T_{\text{SYNC}}$ ) in the vertical interval cause the trailing edges of the HSync output to occur earlier than for the normal-width sync pulses ( $T_{\text{SYNC}}$ ). This bi-modal timing variation on HSync's trailing edge, as shown in *Figure 13*, could affect the performance of the PLL. The bi-modal trailing edge timing also occurs on the CSync output as well.



**FIGURE 13. Bi-modal Timing on HSync's Trailing Edge for Half-Width Pulses for NTSC**

### Vertical Sync Output

VSOUT (pin 7) produces a negative-polarity vertical sync signal, or VSync. VSync's negative-going leading edge is derived from the first vertical serration pulse with a propagation delay, and its output pulse width,  $T_{VSOUT}$ , spans approximately three horizontal periods (3H). When there is no vertical serration pulses (i.e.: non-standard video signal), the LMH1980 will output a default VSync pulse derived from the input's vertical sync leading edge with a propagation delay.

### Composite Sync Output

CSOUT (pin 8) simply reproduces the video input sync pulses below the video blanking level. This is obtained by clamping the video signal sync tip to the internal clamp voltage at  $V_{IN}$  and extracting the resultant composite sync signal, or CSync. For both bi-level and tri-level syncs, CSync's negative-going leading edge is derived from the input's negative-going leading edge with a propagation delay.

### Burst/Back Porch Timing Output

BPOUT (pin 9) provides a negative-polarity burst/back porch signal, which is pulsed low for a fixed width during the back porch interval following the input's sync pulse. The burst/back porch timing pulse is useful as a burst gate signal for NTSC/PAL color burst synchronization and as a clamp signal for black level clamping (DC restoration) and sync stripping applications.

For SDTV formats, the back porch pulse's negative-going leading edge is derived from the input's positive-going sync edge with a propagation delay, and the pulse width spans an appropriate duration of the color burst envelope for NTSC/PAL. For EDTV formats, the back porch pulse behaves similar to the SDTV case except with a narrow pulse width. For HDTV formats, the pulse's leading edge is derived from the input's negative-going trailing sync edge with a propagation delay, and the pulse width is narrow to correspond with the short back porch durations. During the vertical sync period, the back porch output will be muted (no pulses) and remain logic high.

### Odd/Even Field Output

OEOUT (pin 10) provides an odd/even field output signal, which facilitates identification of odd and even fields for interlaced or segmented frame (sF) formats. For interlaced or segmented frame formats, the odd/even output is logic high

during an odd field (field 1) and logic low during an even field (field 2). The odd/even output edge transitions align with VSync's leading edge to designate the start of odd and even fields. For progressive (non-interlaced) video formats, the output is held constantly at logic high.

### HD Detect Flag Output

$\overline{HD}$  (pin 5) is an active-low flag output that only outputs a logic low signal when a valid HD video input (i.e.: 720P, 1080I and 1080P) with tri-level sync is detected; otherwise, it will output logic high. Note that there is a processing delay (within 1 to 2 video fields) from when an HD video signal is applied to when the outputs are correct and the  $\overline{HD}$  flag changes from logic high (default) to logic low, to indicate a valid HD input has been detected.

The  $\overline{HD}$  flag can be used to disable an external switch-controlled SD chroma filter when HD video is detected and conversely, enable it when SD video is detected. This is important because a non-switched chroma filter attenuates signal components above 500 kHz to 3 MHz, which could roll-off and/or attenuate the high bandwidth HD tri-level sync signal prior to the LMH1980 and may increase output propagation delay and jitter. See the Input Filtering section for more information.

### ADDITIONAL CONSIDERATIONS

#### Using an AC-Coupled Video Source into the LMH1980

An AC coupled video source typically has a 100  $\mu\text{F}$  or larger output coupling capacitor ( $C_{OUT}$ ) for protection and to remove the DC bias of the amplifier output from the video signal. When the video source is load terminated, the average value of the video signal will shift dynamically as the video duty cycle varies due to the averaging effect of the  $C_{OUT}$  and termination resistors. The average picture level or APL of the video content is closely related to the duty cycle.

For example, a significant decrease in APL such as a white-to-black field transition will cause a positive-going shift in the sync tips characterized by the source's RC time constant,  $t_{RC-OUT}$  ( $150\Omega * C_{OUT}$ ). The LMH1980's input clamp circuitry may have difficulty stabilizing the input signal under this type of shifting; consequently, the unstable signal at  $V_{IN}$  may cause missing sync output pulses to result, **unless** a proper value for  $C_{IN}$  is chosen.

To avoid this potential problem when interfacing AC-coupled sources to the LMH1980, it's necessary to introduce a voltage droop component via  $C_{IN}$  to compensate for video signal shifting related to changes in the APL. This can be accomplished by selecting  $C_{IN}$  such that the effective time constant of the LMH1980's input circuit,  $t_{RC-IN}$ , is less than  $t_{RC-OUT}$ .

The effective time constant of the input circuit can be approximated as:  $t_{RC-IN} = (R_S + R_I) * C_{IN} * T_{LINE} / T_{CLAMP}$ , where  $R_S = 150\Omega$ ,  $R_I = 1\text{ k}\Omega$  (input resistance when clamping),  $T_{LINE} \sim 64\ \mu\text{s}$  for NTSC, and  $T_{CLAMP} = 250\text{ ns}$  (internal clamp duration). A white-to-black field transition in NTSC video through  $C_{OUT}$  will exhibit the maximum sync tip shifting due to its long line period ( $T_{LINE}$ ). By setting  $t_{RC-IN} < t_{RC-OUT}$ , the maximum value of  $C_{IN}$  can be calculated to ensure proper operation under this worst-case condition.

For instance,  $t_{RC-OUT}$  is about 33 ms for  $C_{OUT} = 220\ \mu\text{F}$ . To ensure  $t_{RC-IN} < 33\text{ ms}$ ,  $C_{IN}$  must be about 100 nF or less. By choosing  $C_{IN} = 47\text{ nF}$ , the LMH1980 will function properly with AC-coupled video sources using  $C_{OUT} \geq 220\ \mu\text{F}$ .

### PCB LAYOUT CONSIDERATIONS

Please refer to the "LMH1980 Evaluation Board Instruction Manual" Application Note (AN-1618) for a good PCB layout

example, which adheres to the following suggestions for component placement and signal routing.

#### **LMH1980 IC Placement**

The LMH1980 should be placed such that critical signal paths are short and direct to minimize PCB parasitics from degrading the video input and logic output signals.

#### **Ground Plane**

A two-layer, FR-4 PCB is sufficient for this device. One of the PCB layers should be dedicated to a single, solid ground plane that connects to the GND pin of the device and connects to other components, serving as the common ground reference. It also helps to reduce trace inductances and minimize ground loops. Routing supply and signal traces on another layer can help to maintain as much ground plane continuity as possible.

#### **Power Supply Routing**

The power supply pin should be connected using short traces with minimal inductance. When routing the supply traces, try not to disrupt the solid ground plane.

For high frequency bypassing, place 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  SMD ceramic bypass capacitors with very short connections to  $V_{\text{CC}}$  and GND pins. Place a 4.7 or 10  $\mu\text{F}$  SMD tantalum bypass capacitor nearby the  $V_{\text{CC}}$  for low frequency supply bypassing.

#### **$R_{\text{EXT}}$ Resistor**

The  $R_{\text{EXT}}$  resistor should be a 10  $\text{k}\Omega$  1% SMD precision resistor. Place  $R_{\text{EXT}}$  as close as possible to the device and

connect to pin 1 and the ground plane using the shortest possible connections. All input and output signals should be kept as far as possible from this pin to prevent unwanted signals from coupling into this bias reference pin.

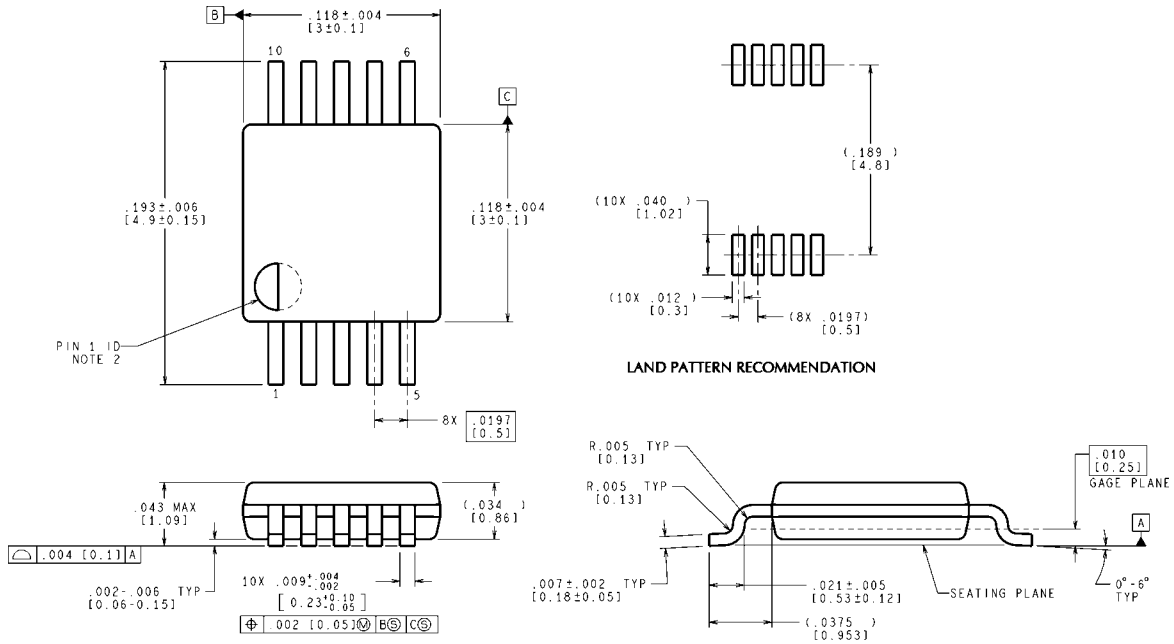
#### **Video Input**

The input signal path should be routed using short, direct traces between video source and input pin. Use a 75 $\Omega$  load termination on the board, if not on the cable. If applicable, the chroma filter components should be connected using short traces and the filter capacitor should be connected to the ground plane. There should be a sufficient return path from the LMH1980 back to the input source via the ground plane.

#### **Output Routing**

The output signal paths should be routed using short, direct traces to minimize parasitic effects that may degrade these high-speed logic signals. The logic outputs do not have high output drive capability. Each output should have a resistive load of about 10 $\text{k}\Omega$  or more and capacitive load of about 10pF including parasitic capacitances for optimal signal quality. Each output can be protected against brief short-circuit events using a small series resistor, like 100 $\Omega$ , to limit output current.

**Physical Dimensions** inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH  
 VALUES IN [ ] ARE MILLIMETERS  
 DIMENSIONS IN ( ) FOR REFERENCE ONLY

MUB10A (Rev B)

**10-Pin MSOP  
 NS Package Number MUB10A**

## Notes

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2007 National Semiconductor Corporation

For the most current product information visit us at [www.national.com](http://www.national.com)



**National Semiconductor  
Americas Customer  
Support Center**  
Email:  
[new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

**National Semiconductor Europe  
Customer Support Center**  
Fax: +49 (0) 180-530-85-86  
Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +49 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia  
Pacific Customer Support Center**  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor Japan  
Customer Support Center**  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560