National Semiconductor

January 2003

LMH6718
Dual, High Output, Programmable Gain Buffer

General Description

The LMH6718 is a dual, low cost high speed (130MHz) buffer which features user programmable gains of +2, +1, and -1V/V. The LMH6718 also has a new output stage that delivers high output drive current (200mA), but consumes minimal quiescent supply current (2.6mA/Amp) from a ±5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of signal levels, and has a linear phase response up to one half of the -3dB frequency.

The LMH6718 offers 0.1dB gain flatness to 30MHz and differential gain and phase errors of .04% and .03˚. These features are ideal for professional and consumer video applications.

The LMH6718 offers superior dynamic performance with a 130MHz small-signal bandwidth, 600V/µs slew rate and 4.2ns rise/fall times ($2V_{STEP}$). The combination of low quiescent current, high output current drive, and high speed performance makes the LMH6718 well suited for many battery powered personal communication/computing systems. The ability to drive low impedance, high capacitive loads, makes the LMH6718 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The LMH6718 will drive a 100Ω load with only –84/–84dBc second/third harmonic distortion (A_V = +2, V_{OUT} = $2V_{PP}$, f = 1MHz). It is also optimized for driving high currents into single-ended transformers and coils. When driving the input of high resolution A/D converters, the LMH6718 provides excellent -88/-98dBc second/third harmonic distortion (A_V = +2, V_{OUT} = $2V_{PP}$, f = 1MHz, R_L = 1kΩ) and fast settling time.

The LMH6718 is fabricated using National's VIP10™ complimentary bipolar process.

Features

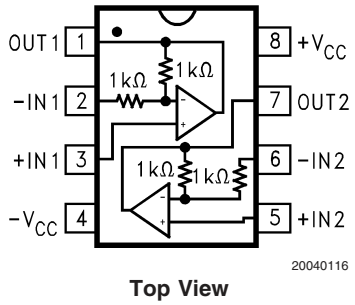
- 200mA output current
- .04%, .03˚ differential gain, phase
- 5.2mA supply current for 2 amplifiers
- 130MHz bandwidth (A_V = +2)
- –88/–98dBc HD2/HD3 (1MHz)
- 16ns settling to 0.05%
- 600V/µs slew rate
- Nominal supply range ±2.5V to ±6V
- Improved replacement for CLC5632

Applications

- Video line driver
- Coaxial cable driver
- Twisted pair driver
- Transformer/coil driver
- High capacitive load driver
- Portable/battery powered applications
- A/D driver
- I/Q Channel Amplifier

Connection Diagram

8-Pin SOIC



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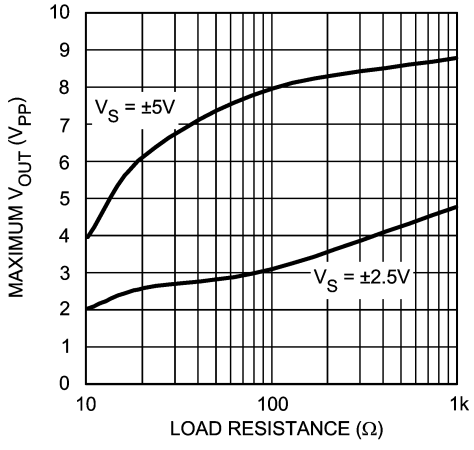
Top View

Maximum Output Voltage vs. Load Resistance



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2kV
Machine Model	200V
Supply Voltage	13.5
Output Current	(Note 3)
Common-Mode Input Voltage	V^+ - V^-
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C

Operating Ratings

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
SOIC	50˚C/W	145˚C/W
Nominal Operating Voltage		±2.5V to ±6V
Operating Temperature Range		−40˚C to +85˚C

+5V Electrical Characteristics (Note 2)

A_V = +2, R_L = 100Ω, V_S = +5V (Note 4), Unless Specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_O =0.5V_{PP}	70	110		MHz
		V_O =2.0V_{PP}		90		
SSBW	−0.1dB Bandwidth	V_O =0.5V_{PP}		23		MHz
GFP	Gain Peaking	<200MHz, V_O =0.5V_{PP}		0		dB
GFR	Gain Rolloff	<30MHz, V_O =0.5V_{PP}		0.2		dB
LPD	Linear Phase Deviation	<30MHz, V_O = 0.5V_{PP}		0.12		deg
Time Domain Response						
Tr	Rise and Fall Time	2V Step		4.8		ns
Ts	Settling Time to 0.05%	1V Step		20		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	2V Step	250	400		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 1MHz		−85		dBc
		2V_{PP}, 1MHz; R_L = 1kΩ		−88		
		2V_{PP}, 5MHz		−73		
HD3	3rd Harmonic Distortion	2V_{PP},1MHz		−89		dBc
		2V_{PP}, 1MHz, R_L = 1kΩ		−91		
		2V_{PP}, 5MHz		−71		
XTLKA	Crosstalk (Input Referred)	10MHz, 1V_{PP}		−85		dB
Static, DC Performance						
V_{IO}	Input Offset Voltage			±.6	±10 **±20**	mV
DV_{IO}	Average Drift			10		µV/˚C
I_{BN}	Input Bias Current (Non-Inverting)			±.6	±15 **±20**	µA
DI_{BN}	Average Drift			20		nA/˚C
GACC	Gain Accuracy			±0.3	±1.5 **±2.0**	%
	Internal Resistors (R_F, R_G)		750	950	1150	Ω
PSRR	Power supply Rejection Ratio	DC	50	60		dB
CMRR	Common Mode Rejection Ratio	DC	50 **47**	56		dB
I_{CC}	Supply Current per channel	R_L = ∞	2.0 **1.9**	2.4	3.0 **3.1**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance (Non-Inverting)			0.38		MΩ

+5V Electrical Characteristics (Note 2) (Continued)

A_V = +2, R_L = 100Ω, V_S = +5V (Note 4), Unless Specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance (Non-Inverting)			2.2		pF
V_{CMH}	Input Voltage Range, High			4.2		V
V_{CML}	Input Voltage Range, Low			0.8		V
V_{ROH}	Output Voltage Range, High	R_L = 100Ω	3.6 **3.5**	4.0		V
V_{ROL}	Output Voltage Range, Low	R_L = 100Ω	1.4 **1.3**	1.0		V
V_{ROH}	Output Voltage Range, High	R_L = ∞		4.1		V
V_{ROL}	Output Voltage Range, Low	R_L = ∞		0.9		V
I_O	Output Current (Note 3)			170		mA
R_O	Output Resistance, Closed Loop	DC		.28		Ω

±5V Electrical Characteristics (Note 2)

A_V = +2, R_L = 100Ω, V_{CC} = ±5V; Unless Specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_O =1.0V_{PP}	100	130		MHz
		V_O =4.0V_{PP}		70		
SSBW	–0.1dB Bandwidth	V_O = 1.0V_{PP}		30		MHz
GFP	Gain Peaking	<200MHz, V_O = 1.0V_{PP}		0		dB
GFR	Gain Rolloff	<300MHz, V_O = 1.0V_{PP}		0.1		dB
LPD	Linear Phase Deviation	<30MHz, V_O = 1.0V_{PP}		0.1		deg
DG	Differential Gain	NTSC, R_L = 150Ω		.04		%
DP	Differential Phase	NTSC, R_L = 150Ω		.03		deg
Time Domain Response						
Tr	Rise and Fall Time	2V Step		4.2		ns
Ts	Settling Time to 0.05%	2V Step		17		ns
OS	Overshoot	2V Step		14		%
SR	Slew Rate	2V Step	400	600		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP},1MHz		–84		dBc
		2V_{PP}, 1MHz; R_L =1kΩ		–88		
		2V_{PP}, 5MHz		–73		
HD3	3rd Harmonic Distortion	2V_{PP},1MHz		–84		dBc
		2V_{PP}, 1MHz; R_L = 1kΩ		–98		
		2V_{PP}, 5MHz		–76		
	Equivalent Input Noise					
V_N	Voltage (e_{ni})	>1MHz		8		nV/$\sqrt{Hz}$
I_{NN}	Non-Inverting Current (i_{bn})	>1MHz		9		pA/$\sqrt{Hz}$
XTLKA	Crosstalk (Input Referred)	10MHz, 1V_{PP}		–85		dB
Static, DC Performance						
V_{IO}	Input Offset Voltage			.2	±9.5 **±15**	mV
DV_{IO}	Average Drift			5		µV/˚C
I_{BN}	Input Bias Current (Non-Inverting)			1.3	±15 **±20**	µA
DI_{BN}	Average Drift			12		nA/˚C

±5V Electrical Characteristics (Note 2) (Continued)

A_V = +2, R_L = 100Ω, V_{CC} = ±5V; Unless Specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GACC	Gain Accuracy			±0.3	±1.5 **±2.0**	%
	Internal Resistor (R_F, R_G)		750	950	1150	Ω
PSRR	Power Supply Rejection Ratio	DC	50	62		dB
CMRR	Common Mode Rejection Ratio	DC	52 **49**	57		dB
I_{CC}	Supply Current per channel	R_L = ∞	2.2 **2.1**	2.6	3.3 **3.4**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance (Non-Inverting)			0.50		MΩ
C_{IN}	Input Capacitance (Non-Inverting)			1.9		pF
CMVR	Common-Mode Voltage Range			±4.2		V
V_{RO}	Output Voltage Range	R_L = 100Ω	3.6 **3.5**	±3.8		V
V_{RO}	Output Voltage Range	R_L = ∞		±4.0		V
I_O	Output Current (Note 3)			200		mA
R_O	Output Resistance, Closed Loop	DC		.28		Ω

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Note 3: The maximum current is determined by device power dissipation limitations. See the Power Dissipation section of the Application Division for more details.

Note 4: $V_S = V_{CC} - V_{EE}$

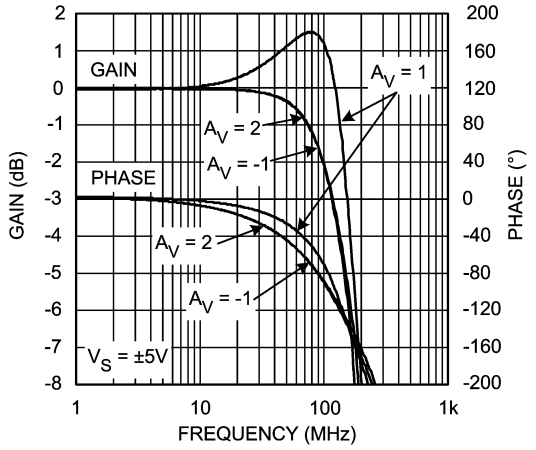
Note 5: Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω In series with 200pF.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-pin SOIC	LMH6718MA	LMH6718MA	Rails	M08A
	LMH6718IMAX		2.5k Units Tape and Reel	

Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified).

Frequency Response vs. Gain



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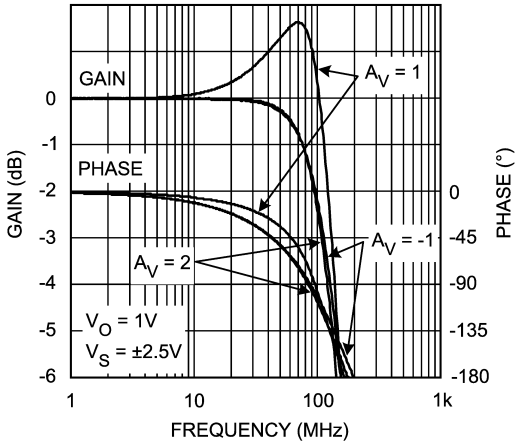
Frequency Response



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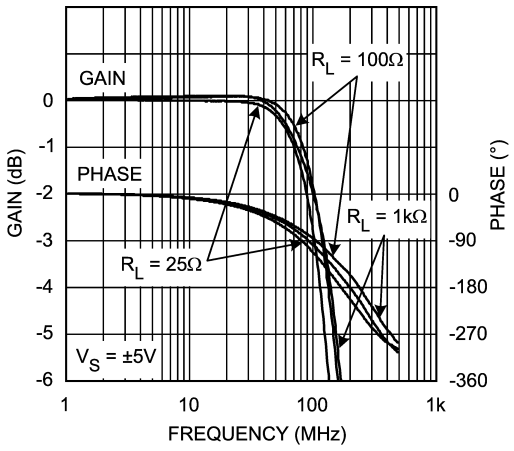
Frequency Response R_L



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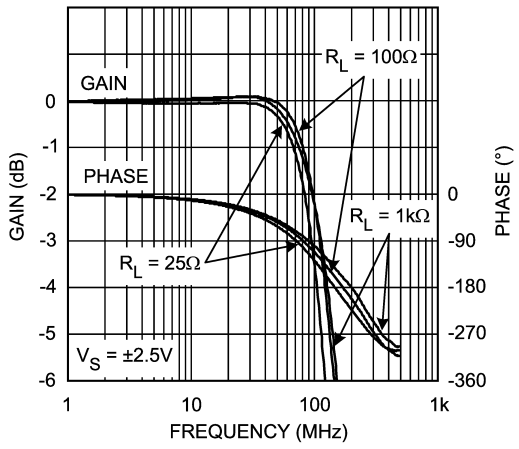
Frequency Response vs. R_L



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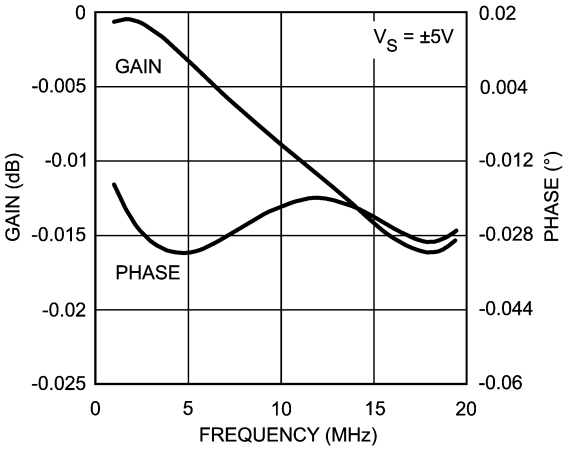
Gain Flatness & Linear Phase



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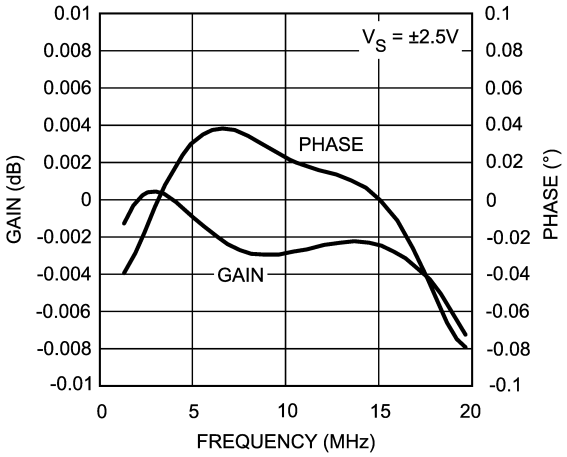
Gain Flatness & Linear Phase



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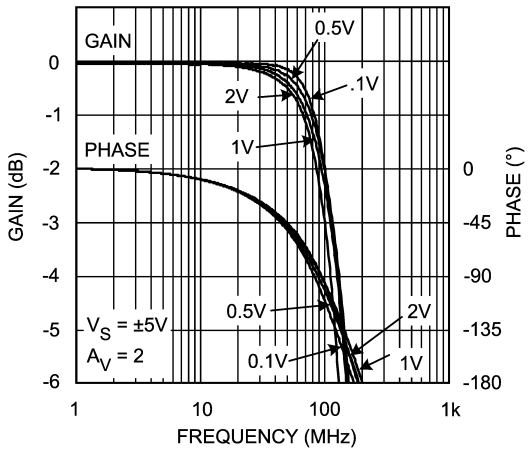
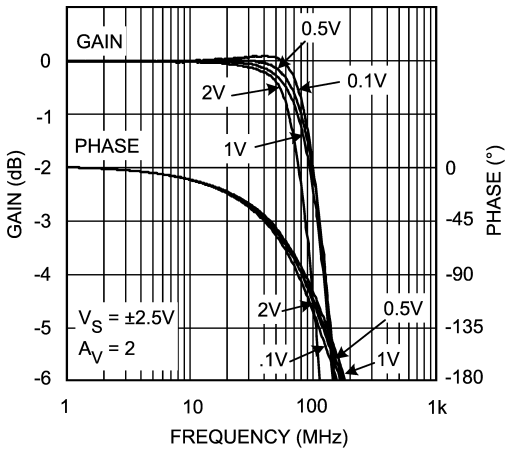
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified). (Continued)

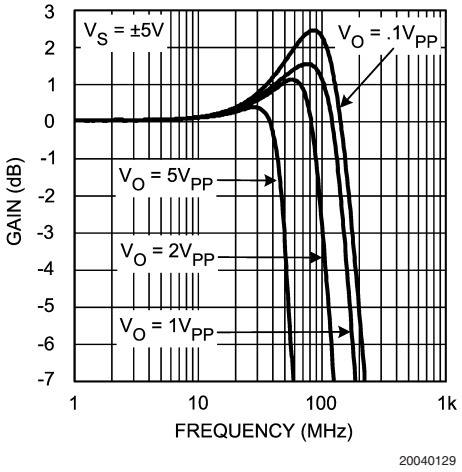
Frequency Response vs. V_O (A_V = 2)



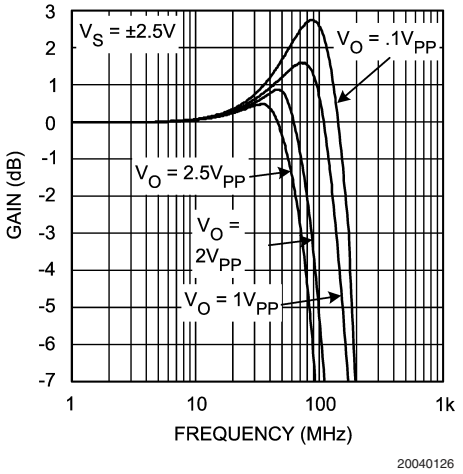
Frequency Response vs. V_O (A_V = 2)



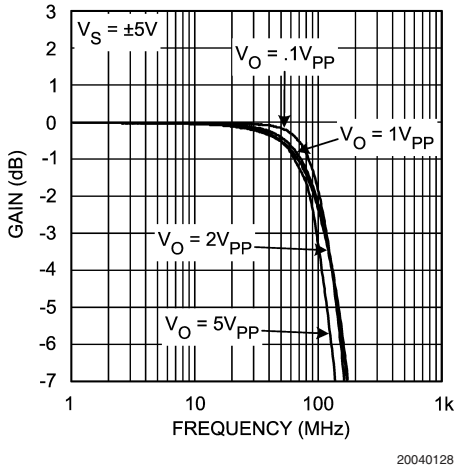
Frequency Response vs. V_O (A_V = 1)



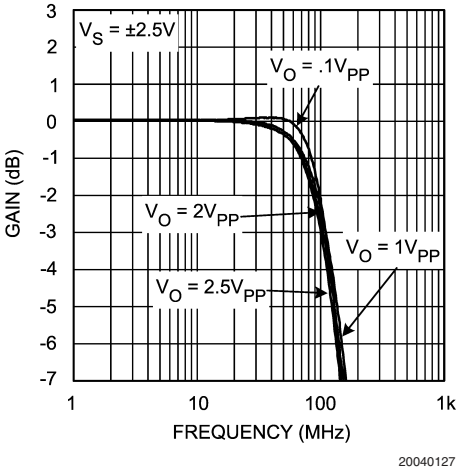
Frequency Response vs. V_O (A_V = 1)



Frequency Response vs. V_O (A_V = -1)

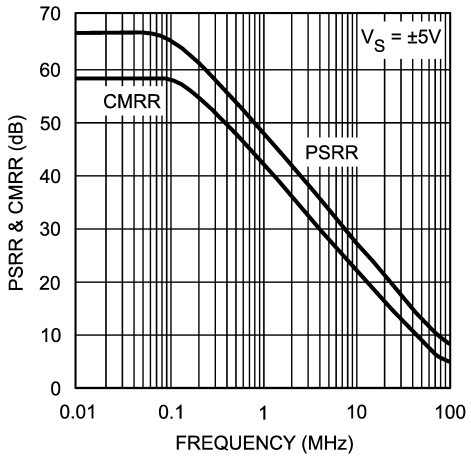


Frequency Response vs. V_O (A_V = -1)



Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified). (Continued)

PSRR & CMRR



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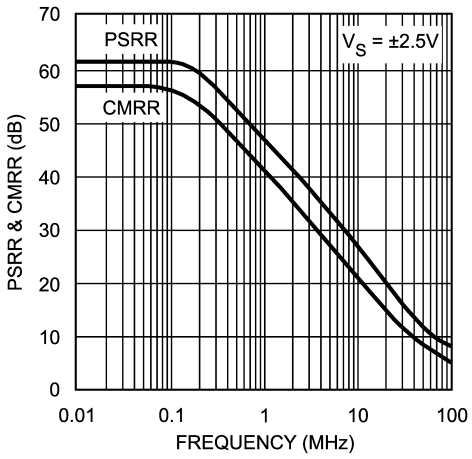
PSRR & CMRR



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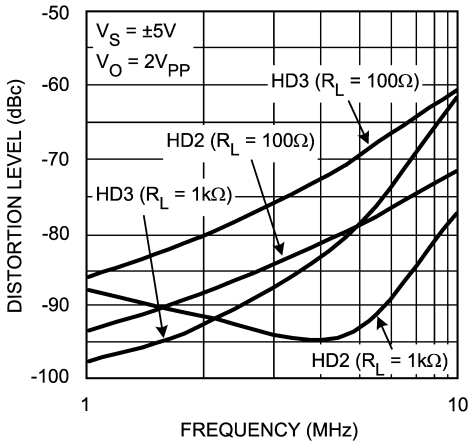
2nd & 3rd Harmonic Distortion vs. Frequency



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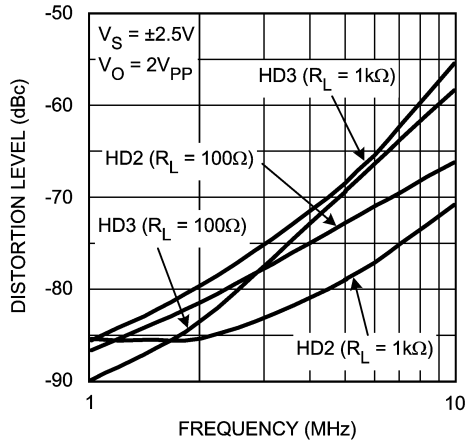
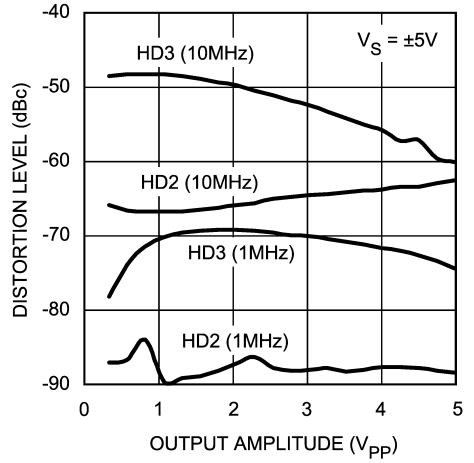
2nd & 3rd Harmonic Distortion vs. Frequency



20040109

2nd & 3rd Harmonic Distortion R_L = 25Ω



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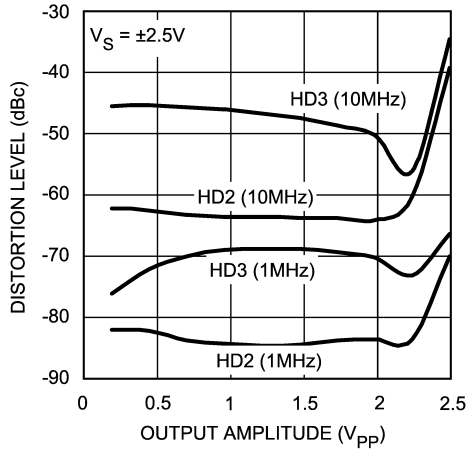
2nd & 3rd Harmonic Distortion R_L = 25Ω



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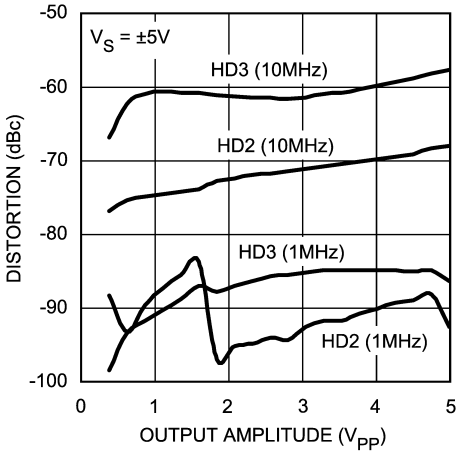
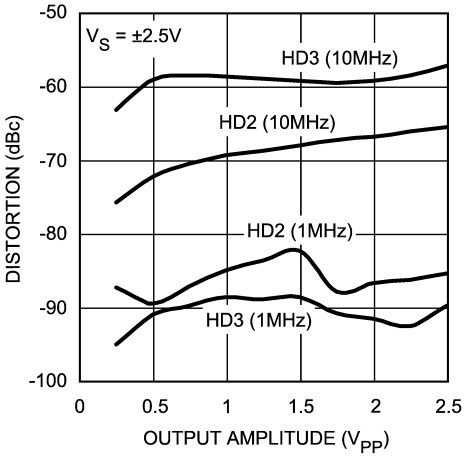
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified). (Continued)

2nd & 3rd Harmonic Distortion R_L = 100Ω



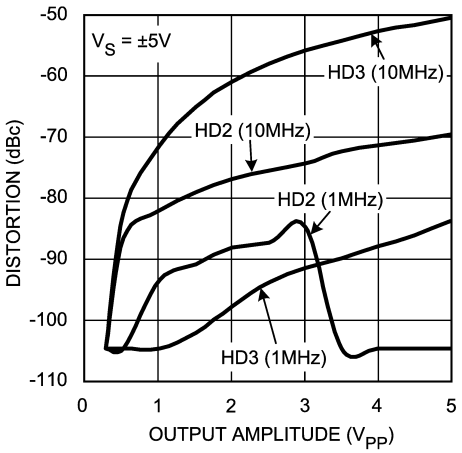
20040110

2nd & 3rd Harmonic Distortion R_L = 100Ω



20040111

2nd & 3rd Harmonic Distortion R_L = 1kΩ



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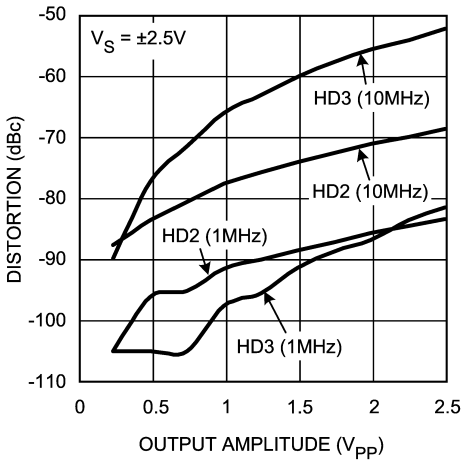
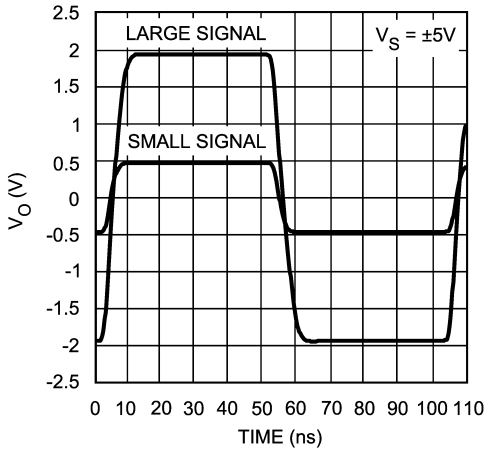
2nd & 3rd Harmonic Distortion R_L = 1kΩ



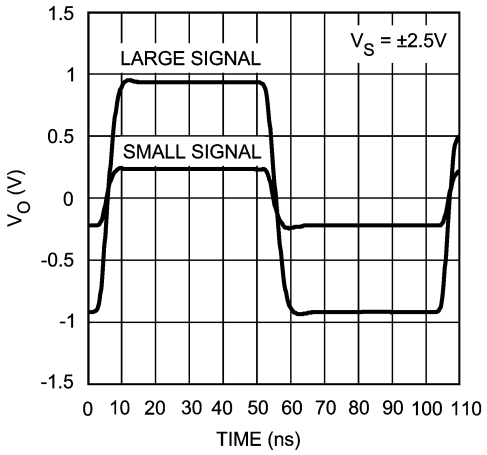
20040108

Pulse Response



20040119

Pulse Response



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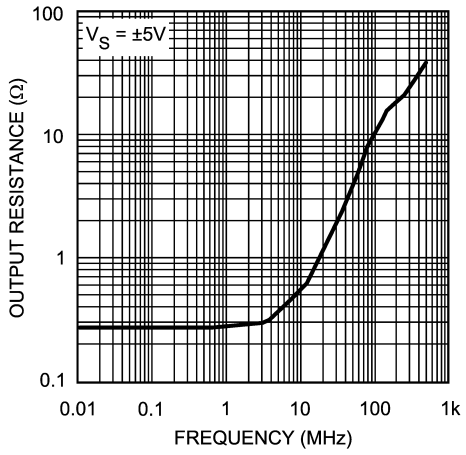
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified). (Continued)

Closed Loop Output Resistance



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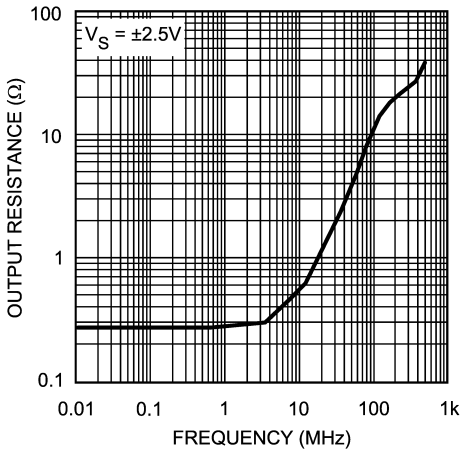
Closed Loop Output Resistance



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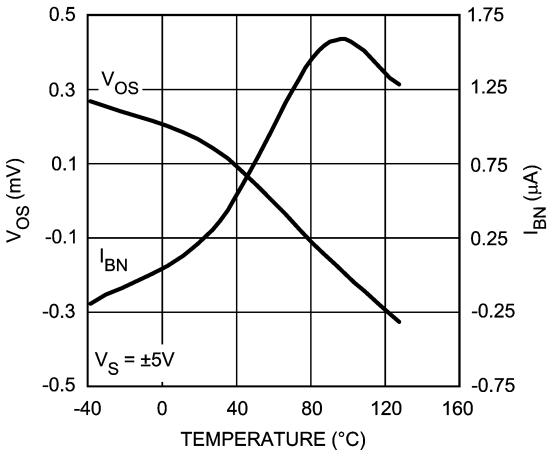
I_{BN} &V_{IO} vs. Temperature



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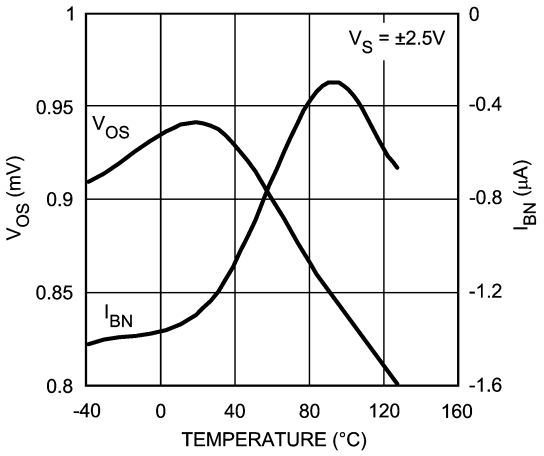
I_{BN} &V_{IO} vs. Temperature



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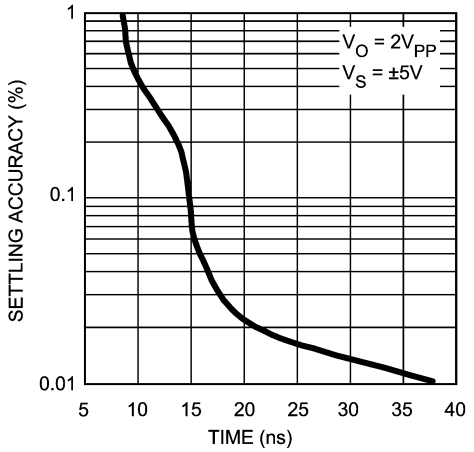
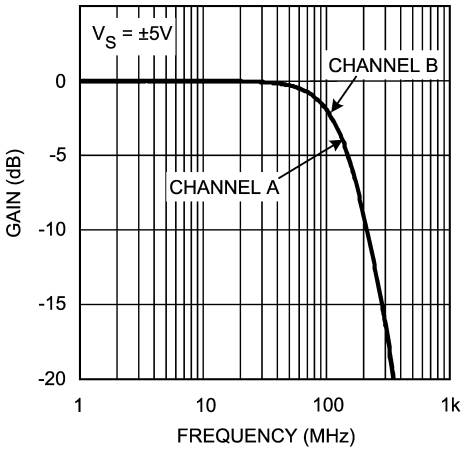
Settling Time vs. Accuracy



20040161

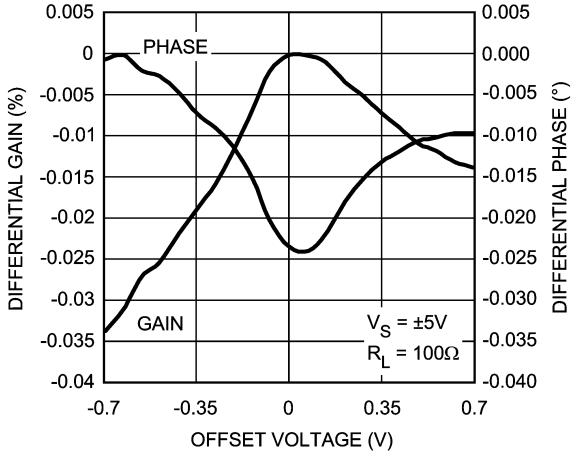
Channel Matching



20040103

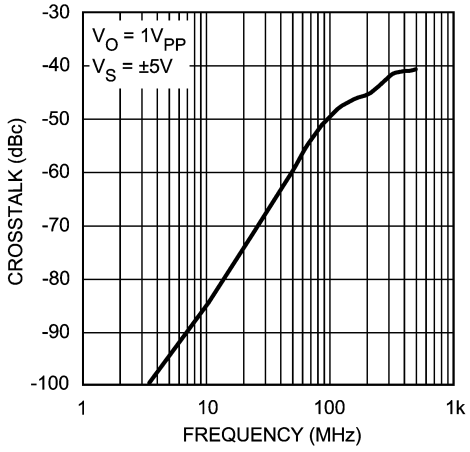
Typical Performance Characteristics (A_V = +2, R_L = 100Ω, Unless Specified). (Continued)

Differential Gain & Phase



20040165

Input Referred Crosstalk



20040132

Application Section

LMH6718 OPERATION

The LMH6718 is a current feedback buffer fabricated in an advanced complementary bipolar process. The LMH6718 operates from a single 5V supply or dual ±5V supplies. Operating from a single 5V supply, the LMH6718 has the following features:

- Gains of ±1, −1, and 2V/V are achievable without external resistors
- Provides 170mA of output current
- Offers low −88/−91dBc 2nd & 3rd harmonic distortion
- Provides BW > 110MHz

The LMH6718 performance is further enhanced in ±5V supply applications as indicated in the **±5V Electrical Characteristics** table and the **±5V Typical Performance** plots.

LMH6718 DESIGN INFORMATION

CLOSED LOOP GAIN SELECTION

The LMH6718 is a current feedback op amp with R_F = R_G = 1kΩ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of +2, +1, and −1V/V by connecting pins 2 and 3 (or 5 and 6) as described in the chart below.

Gain A_V	Input Connections	
	Non-Inverting (pins 3, 5)	Inverting (pins 2, 6)
−1V/V	ground	input signal
+1V/V	input signal	NC (open)
+2V/V	input signal	ground

The gain accuracy of the LMH6718 is excellent and stable over temperature change. The internal gain setting resistors, R_F and R_G are poly silicon resistors. Although their absolute values change with processing and temperature, their ratio (R_F/R_G) remains constant. If an external resistor is used in series with R_G, gain accuracy over temperature will suffer.

SINGLE SUPPLY OPERATION (V_{CC} = +5V, V_{EE} = GND)

The specifications given in the **+5V Electrical Characteristics** table for single supply operation are measured with a common mode voltage (V_{CM}) of 2.5V. V_{CM} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Voltage Range (CMVR) of the LMH6718 is typically +0.8V to +4.2V. The typical output range with R_L = 100Ω is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC COUPLED SINGLE SUPPLY OPERATION

Figure 1, *Figure 2*, and *Figure 3* on the following page, show the recommended configurations for input signals that remain above 0.8V DC.

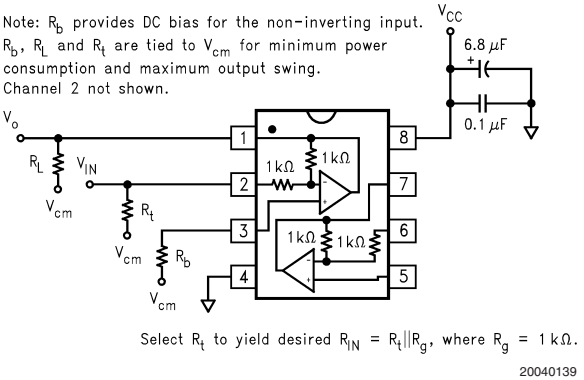


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FIGURE 1. DC Coupled, A_V = −1V/V Configuration

Application Section (Continued)

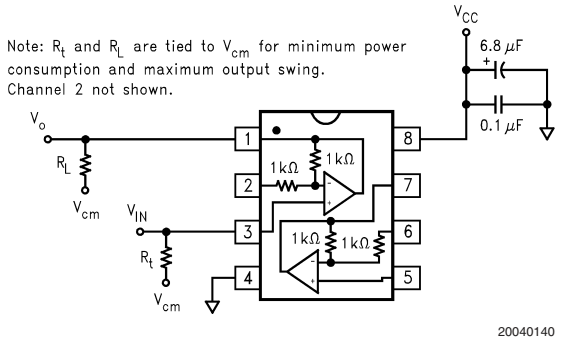


FIGURE 2. DC Coupled, A_V = +1V/V Configuration

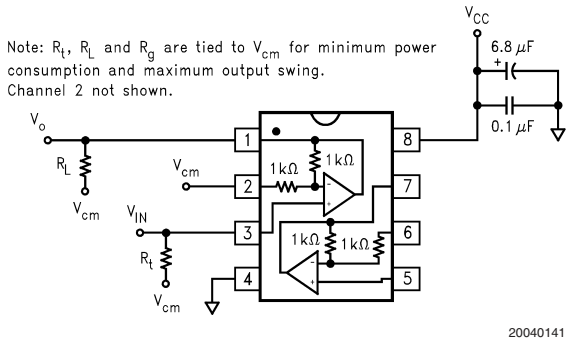


FIGURE 3. DC Coupled, A_V = +2V/V Configuration

AC COUPLED SINGLE SUPPLY OPERATION

Figure 4, *Figure 5*, and *Figure 6* show possible non-inverting and inverting configurations for input signals that go below 0.8V DC.

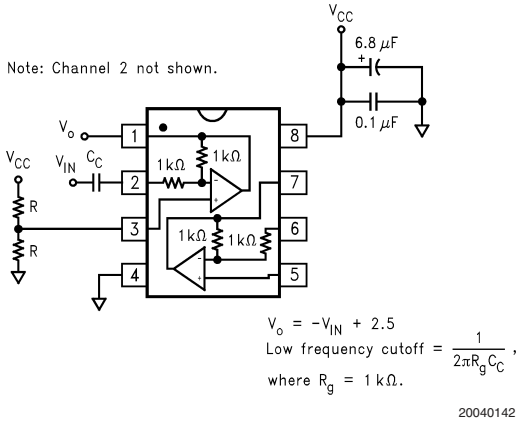


FIGURE 4. AC Coupled, A_V = –1V/V Configuration

The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For V_{CC} = +5V)

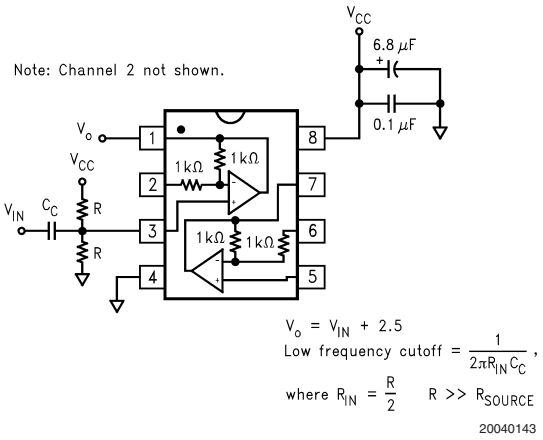


FIGURE 5. AC Coupled, A_V = +1V/V Configuration

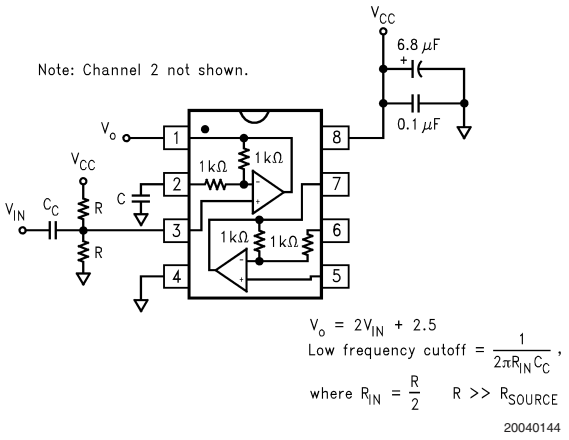


FIGURE 6. AC Coupled, A_V = +2V/V Configuration

DUAL SUPPLY OPERATION

The LMH6718 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in *Figure 7*, *Figure 8*, and *Figure 9*.

Application Section (Continued)

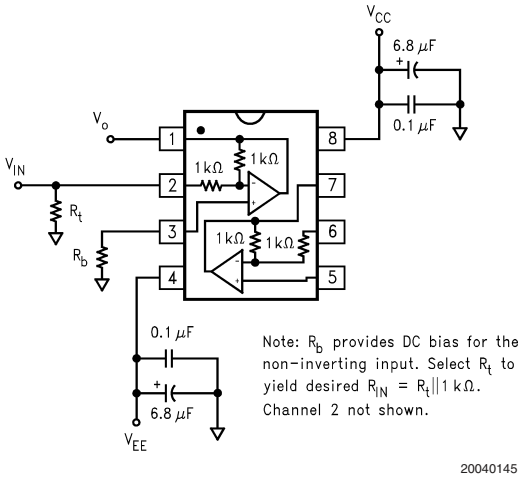


FIGURE 7. Dual Supply, A_V = –1V/V Configuration

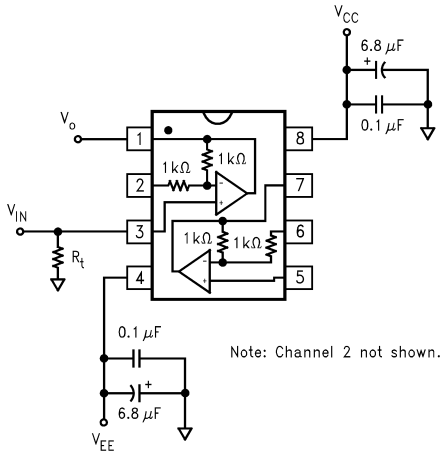


FIGURE 8. Dual Supply, A_V = +1V/V Configuration

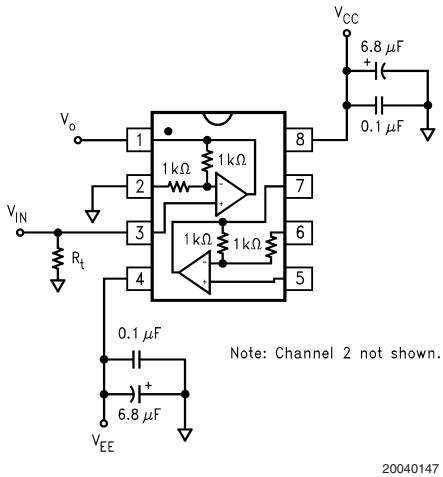


FIGURE 9. Dual Supply, A_V = +2V/V Configuration

LOAD TERMINATION

The LMH6718 can source and sink nearly equal amounts of current.

DRIVING CABLES AND CAPACITIVE LOADS

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the LMH6718 will improve stability and settling performance. The **Suggested R_S vs. C_L** plot, shown below in *Figure 10*, gives the recommended series resistance value for optimum flatness at various capacitive loads.

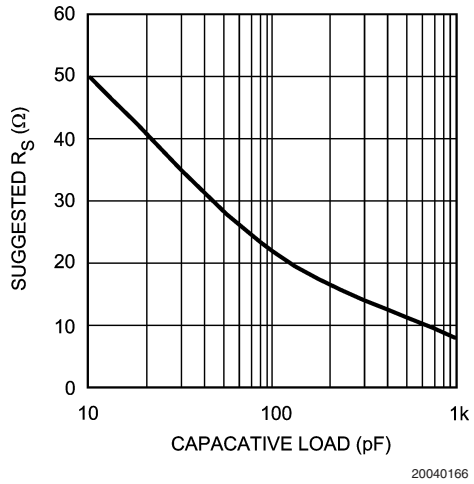


FIGURE 10. Suggested R_S vs. C_L

TRANSMISSION LINE MATCHING

One method for matching the characteristic impedance (Z_O) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. *Figure 11* shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-Inverting gain applications:

- Connect pin 2 as indicated in the table in the **Closed Loop Gain Selection** section.
- Make R_1, R_2, R_6, and R_7 equal to Z_O.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_O.
- Make $R_5 \parallel R_g = Z_O$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C6 to match the output transmission line over a greater frequency range. C6 compensates for the increase of the amplifier's output impedance with frequency.

Application Section (Continued)

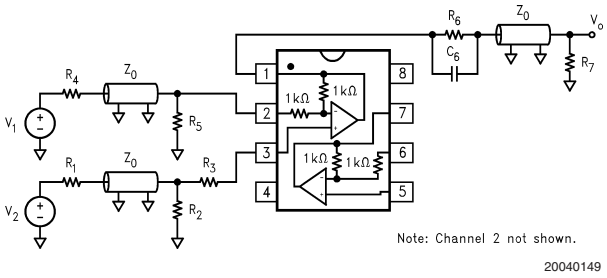


FIGURE 11. Transmission Line Matching

POWER DISSIPATION

Follow these steps to determine the power consumption of the LMH6718:

1. Calculate the quiescent (no-load) power: $P_{amp} = I_{CC} (V_{CC}–V_{EE})$

2. Calculate the RMS power at the output stage: $P_O = (V_{CC} –V_{LOAD}) (I_{LOAD})$, where V_{LOAD} and I_{LOAD} are the voltage and current across the external load.

3. Calculate the total RMS power: $P_t = P_{amp}+P_O$. The maximum power that the SOIC, package can dissipate at a given temperature is illustrated in *Figure 12*. The power derating curve for any LMH6718 package can be derived by utilizing the following equation:

$$\frac{(150° - T_{amb})}{\theta_{JA}}$$

where

T_{amb} = Ambient temperature (˚C)

θ_{JA} = Thermal resistance, from junction to ambient, for a given package (˚C/W)

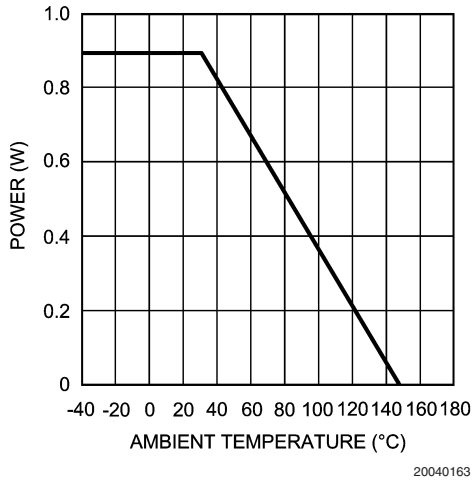


FIGURE 12. Power Derating Curve

LAYOUT CONSIDERATIONS

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the LMH6718 (CLC730036-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

EVALUATION BOARD INFORMATION

A datasheet is available for the CLC730036 evaluation board. The evaluation board data sheets provide:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

SPECIAL EVALUATION BOARD CONSIDERATION FOR THE LMH6718

To optimize off-isolation of the LMH6718, cut the R_f trace on the CLC730036 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. *Figure 13* shows where to cut both evaluation boards for improved off-isolation.

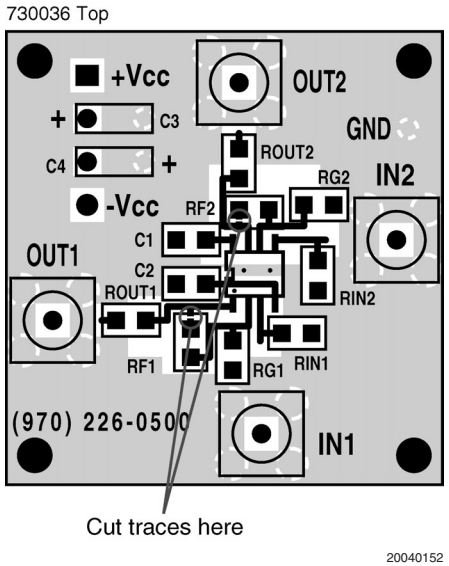


FIGURE 13. Evaluation Board Changes

Application Circuits

SINGLE SUPPLY CABLE DRIVER

Figure 14 below shows the LMH6718 driving 10m of 75Ω coaxial cable. The LMH6718 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_O. The response after 10m of cable is illustrated in *Figure 15*

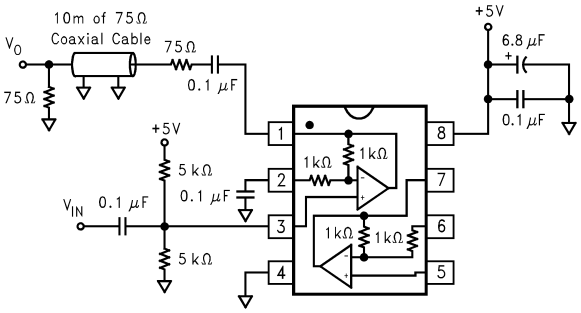


FIGURE 14. Single Supply Cable Driver

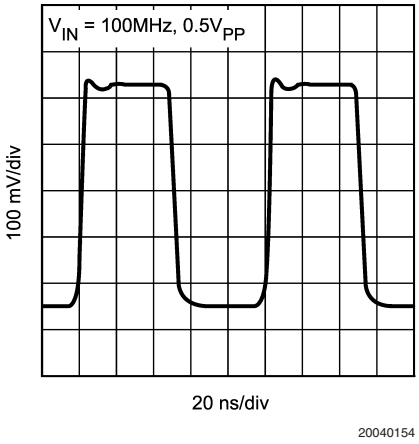


FIGURE 15. Response After 10m of Cable

DIFFERENTIAL LINE DRIVER WITH LOAD IMPEDANCE CONVERSION

The circuit shown in *Figure 16*, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the LMH6718's output capabilities. The single-ended input signal is converted to a differential signal by the LMH6718. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.

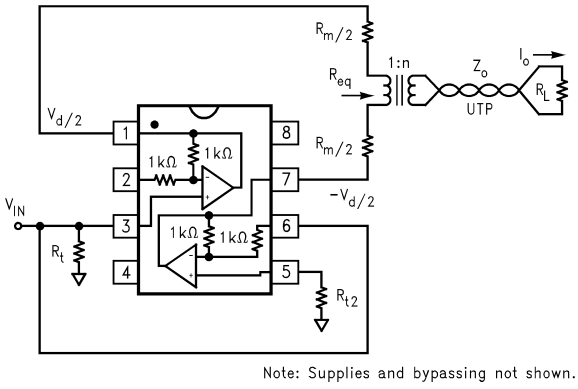


FIGURE 16. Differential Line Driver with Load Impedance Conversion

Set up the LMH6718 as a difference amplifier:

- Set the Channel 1 amplifier to a gain of +1V/V
- Set the Channel 2 amplifier to a gain of −1V/V

Make the best use of the LMH6718's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where R_{eq} is the transformed value of the load impedance, V_{max} is the output Voltage Range, and I_{max} is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_O$$
$$R_M = R_{EQ}$$
$$N = \sqrt{\frac{R_L}{R_{EQ}}}$$

Select the transformer so that it loads the line with a value very near Z_O over frequency range. The output impedance of the LMH6718 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_0(j\omega)}{Z_0} \right|, \text{ dB}$$

where $Z_O(6718)(j\omega)$ is the output impedance of the LMH6718 and $|Z_O(6718)(j\omega)| << R_m$.

The load voltage and current will fall in the ranges:

$$\left| V_O \right| \leq n \cdot V_{max}$$
$$\left| I_O \right| \leq \frac{I_{max}}{n}$$

The LMH6718's high output drive current and low distortion make it a good choice for this application.

Application Circuits (Continued)

DIFFERENTIAL INPUT/DIFFERENTIAL OUTPUT AMPLIFIER

below illustrates a differential input/differential output configuration. The bypass capacitors are the only external components required.

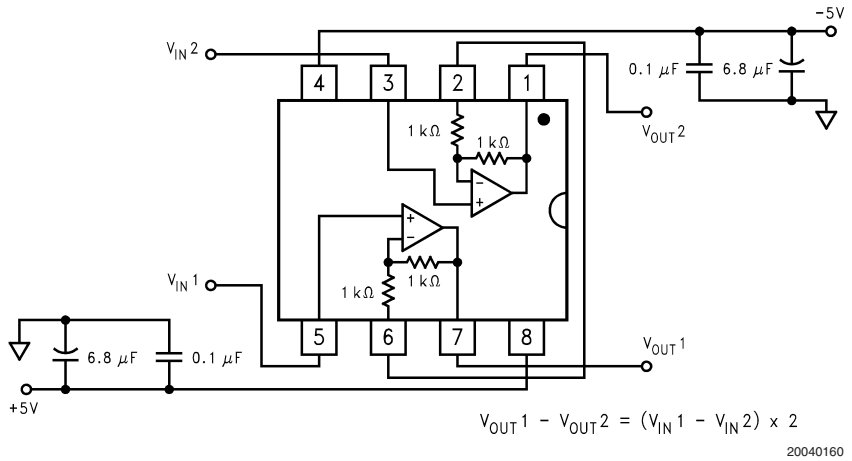
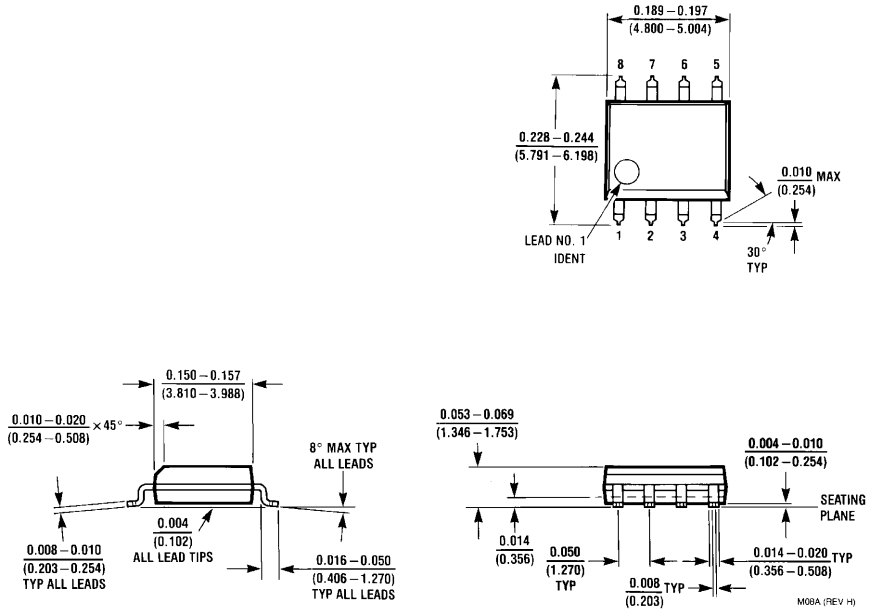


FIGURE 17. Differential Input/Differential Output Amplifier

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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