National Semiconductor

ADVANCE INFORMATION
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LMK03000/LMK03000C/LMK03001/LMK03001C Precision Clock Conditioner with Integrated VCO

LMK03000/LMK03000C/LMK03001/LMK03001C
Precision Clock Conditioner with Integrated VCO

General Description

The LMK03000/LMK03000C/LMK03001/LMK03001C precision clock conditioners combine the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The devices integrate a Voltage Controlled Oscillator (VCO), a high performance Integer-N Phase Locked Loop (PLL), a partially integrated loop filter, three LVDS, and five LVPECL clock output distribution blocks.

The VCO output is optionally accessible on the Fout port. Internally, the VCO output goes through an Input Divider to feed the various clock distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVDS or LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to eight system components.

The clock conditioners come in a 48-pin LLP package and are footprint compatible with other clocking devices in the same family.

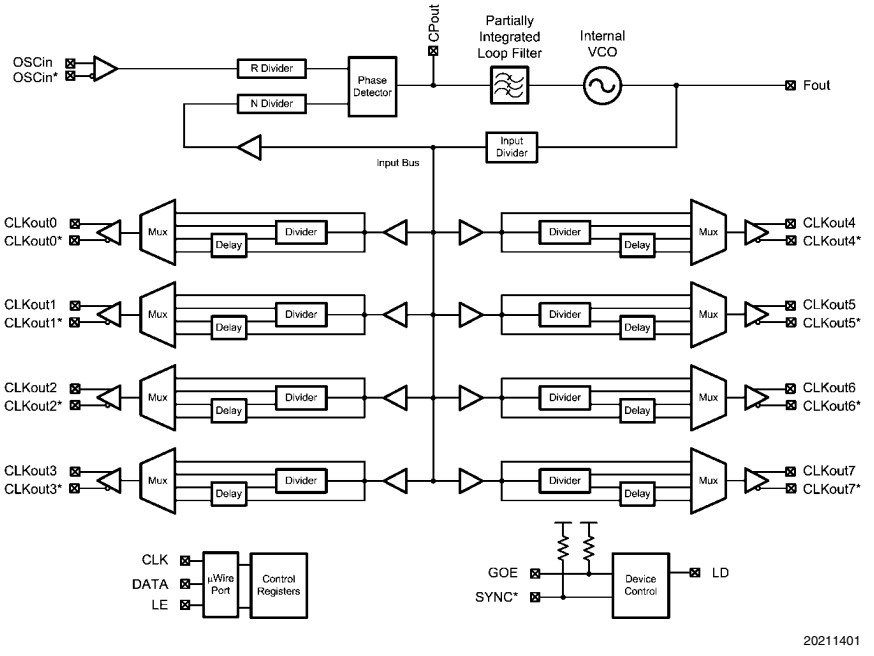
Features

- Integrated VCO and Integer-N PLL
- Two performance grades (12 kHz to 20 MHz)
  - — LMK03000/LMK03001: Less than 800 fs RMS
  - — LMK03000C/LMK03001C: Less than 400 fs RMS
- Two VCO frequency plans
  - — LMK03000/LMK03000C: 1185 to 1296 MHz
  - — LMK03001/LMK03001C: 1470 to 1570 MHz
- Clock output frequency range of 1 to 785 MHz
- 3 LVDS and 5 LVPECL clock outputs
- Partially integrated loop filter
- Dedicated divider and delay blocks on each clock output
- Pin compatible family of clocking devices
- 3.15 to 3.45 V operation
- Package: 48 pin LLP (7.0 x 7.0 x 0.8 mm)

Target Applications

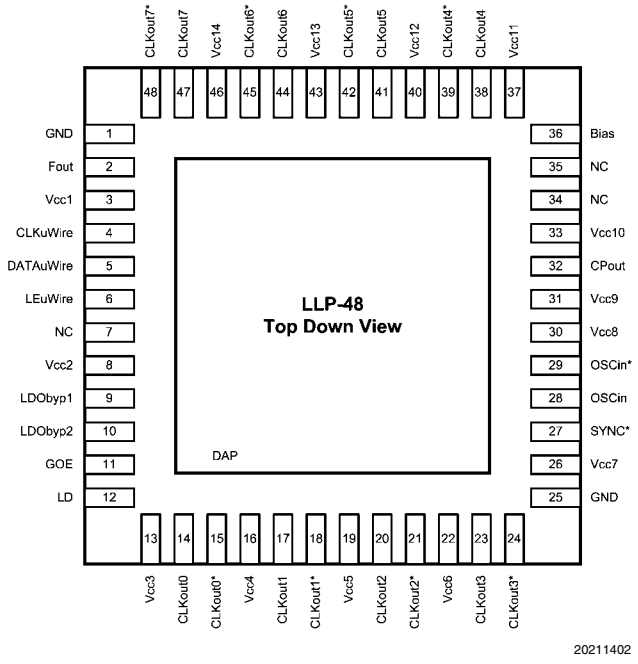
- Data Converter Clocking
- SONET/SDH, DSLAM
- Networking
- Wireless Infrastructure
- Medical
- Test and Measurement
- Military / Aerospace

Functional Block Diagram



Connection Diagram

48-Pin LLP Package



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Pin Descriptions

Pin #	Pin Name	I/O	Description
1, 25	GND	-	Ground
2	Fout	O	Internal VCO Frequency Output
3, 8, 13, 16, 19, 22, 26, 30, 31, 33, 37, 40, 43, 46	Vcc1, Vcc2, Vcc3, Vcc4, Vcc5, Vcc6, Vcc7, Vcc8, Vcc9, Vcc10, Vcc11, Vcc12, Vcc13, Vcc14	-	Power Supply
4	CLKuWire	I	MICROWIRE Clock Input
5	DATAuWire	I	MICROWIRE Data Input
6	LEuWire	I	MICROWIRE Latch Enable Input
7, 34, 35	NC	-	No Connection to these pins
9, 10	LDObyp1, LDObyp2	-	LDO Bypass
11	GOE	I	Global Output Enable
12	LD	O	Lock Detect and Test Output
14, 15	CLKout0, CLKout0*	O	LVDS Clock Output 0
17, 18	CLKout1, CLKout1*	O	LVDS Clock Output 1
20, 21	CLKout2, CLKout2*	O	LVDS Clock Output 2
23, 24	CLKout3, CLKout3*	O	LVPECL Clock Output 3
27	SYNC*	I	Global Clock Output Synchronization
28, 29	OSCin, OSCin*	I	Oscillator Clock Input; Must be AC coupled
32	CPout	O	Charge Pump Output
36	Bias	I	Bias Bypass
38, 39	CLKout4, CLKout4*	O	LVPECL Clock Output 4
41, 42	CLKout5, CLKout5*	O	LVPECL Clock Output 5
44, 45	CLKout6, CLKout6*	O	LVPECL Clock Output 6
47, 48	CLKout7, CLKout7*	O	LVPECL Clock Output 7
DAP	DAP	-	Die Attach Pad is Ground

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Power Supply Voltage	V_{CC}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to (V_{CC} + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 s)	T_L	+260	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	-40	25	85	°C
Power Supply Voltage	V_{CC}	3.15	3.3	3.45	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.

Note 2: This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of >2 kV, a MM-ESD of >200 V, and a CDM-ESD of >1.2 kV.

Electrical Characteristics

(Vcc = 3.3 V, -40 °C ≤ T_A ≤ 85 °C; Differential Inputs/Outputs; except as specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Consumption						
I_{CC}	Power Supply Current	Entire device with one LVPECL and one LVDS output operating at 765 MHz in bypass mode (CLKoutX_MUX = Bypass)		162		mA
		Divider Circuitry (CLKoutX_DIV = 4) Each clock output		9		
		Delay Circuitry (CLKoutX_DLY = 2250 ps) Each clock output		10		
$I_{CC}PD$	Power Down Current	POWERDOWN = 1		1		mA
Reference Oscillator						
f_{OSCin}	Reference Oscillator Input Frequency Range		1		200	MHz
$SLEW_{OSCin}$	Reference Oscillator Input Slew Rate	(Note 3)	0.5			V/ns
V_{OSCin}	Input voltage for OSCin and OSCin*	AC coupled; Single ended	0.2		1.6	Vpp
PLL						
f_{COMP}	Phase Detector Frequency				40	MHz
$I_{SRCE}CPout$	Charge Pump Source Current	V_{CPout} = Vcc/2, PLL_CP_GAIN = 1x		100		µA
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 4x		400		
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 16x		1600		
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 32x		3200		
$I_{SINK}CPout$	Charge Pump Sink Current	V_{CPout} = Vcc/2, PLL_CP_GAIN = 1x		-100		µA
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 4x		-400		
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 16x		-1600		
		V_{CPout} = Vcc/2, PLL_CP_GAIN = 32x		-3200		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
		PLL (Continued)					
I_{CPout}TRI	Charge Pump TRI-STATE Current	0.5 V < V_{CPout} < Vcc - 0.5 V			2	10	nA
I_{CPout}%MIS	Magnitude of Charge Pump Sink vs. Source Current Mismatch	V_{CPout} = Vcc / 2 T_A = 25°C			3		%
I_{CPout}VTUNE	Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation	0.5 V < V_{CPout} < Vcc - 0.5 V T_A = 25°C			4		%
I_{CPout}TEMP	Magnitude of Charge Pump Current vs. Temperature Variation				4		%
PN10kHz	PLL 1/f Noise at 10 kHz Offset (Note 4) Normalized to 1 GHz Output Frequency	PLL_CP_GAIN = 1x			-117		dBc/Hz
		PLL_CP_GAIN = 32x			-122		
PN1Hz	Normalized Phase Noise Contribution (Note 5)	PLL_CP_GAIN = 1x			-219		dBc/Hz
		PLL_CP_GAIN = 32x			-224		
		VCO					
f_{Fout}	VCO Tuning Range	LMK03000/LMK03000C		1185		1296	MHz
		LMK03001/LMK03001C		1470		1570	
$\|\Delta T_{CL}\|$	Allowable Temperature Drift for Continuous Lock	After programming R15 for lock, no changes to output configuration are permitted to guarantee continuos lock. (Note 6)				125	°C
p_{Fout}	Output Power to a 50 Ω load driven by Fout	LMK03000/LMK03000C; T_A = 25 °C			3.3		dBm
		LMK03001/LMK03001C; T_A = 25 °C			2.7		
K_{Vtune}	Fine Tuning Sensitivity (The lower sensitivity indicates the typical sensitivity at the lower end of the tuning range, the higher sensitivity at the higher end of the tuning range)	LMK03000/LMK03000C			7 to 9		MHz/V
		LMK03001/LMK03001C			9 to 11		
J_{RMS}Fout	Fout RMS Period Jitter	LMK03000/LMK03001 12 kHz to 20 MHz bandwidth			< 800		fs
		LMK03000C/LMK03001C 12 kHz to 20 MHz bandwidth			< 400		fs
$L(f)_{Fout}$	Fout Single Side Band Phase Noise	LMK03000C f_{Fout} = 1296 MHz (Note 7)	1 kHz Offset		TBD		dBc/Hz
			10 kHz Offset		-91.4		
			100 kHz Offset		-116.8		
			1 MHz Offset		-137.8		
			10 MHz Offset		-156.9		
		LMK03000C f_{Fout} = 1185 MHz (Note 7)	1 kHz Offset		TBD		
			10 kHz Offset		-93.5		
			100 kHz Offset		-118.5		
			1 MHz Offset		-139.4		
			10 MHz Offset		-158.4		
		LMK03001C f_{Fout} = 1570 MHz (Note 7)	1 kHz Offset		TBD		
			10 kHz Offset		-89.6		
			100 kHz Offset		-115.2		
			1 MHz Offset		-136.5		
			10 MHz Offset		-156.0		
		LMK03001C f_{Fout} = 1470 MHz (Note 7)	1 kHz Offset		TBD		
			10 kHz Offset		-91.6		
			100 kHz Offset		-116.0		
			1 MHz Offset		-137.9		
			10 MHz Offset		-156.2		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Clock Distribution Section (Note 8) **- LVDS Clock Outputs (CLKout0 to CLKout2)**							
$Jitter_{ADD}$	Additive RMS Jitter (Note 8)	R_L = 100 Ω Input Bus = 785 MHz Bandwidth = 12 kHz to 20 MHz	CLKoutX_MUX = Bypass		40		fs
			CLKoutX_MUX = Divided CLKoutX_DIV = 4		150		
t_{SKEW}	CLKoutX to CLKoutY	Equal loading and identical channel configuration R_L = 100 Ω		-30	±4	30	ps
V_{OD}	Differential Output Voltage	R_L = 100 Ω		250	350	450	mV
ΔV_{OD}	Change in magnitude of V_{OD} for complementary output states	R_L = 100 Ω		-35		35	mV
V_{OS}	Output Offset Voltage	R_L = 100 Ω		1.125	1.25	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states	R_L = 100 Ω		-35		35	mV
I_{SA} I_{SB}	Clock Output Short Circuit Current single ended	Single ended outputs shorted to GND		-24		24	mA
I_{SAB}	Clock Output Short Circuit Current differential	Complementary outputs tied together		-12		12	mA
Clock Distribution Section (Note 8) **- LVPECL Clock Outputs (CLKout3 to CLKout7)**							
$Jitter_{ADD}$	Additive RMS Jitter (Note 8)	R_L = 100 Ω Input Bus = 785 MHz Integration Bandwidth = 12 kHz to 20 MHz	CLKoutX_MUX = Bypass		40		fs
			CLKoutX_MUX = Divided CLKoutX_DIV = 4		150		
t_{SKEW}	CLKoutX to CLKoutY	Equal loading and identical channel configuration Termination = 50 Ω to Vcc - 2 V		-30	±3	30	ps
V_{OH}	Output High Voltage	Termination = 50 Ω to Vcc - 2 V			Vcc - 0.98		V
V_{OL}	Output Low Voltage				Vcc - 1.8		V
V_{OD}	Differential Output Voltage			660	810	965	mV
Digital LVTTL Interfaces (Note 9)							
V_{IH}	High-Level Input Voltage			2.0		Vcc	V
V_{IL}	Low-Level Input Voltage					0.8	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc		-1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0		-1.0		1.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = -500 µA		Vcc - 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -500 µA				0.4	V
Digital MICROWIRE Interfaces (Note 10)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage					0.4	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc		-1.0		1.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0		-1.0		1.0	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MICROWIRE Timing						
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	25			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	8			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	25			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	25			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	25			ns
t_{CES}	Enable to Clock Set Up Time	See Data Input Timing	25			ns
t_{EWH}	Enable Pulse Width High	See Data Input Timing	25			ns

Note 3: For all frequencies the slew rate, $SLEW_{OSCin}$, is measured between 20% and 80%. If only OSCin is being driven (OSCin* AC grounded), the slew rate is half, 0.25 V/ns.

Note 4: A specification in modeling PLL in-band phase noise is the 1/f flicker noise, $L_{PLL\_flicker}(f)$, which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10kHz = $L_{PLL\_flicker}$(10 kHz) - 20log(Fout / 1 GHz), where $L_{PLL\_flicker}$ (f) is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure $L_{PLL\_flicker}(f)$ it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f).

Note 5: A specification in modeling PLL in-band phase noise is the Normalized Phase Noise Contribution, $L_{PLL\_flat}(f)$, of the PLL and is defined as: PN1Hz = $L_{PLL\_flat}(f) - 20\log(N) - 10\log(Fcomp)$. $L_{PLL\_flat}(f)$ is the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth and Fcomp is the comparison frequency of the synthesizer. $L_{PLL\_flat}(f)$ contributes to the total noise, L(f). To measure $L_{PLL\_flat}(f)$ the offset frequency, f, must be chosen sufficiently smaller then the loop bandwidth of the PLL, and yet large enough to avoid a substantial noise contribution from the reference and flicker noise.

Note 6: Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction and stay in lock from the ambient temperature and programmed state at which the device was when register R15 was programmed. The action of programming the R15 register, even to the same value, activates a frequency calibration routine. This implies that the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R15 register to ensure that it stays in lock. Regardless of what temperature the part was initially programmed at, the ambient temperature can never drift outside the range of -40 °C $\leq T_A \leq$ 85 °C without violating specifications. For this specification to be valid the programmed state of the device must not change after R15 is programmed.

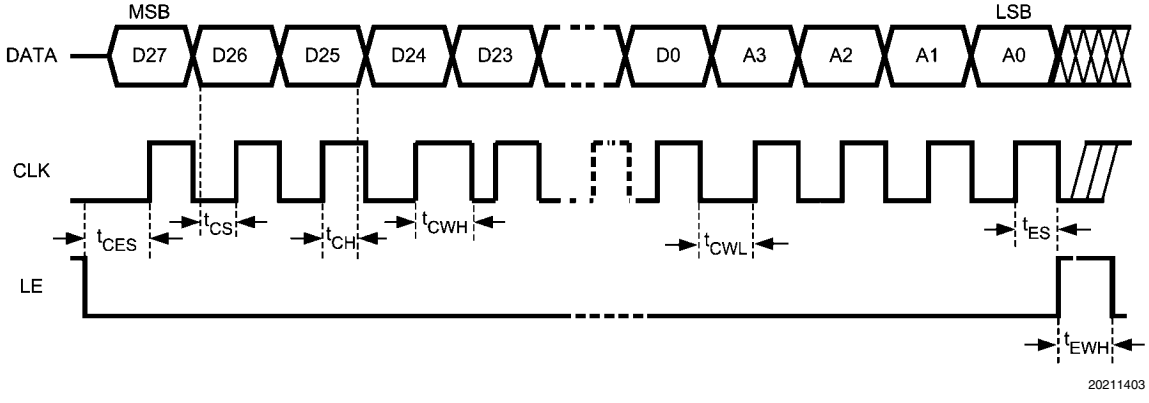
Note 7: VCO phase noise is measured assuming the VCO is the dominant noise source due to a 75 Hz loop bandwidth. Over frequency, the phase noise typically varies by 1 to 2 dB, with the worst case performance typically occurring at the highest frequency. Over temperature, the phase noise typically varies by 1 to 2 dB, assuming the part is not reloaded. Re-programming R15 will run the frequency calibration routine for optimum phase noise.

Note 8: The Clock Distribution Section includes all parts of the device except the PLL and VCO sections. Typical Additive Jitter specifications apply to the clock distribution section only and is in RMS form addition to the jitter from the VCO.

Note 9: Applies to GOE, LD, and SYNC*.

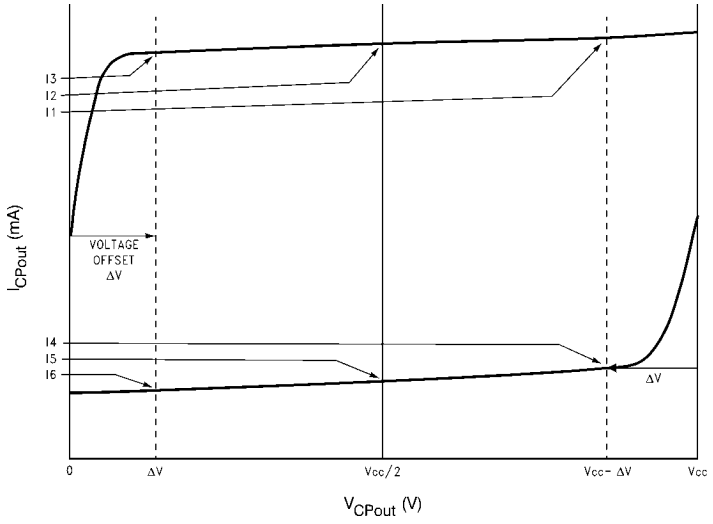
Note 10: Applies to uWireCLK, uWireDATA, and uWireLE.

Serial Data Timing Diagram



Data bits set on the DATA signal are clocked into a shift register, MSB first, on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift register to the addressed register determined by the LSB bits. After the programming is complete the CLK, DATA, and LE signals should be returned to a low state.

Charge Pump Current Specification Definitions



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I1 = Charge Pump Sink Current at V_{CPout} = Vcc - ΔV

I2 = Charge Pump Sink Current at V_{CPout} = Vcc/2

I3 = Charge Pump Sink Current at V_{CPout} = ΔV

I4 = Charge Pump Source Current at V_{CPout} = Vcc - ΔV

I5 = Charge Pump Source Current at V_{CPout} = Vcc/2

I6 = Charge Pump Source Current at V_{CPout} = ΔV

ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

Charge Pump Output Current Magnitude Variation vs. Charge Pump Output Voltage

$$I_{CPout}\ Vs\ V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

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Charge Pump Sink Current vs. Charge Pump Output Source Current Mismatch

$$I_{CPout}\ Sink\ Vs\ I_{CPout}\ Source = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

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Charge Pump Output Current Magnitude Variation vs. Temperature

$$I_{CPout}\ Vs\ T_A = \frac{|I_2|_{T_A} - |I_2|_{T_A = 25°C}}{|I_2|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|_{T_A} - |I_5|_{T_A = 25°C}}{|I_5|_{T_A = 25°C}} \times 100\%$$

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1.0 Functional Description

The LMK03000/LMK03000C/LMK03001/LMK03001C precision clock conditioners combine the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The devices integrate a Voltage Controlled Oscillator (VCO), a high performance Integer-N Phase Locked Loop (PLL), a partially integrated loop filter, three LVDS, and five LVPECL clock output distribution blocks.

The LMK03000 and LMK03001 Standard Grade devices feature jitter performance of less than 800 fs RMS. The LMK03000C and LMK03001C Premium Grade devices each feature jitter performance of less than 400 fs RMS.

The devices include internal 3rd and 4th order poles to simplify loop filter design and improve spurious performance. The 1st and 2nd order poles are off-chip to provide flexibility for the design of various loop filter bandwidths.

Two VCO frequency plans are available for each performance grade. The LMK03000 and LMK03000C include a 1.24 GHz VCO. The LMK03001 and LMK03001C include a 1.52 GHz VCO. The VCO output is optionally accessible on the Fout port. Internally, the VCO output goes through an Input Divider to feed the various clock distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVDS or LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to eight system components.

The clock conditioners come in a 48-pin LLP package and are footprint compatible with other clocking devices in the same family.

1.1 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1 µF capacitor connected to Vcc. This is important for low noise performance.

1.2 LDO BYPASS

To properly use the device, bypass LDObyp1 (pin 9) with a 10 µF capacitor and LDObyp2 (pin 10) with a 0.1 µF capacitor.

1.3 OSCILLATOR INPUT PORT (OSCin, OSCin*)

The purpose of OSCin is to provide the PLL with a reference signal. The OSCin port may be driven single endedly by AC grounding OSCin* with a 0.1 µF capacitor.

1.4 LOW NOISE, FULLY INTEGRATED VCO

The LMK03000/LMK03000C/LMK03001/LMK03001C devices contain a fully integrated VCO. In order for proper operation the VCO uses a frequency calibration algorithm. The frequency calibration algorithm is activated any time that the R15 register is programmed. Once R15 is programmed the temperature may not drift more than the maximum allowable drift for continuous lock, ΔT_{CL}, or else the VCO is not guaranteed to stay in lock.

For the frequency calibration algorithm to work properly OSCin must be driven by a valid signal when R15 is programmed.

1.5 CLKout DELAYS

Each individual clock output includes a delay adjustment. Clock output delay registers (CLKoutX_DLY) support a 150 ps step size and range from 0 to 2250 ps of total delay.

1.6 LVDS/LVPECL OUTPUTS

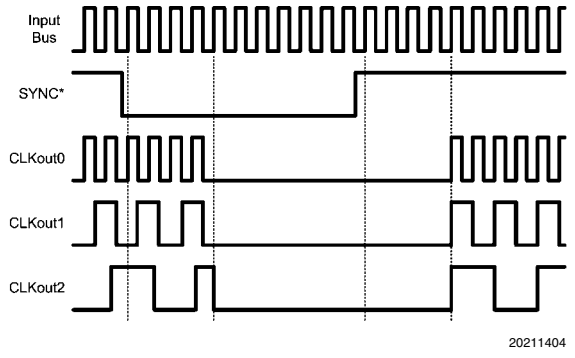
Each LVDS or LVPECL output may be disabled individually by programming the CLKoutX_EN bits. All the outputs may be disabled simultaneously by pulling the GOE pin low or programming EN_CLKout_Global to 0.

1.7 GLOBAL CLOCK OUTPUT SYNCHRONIZATION

The SYNC* synchronizes the clock outputs. When SYNC* is held in a logic low state, the outputs are also held in a logic low state. When SYNC* goes high, the clock outputs are activated and will transition to a high state simultaneously.

SYNC* must be held low for greater than one clock cycle of the Input Channel Bus. Once this low event has been registered, the outputs will not reflect the low state for four more cycles. Similarly once SYNC* becomes high, the outputs will not simultaneously transition high until four more Input Channel Bus clock cycles have passed. See the timing diagram below for further detail.

SYNC* Timing Diagram



1.8 GLOBAL OUTPUT ENABLE AND LOCK DETECT

Each clock output may be individually enabled. Each output enable control bit is gated with the Global Output Enable input pin (GOE) and the Global Output Enable bit (EN_CLKout_Global).

The GOE pin provides an internal pull-up. If it is unterminated externally, the clock output states are determined by the Clock Output Enable bits (CLKoutX_EN).

All clock outputs can be disabled simultaneously if the GOE pin is pulled low by an external signal or EN_CLKout_Global is set to 0.

The Lock Detect (LD) signal can be connected to the GOE pin in which case all outputs are disabled automatically if the synthesizer is not locked.

2.0 General Programming Information

The LMK03000/LMK03000C/LMK03001/LMK03001C devices are programmed using sixteen 32-bit registers which control the device's operation. The registers consist of a data field and an address field. The last 4 register bits, ADDR[3:0] form the address field. The remaining 28 bits form the data field DATA[27:0].

During programming LE is low, serial data is clocked in on the rising edge of clock (MSB first). When LE goes high, data is transferred to the register bank selected by the address field. Only registers R0 to R7 and R13 to R15 need to be programmed for proper device operation.

For the frequency calibration algorithm to work properly OSCin must be driven by a valid signal when R15 is programmed.

2.1 LMK03000/LMK03000C/LMK03001/LMK03001C REGISTER MAP

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data [27:0]																												A3	A2	A1	A0
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout0_MUX [1:0]		CLKout0_EN	CLKout0_DIV [7:0]								CLKout0_DLY [3:0]				0	0	0	0
R1	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout1_MUX [1:0]		CLKout1_EN	CLKout1_DIV [7:0]								CLKout1_DLY [3:0]				0	0	0	1
R2	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout2_MUX [1:0]		CLKout2_EN	CLKout2_DIV [7:0]								CLKout2_DLY [3:0]				0	0	1	0
R3	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout3_MUX [1:0]		CLKout3_EN	CLKout3_DIV [7:0]								CLKout3_DLY [3:0]				0	0	1	1
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout4_MUX [1:0]		CLKout4_EN	CLKout4_DIV [7:0]								CLKout4_DLY [3:0]				0	1	0	0
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout5_MUX [1:0]		CLKout5_EN	CLKout5_DIV [7:0]								CLKout5_DLY [3:0]				0	1	0	1
R6	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout6_MUX [1:0]		CLKout6_EN	CLKout6_DIV [7:0]								CLKout6_DLY [3:0]				0	1	1	0
R7	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout7_MUX [1:0]		CLKout7_EN	CLKout7_DIV [7:0]								CLKout7_DLY [3:0]				0	1	1	1

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R13	0	0	0	0	0	0	1	0	1	0	OSCin_FREQ [7:0]								VCO_ R4_LF [2:0]			VCO_ R3_LF [2:0]			VCO_ C3_C4_LF [3:0]				0	1	0	1
R14	0	0	0	EN_Fout	EN_CLKout_Global	POWERDOWN	0	0	PLL_ MUX [3:0]		PLL_R [11:0]														0	0	0	0	1	1	1	0
R15	PLL_ CP_ GAIN [1:0]		INPUT_DIV [3:0]				PLL_N [17:0]																		0	0	0	0	1	1	1	1

2.2 REGISTER R0 to R7

Registers R0 through R7 control the eight clock output pins. Register R0 controls CLKout0, Register R1 controls CLKout1, and so on. Aside from this, the functions of these bits are identical. The X in CLKoutX_MUX, CLKoutX_DIV, CLKoutX_DLY, and CLKoutX_EN denote the actual clock output which may be from 0 to 7.

2.2.1 CLKoutX_MUX[1:0] -- Clock Output Multiplexers

These bits control the Clock Output Multiplexer for each pin. Changing between the different modes changes the blocks in the signal path and therefore incurs a delay relative to the bypass mode. The different MUX modes and associated delays are listed below.

CLKoutX_MUX[1:0]	Mode	Added Delay Relative to Bypass Mode
0	Bypassed	0 ps
1	Divided	100 ps
2	Delayed	400 ps (In addition to the programmed delay)
3	Divided and Delayed	500 ps (In addition to the programmed delay)

2.2.2 CLKoutX_DIV[7:0] -- Clock Output Dividers

These bits control the clock output divider value. In order for these dividers to be active, the respective CLKoutX_MUX (See 2.2.1) bit must be set to either "Divided" or "Divided and Delayed" mode. After all the dividers are programed, the SYNC* pin must be used to ensure that all edges of the clock output pins are aligned (See 1.7). The Clock Output Dividers follow the Input Divider so the final clock divide for an output is Input Divider x Clock Output Divider. By adding the divider block to the output path a fixed delay of approximately 100 ps is incurred.

The actual Clock Output Divide value is twice the binary value programmed as listed in the table below.

CLKoutX_DIV[7:0]								Clock Output Divider value
0	0	0	0	0	0	0	0	Invalid
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	4
0	0	0	0	0	0	1	1	6
0	0	0	0	0	1	0	0	8
0	0	0	0	0	1	0	1	10
.	.	.	.	.	.	.	.	...
1	1	1	1	1	1	1	1	510

2.2.3 CLKoutX_DLY[3:0] -- Clock Output Delays

These bits control the delay stages for each clock output pin. In order for these delays to be active, the respective CLKoutX_MUX (See 2.2.1) bit must be set to either "Delayed" or "Divided and Delayed" mode. By adding the delay block to the output path a fixed delay of approximately 400 ps is incurred in addition to the delay shown in the table below.

CLKoutX_DLY[3:0]	Delay (ps)
0	0
1	150
2	300
3	450
4	600
5	750
6	900
7	1050
8	1200
9	1350
10	1500
11	1650
12	1800
13	1950
14	2100
15	2250

2.2.4 CLKoutX_EN bit -- Clock Output Enables

This bit controls whether each clock output is enabled or not. If the EN_CLKout_Global bit (See 2.4.4) is set to zero or if GOE pin is held low, all CLKoutX_EN bit states will be ignored and all clock outputs will be disabled.

CLKoutX_EN bit	EN_CLKout_Global bit	GOE pin	Clock X Output State
Don't care	Don't care	0	Disabled
Don't care	0	Don't care	Disabled
0	Don't care	Don't care	Disabled
1	1	High	Enabled

2.3 REGISTER R13

2.3.1 VCO_C3_C4_LF[3:0] -- Value for Internal Loop Filter Capacitors C3 and C4

These bits control the capacitor values for C3 and C4 in the internal loop filter.

VCO_C3_C4_LF[3:0]	Loop Filter Capacitors	
	C3 (pF)	C4 (pF)
0	0	10
1	0	60
2	50	10
3	0	110
4	50	110
5	100	110
6	0	160
7	50	160
8	100	10
9	100	60
10	150	110
11	150	60
12 to 15	Invalid	

2.3.2 VCO_R3_LF[2:0] -- Value for Internal Loop Filter Resistor R3

These bits control the R3 resistor value in the internal loop filter. The recommended setting for VCO_R3_LF[2:0] = 0 for optimum phase noise and jitter.

VCO_R3_LF[2:0]	R3 Value (kΩ)
0	Low (< 100 Ω)
1	10
2	20
3	30
4	40
5 to 7	Invalid

2.3.3 VCO_R4_LF[2:0] -- Value for Internal Loop Filter Resistor R4

These bits control the R4 resistor value in the internal loop filter. The recommended setting for VCO_R4_LF[2:0] = 0 for optimum phase noise and jitter.

VCO_R4_LF[2:0]	R4 Value (kΩ)
0	Low (< 100 Ω)
1	10
2	20
3	30
4	40
5 to 7	Invalid

2.3.4 OSCin_FREQ[7:0] -- Oscillator Input Calibration Adjustment

These bits are to be programmed to the OSCin frequency. If the OSCin frequency is not an integral multiple of 1 MHz, then round to the closest value.

OSCin_FREQ[7:0]	OSCin Frequency
1	1 MHz
2	2 MHz
...	...
200	200 MHz
201 to 255	Invalid

2.4 REGISTER R14

2.4.1 PLL_R[11:0] -- R Divider Value

These bits program the PLL R Divider and are programmed in binary fashion.

PLL_R[11:0]												PLL R Divide Value
0	0	0	0	0	0	0	0	0	0	0	0	Invalid
0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	1	0	2
.	.	.	.	.	.	.	.	.	.	.	.	...
1	1	1	1	1	1	1	1	1	1	1	1	4095

2.4.2 PLL_MUX[3:0] -- Multiplexer Control for LD Pin

These bits set the output mode of the LD pin. The table below lists several different modes.

PLL_MUX[3:0]	Output Type	LD Pin Function
0	Hi-Z	Disabled
1	Push-Pull	Logic High
2	Push-Pull	Logic Low
3	Push-Pull	Digital Lock Detect (Active High)
4	Push-Pull	Digital Lock Detect (Active Low)
5	Push-Pull	Analog Lock Detect
6	Open Drain NMOS	Analog Lock Detect
7	Open Drain PMOS	Analog Lock Detect
8	Push-Pull	N Divider Output (Very Low Duty Cycle)
9	Push-Pull	N Divider Output/2 (50% Duty Cycle)
10	Push-Pull	R Divider Output (Very Low Duty Cycle)
11	Push-Pull	R Divider Output/2 (50% Duty Cycle)
12 to 15	Invalid	

2.4.3 POWERDOWN bit -- Device Power Down

This bit can power down the device. Enabling this bit powers down the entire chip and all blocks, regardless of the state of any of the other bits or pins.

POWERDOWN bit	Mode
0	Normal Operation
1	Entire Chip Powered Down

2.4.4 EN_CLKout_Global bit -- Global Clock Output Enable

This bit overrides the individual CLKoutX_EN bits (See 2.2.4). When this bit is set to 0, all clock outputs are disabled, regardless of the state of any of the other bits or pins.

EN_CLKout_Global bit	Clock Outputs
0	All Disabled
1	Normal Operation

2.4.5 EN_Fout bit -- Fout port enable

This bit enables the Fout pin.

EN_Fout bit	Fout Pin Status
0	Disabled
1	Enabled

2.5 Register R15

2.5.1 PLL_N[17:0] -- PLL N Divider

These bits program the divide value for the PLL N Divider. The PLL N Divider follows the Input Divider and precedes the PLL phase detector. Since the Input Divider is also in the feedback path from the VCO to the PLL Phase Detector, the total N divide value, N_{Total}, is also influenced by the Input Divider value. N_{Total} = PLL N Divider * Input Divider. The VCO frequency is calculated as, $f_{VCO} = f_{OSCin}$ * PLL N Divider * Input Divider / R. Since the PLL N divider is a pure binary counter, there are no illegal divide values for PLL_N[17:0].

PLL_N[17:0]																		PLL N Divider Value
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	262143

2.5.2 INPUT_DIV[3:0] -- Input Divider

These bits program the divide value for the Input Divider. The Input Divider follows the VCO output and precedes the clock distribution blocks. Since the Input Divider is in the feedback path from the VCO to the PLL phase detector the Input Divider contributes to the total N divide value, N_{Total}. N_{Total} = PLL N Divider * Input Divider. The Input Divider can not be bypassed. See 2.5.1 (PLL N Divider) for more information on setting the VCO frequency.

INPUT_DIV[3:0]				Input Divider Value
0	0	0	0	Invalid
0	0	0	1	Invalid
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	Invalid
.	.	.	.	...
1	1	1	1	Invalid

2.5.3 PLL_CP_GAIN[1:0] -- PLL Charge Pump Gain

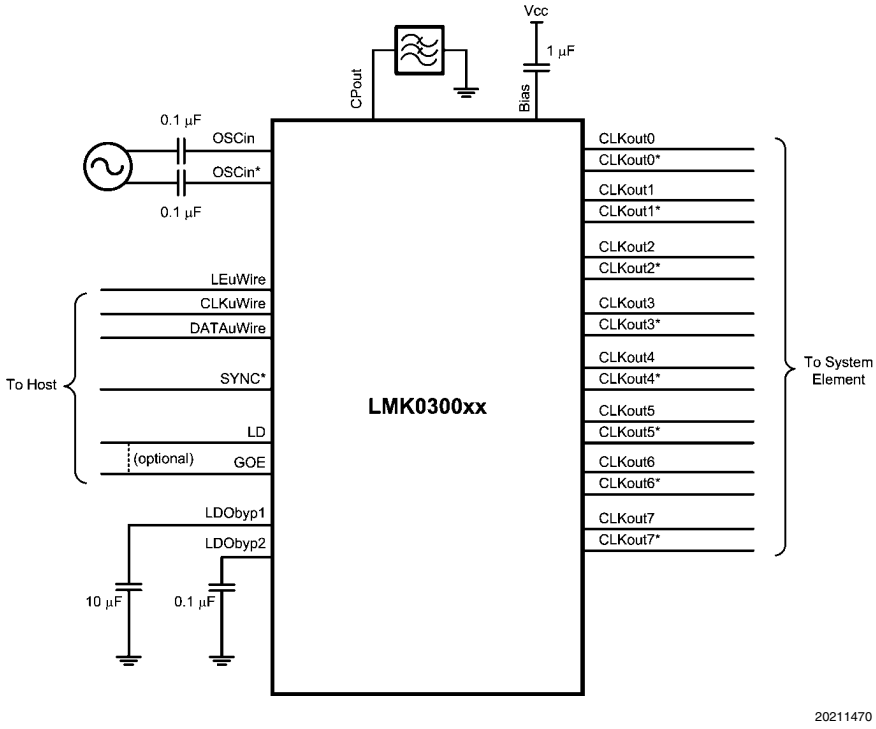
These bits set the charge pump gain of the PLL.

PLL_CP_GAIN[1:0]	Charge Pump Gain
0	1x
1	4x
2	16x
3	32x

3.0 Application Information

3.1 System Level Diagram

The following shows the LMK300xx in a typical application. In this setup the clock may be multiplied, reconditioned, and redistributed. The first and second pole of the loop filter are external. The third and fourth poles are integrated.



3.2 Bias Pin

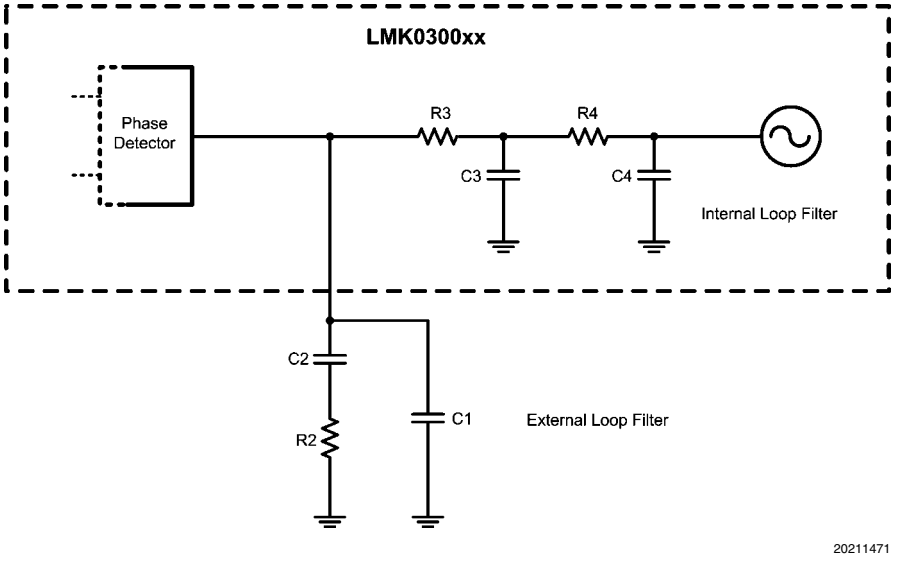
To properly use the device, bypass Bias (pin 36) with a low leakage 1 µF capacitor connected to Vcc. This is important for low noise performance.

3.3 LDO bypass

To properly use the device, bypass LDObyp1 (pin 9) with a 10 µF capacitor and LDObyp2 (pin 10) with a 0.1 µF capacitor.

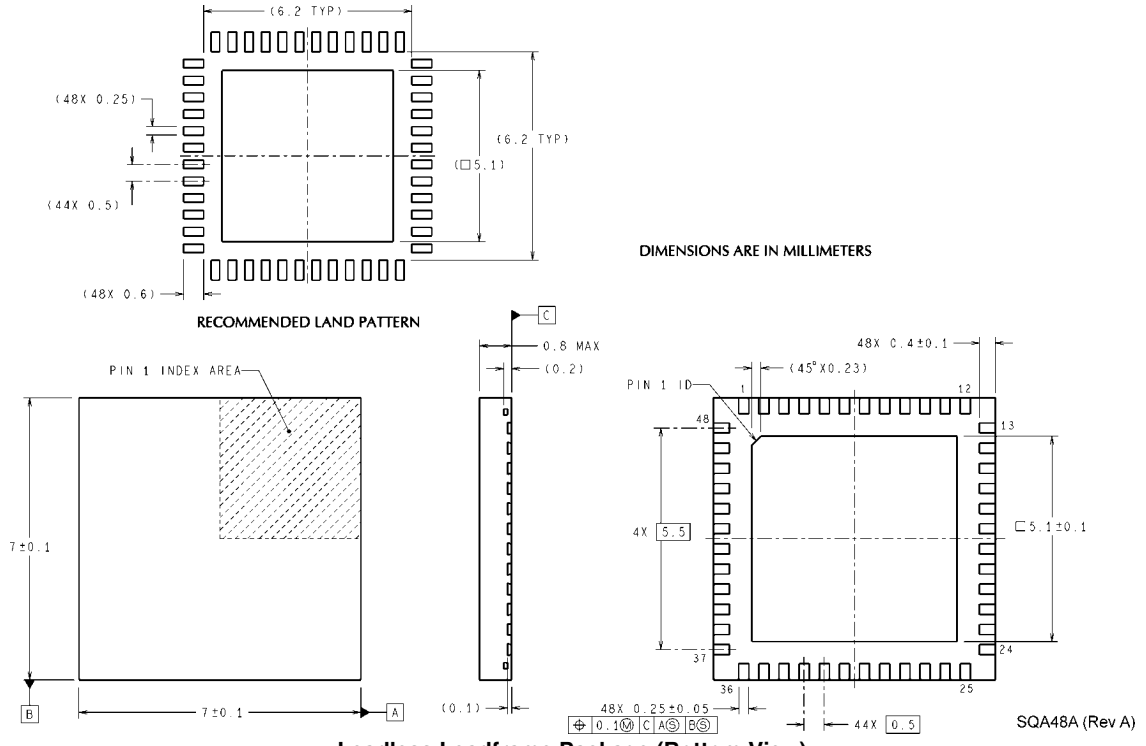
3.4 Loop Filter

The internal charge pump is directly connected to the integrated loop filter components. The first and second pole of the loop filter are externally attached as shown in the diagram below. When the loop filter is designed, it must be stable over the entire frequency band, meaning that the changes in K_{Vtune} from the low to high band specification will not make the loop filter unstable.



20211471

Physical Dimensions inches (millimeters) unless otherwise noted



Leadless Leadframe Package (Bottom View)
48 Pin LLP (SQA48A) Package

Ordering Information

Order Number	Package Marking	Packing	VCO Version	Performance Grade	LVDS Outputs	LVPECL Outputs
LMK03000	K03000 I	1000 Unit Tape and Reel	1.24 GHz	800 fs	3	5
LMK03000X	K03000 I	4000 Unit Tape and Reel	1.24 GHz	800 fs	3	5
LMK03001	K03001 I	1000 Unit Tape and Reel	1.52 GHz	800 fs	3	5
LMK03001X	K03001 I	4000 Unit Tape and Reel	1.52 GHz	800 fs	3	5
LMK03000C	K03000CI	1000 Unit Tape and Reel	1.24 GHz	400 fs	3	5
LMK03000CX	K03000CI	4000 Unit Tape and Reel	1.24 GHz	400 fs	3	5
LMK03001C	K03001CI	1000 Unit Tape and Reel	1.52 GHz	400 fs	3	5
LMK03001CX	K03001CI	4000 Unit Tape and Reel	1.52 GHz	400 fs	3	5

Notes

Notes

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