

## LMK03002/LMK03002C Precision Clock Conditioner with Integrated VCO

### General Description

The LMK03002/LMK03002C precision clock conditioners combine the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The devices integrate a Voltage Controlled Oscillator (VCO), a high performance Integer-N Phase Locked Loop (PLL), a partially integrated loop filter, and four LVPECL clock output distribution blocks.

The VCO output is optionally accessible on the Fout port. Internally, the VCO output goes through a VCO Divider to feed the various clock distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to four system components.

The clock conditioners come in a 48-pin LLP package and are footprint compatible with other clocking devices in the same family.

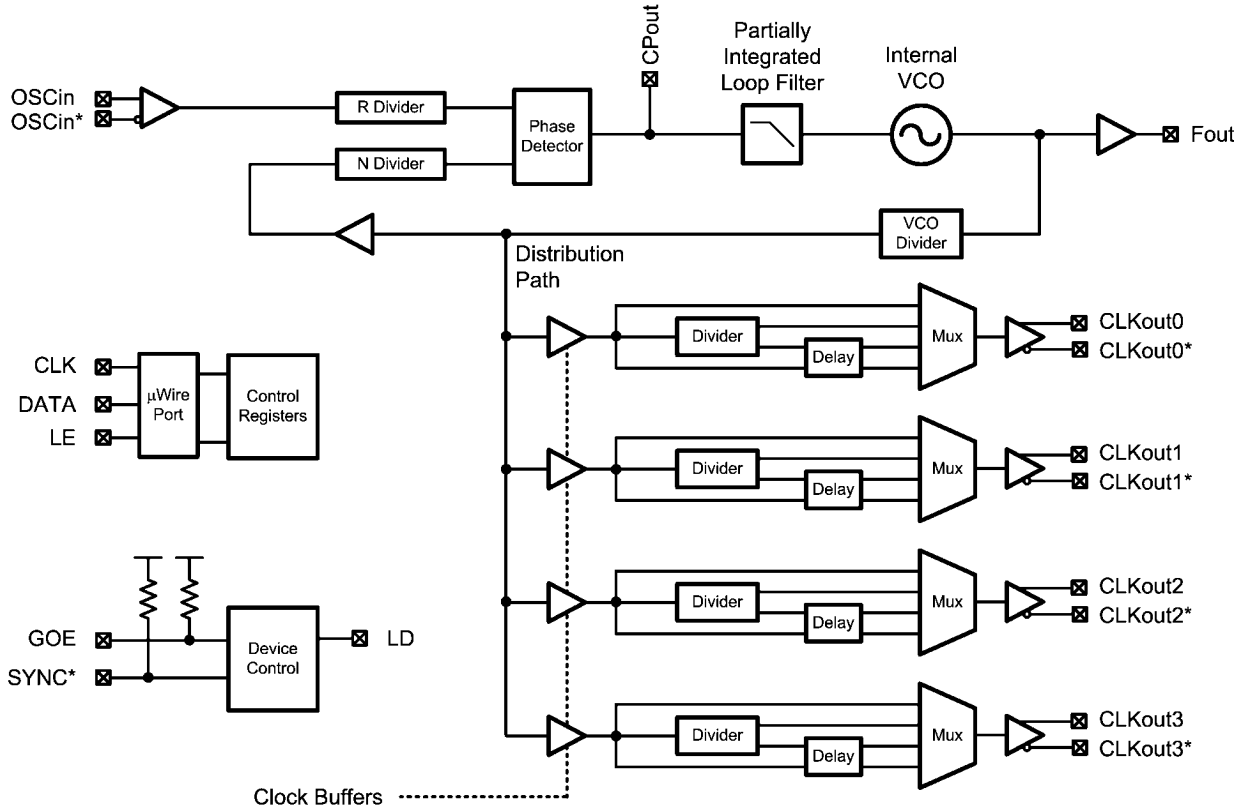
### Features

- Integrated VCO with very low phase noise floor
- Integrated Integer-N PLL with outstanding normalized phase noise contribution of -224 dBc/Hz
- Clock generator performance (10 Hz - 20 MHz)
  - LMK03002C: 200 fs RMS jitter
- Jitter cleaner performance grade (12 kHz to 20 MHz)
  - LMK03002: 800 fs RMS jitter
  - LMK03002C: 400 fs RMS jitter
- VCO frequency: 1566 to 1724 MHz
- Clock output frequency range of 1 to 862 MHz
- 4 LVPECL clock outputs
- Partially integrated loop filter
- Dedicated divider and delay blocks on each clock output
- Pin compatible family of clocking devices
- 3.15 to 3.45 V operation
- Package: 48 pin LLP (7.0 x 7.0 x 0.8 mm)

### Target Applications

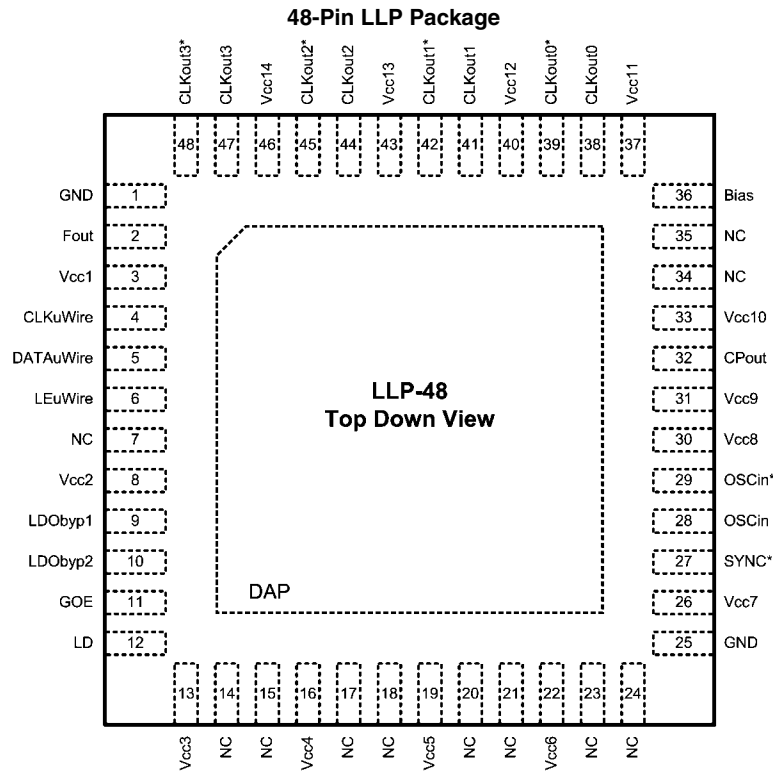
- Data Converter Clocking
- Networking, SONET/SDH, DSLAM
- Wireless Infrastructure
- Medical
- Test and Measurement
- Military / Aerospace

# Functional Block Diagram



30020601

# Connection Diagram



## Pin Descriptions

| Pin #  | Pin Name  | I/O | Description                                |
|--|---|-----|--|
| 1, 25  | GND   | -   | Ground                                     |
| 2  | Fout  | O   | Internal VCO Frequency Output              |
| 3, 8, 13, 16, 19, 22, 26, 30, 31, 33, 37, 40, 43, 46 | Vcc1, Vcc2, Vcc3, Vcc4, Vcc5, Vcc6, Vcc7, Vcc8, Vcc9, Vcc10, Vcc11, Vcc12, Vcc13, Vcc14 | -   | Power Supply                               |
| 4  | CLKuWire  | I   | MICROWIRE Clock Input                      |
| 5  | DATAuWire   | I   | MICROWIRE Data Input                       |
| 6  | LEuWire   | I   | MICROWIRE Latch Enable Input               |
| 7, 14, 15, 17, 18, 20, 21, 23, 24, 34, 35            | NC  | -   | No Connection to these pins                |
| 9, 10  | LDObyp1, LDObyp2  | -   | LDO Bypass                                 |
| 11   | GOE   | I   | Global Output Enable                       |
| 12   | LD  | O   | Lock Detect and Test Output                |
| 27   | SYNC*   | I   | Global Clock Output Synchronization        |
| 28, 29   | OSCin, OSCin*   | I   | Oscillator Clock Input; Must be AC coupled |
| 32   | CPout   | O   | Charge Pump Output                         |
| 36   | Bias  | I   | Bias Bypass                                |
| 38, 39   | CLKout0, CLKout0*   | O   | LVPECL Clock Output 0                      |
| 41, 42   | CLKout1, CLKout1*   | O   | LVPECL Clock Output 1                      |
| 44, 45   | CLKout2, CLKout2*   | O   | LVPECL Clock Output 2                      |
| 47, 48   | CLKout3, CLKout3*   | O   | LVPECL Clock Output 3                      |
| DAP  | DAP   | -   | Die Attach Pad is Ground                   |

## Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| Parameter                     | Symbol    | Ratings                    | Units |
|-------------------------------|-----------|----------------------------|-------|
| Power Supply Voltage          | $V_{CC}$  | -0.3 to 3.6                | V     |
| Input Voltage                 | $V_{IN}$  | -0.3 to ( $V_{CC} + 0.3$ ) | V     |
| Storage Temperature Range     | $T_{STG}$ | -65 to 150                 | °C    |
| Lead Temperature (solder 4 s) | $T_L$     | +260                       | °C    |
| Junction Temperature          | $T_J$     | 125                        | °C    |

## Recommended Operating Conditions

| Parameter            | Symbol   | Min  | Typ | Max  | Units |
|----------------------|----------|------|-----|------|-------|
| Ambient Temperature  | $T_A$    | -40  | 25  | 85   | °C    |
| Power Supply Voltage | $V_{CC}$ | 3.15 | 3.3 | 3.45 | V     |

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

**Note 2:** This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of > 2 kV, a MM-ESD of > 200 V, and a CDM-ESD of > 1.2 kV.

## Package Thermal Resistance

| Package              | $\theta_{JA}$ | $\theta_{J-PAD}$ (Thermal Pad) |
|----------------------|---------------|--------------------------------|
| 48-Lead LLP (Note 3) | 27.4° C/W     | 5.8° C/W                       |

**Note 3:** Specification assumes 16 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the LLP. It is recommended that the maximum number of vias be used in the board layout.

## Electrical Characteristics (Note 4)

(3.15 V ≤  $V_{CC}$  ≤ 3.45 V, -40 °C ≤  $T_A$  ≤ 85 °C, Differential Inputs/Outputs; except as specified. Typical values represent most likely parametric norms at  $V_{CC}$  = 3.3 V,  $T_A$  = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed).

| Symbol                      | Parameter  | Conditions   | Min | Typ  | Max | Units |
|-----------------------------|--|--|-----|------|-----|-------|
| <b>Current Consumption</b>  |  |  |     |      |     |       |
| $I_{CC}$                    | Power Supply Current (Note 5)                              | Entire device; CLKout0 & CLKout3 enabled in Bypass Mode      |     | 175  |     | mA    |
|                             |  | Entire device; All Outputs Off (no emitter resistors placed) |     | 86   |     |       |
| $I_{CCPD}$                  | Power Down Current   | POWERDOWN = 1  |     | 1    |     | mA    |
| <b>Reference Oscillator</b> |  |  |     |      |     |       |
| $f_{OSCin\ square}$         | Reference Oscillator Input Frequency Range for Square Wave | AC coupled; Differential ( $V_{OD}$ )                        | 1   |      | 200 | MHz   |
| $V_{OSCin\ square}$         | Square Wave Input Voltage for OSCin and OSCin*             |  | 0.2 |      | 1.6 | Vpp   |
| <b>PLL</b>                  |  |  |     |      |     |       |
| $f_{COMP}$                  | Phase Detector Frequency                                   |  |     |      | 40  | MHz   |
| $I_{SRCECPout}$             | Charge Pump Source Current                                 | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 1x                    |     | 100  |     | μA    |
|                             |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 4x                    |     | 400  |     |       |
|                             |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 16x                   |     | 1600 |     |       |
|                             |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 32x                   |     | 3200 |     |       |

| Symbol                 | Parameter  | Conditions  | Min            | Typ      | Max  | Units      |
|------------------------|--|---|----------------|----------|------|------------|
| <b>PLL (Continued)</b> |  |   |                |          |      |            |
| $I_{SINK\_CPout}$      | Charge Pump Sink Current   | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 1x   |                | -100     |      | $\mu A$    |
|                        |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 4x   |                | -400     |      |            |
|                        |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 16x  |                | -1600    |      |            |
|                        |  | $V_{CPout} = V_{CC}/2$ , PLL_CP_GAIN = 32x  |                | -3200    |      |            |
| $I_{CPout\_TRI}$       | Charge Pump TRI-STATE® Current   | $0.5 V < V_{CPout} < V_{CC} - 0.5 V$  |                | 2        | 10   | nA         |
| $I_{CPout\%MIS}$       | Magnitude of Charge Pump Sink vs. Source Current Mismatch  | $V_{CPout} = V_{CC} / 2$<br>$T_A = 25^\circ C$  |                | 3        |      | %          |
| $I_{CPout\_VTUNE}$     | Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation   | $0.5 V < V_{CPout} < V_{CC} - 0.5 V$<br>$T_A = 25^\circ C$  |                | 4        |      | %          |
| $I_{CPout\_TEMP}$      | Magnitude of Charge Pump Current vs. Temperature Variation   |   |                | 4        |      | %          |
| PN10kHz                | PLL 1/f Noise at 10 kHz Offset (Note 6) Normalized to 1 GHz Output Frequency   | PLL_CP_GAIN = 1x  |                | -117     |      | dBc/Hz     |
|                        |  | PLL_CP_GAIN = 32x   |                | -122     |      |            |
| PN1Hz                  | Normalized Phase Noise Contribution (Note 7)   | PLL_CP_GAIN = 1x  |                | -219     |      | dBc/Hz     |
|                        |  | PLL_CP_GAIN = 32x   |                | -224     |      |            |
| <b>VCO</b>             |  |   |                |          |      |            |
| $f_{Fout}$             | VCO Tuning Range   | LMK03002/LMK03002C  | 1566           |          | 1724 | MHz        |
| $ \Delta T_{CL} $      | Allowable Temperature Drift for Continuous Lock  | After programming R15 for lock, no changes to output configuration are permitted to guarantee continuous lock. (Note 8) |                |          | 125  | $^\circ C$ |
| $P_{Fout}$             | Output Power to a 50 $\Omega$ load driven by Fout  | LMK03002/LMK03002C; $T_A = 25^\circ C$  |                | 2        |      | dBm        |
| $K_{Vtune}$            | Fine Tuning Sensitivity (The lower sensitivity indicates the typical sensitivity at the lower end of the tuning range, the higher sensitivity at the higher end of the tuning range) | LMK03002/LMK03002C  |                | 11 to 15 |      | MHz/V      |
| $J_{RMS\_Fout}$        | Fout RMS Period Jitter   | LMK03002<br>12 kHz to 20 MHz bandwidth  |                | 800      |      | fs         |
|                        |  | LMK03002C<br>12 kHz to 20 MHz bandwidth   |                | 400      |      |            |
| $L(f)_{Fout}$          | Fout Single Side Band Phase Noise  | LMK03002C<br>$f_{Fout} = 1724$ MHz<br>(Note 9)  | 10 kHz Offset  | -89      |      | dBc/Hz     |
|                        |  |   | 100 kHz Offset | -113     |      |            |
|                        |  |   | 1 MHz Offset   | -135     |      |            |
|                        |  |   | 10 MHz Offset  | -155     |      |            |
|                        |  | LMK03002C<br>$f_{Fout} = 1566$ MHz<br>(Note 9)  | 10 kHz Offset  | -91      |      |            |
|                        |  |   | 100 kHz Offset | -115     |      |            |
|                        |  |   | 1 MHz Offset   | -137     |      |            |
|                        |  |   | 10 MHz Offset  | -156     |      |            |

| Symbol   | Parameter                     | Conditions  | Min  | Typ           | Max | Units |
|--|-------------------------------|---|--|---------------|-----|-------|
| <b>Clock Distribution Section (Note 10) - LVPECL Clock Outputs</b> |                               |   |  |               |     |       |
| Jitter <sub>ADD</sub>  | Additive RMS Jitter (Note 10) | R <sub>L</sub> = 100 Ω<br>Distribution Path =<br>800 MHz<br>Bandwidth =<br>12 kHz to 20 MHz | CLKoutX_MUX<br>= Bypass                        |               | 20  | fs    |
|  |                               |   | CLKoutX_MUX<br>= Divided<br>CLKoutX_DIV =<br>4 |               | 75  |       |
| t <sub>SKEW</sub>  | CLKoutX to CLKoutY (Note 11)  | Equal loading and identical clock<br>configuration<br>Termination = 50 Ω to Vcc - 2 V       | -30  | ±3            | 30  | ps    |
| V <sub>OH</sub>  | Output High Voltage           | Termination = 50 Ω to Vcc - 2 V<br>CLKoutX output frequency = 200 MHz                       |  | Vcc -<br>0.98 |     | V     |
| V <sub>OL</sub>  | Output Low Voltage            |   |  | Vcc -<br>1.8  |     | V     |
| V <sub>OD</sub>  | Differential Output Voltage   |   | 660  | 810           | 965 | mV    |

| <b>Digital LVTTTL Interfaces (Note 12)</b> |                           |                           |       |              |     |    |
|--|---------------------------|---------------------------|-------|--------------|-----|----|
| V <sub>IH</sub>                            | High-Level Input Voltage  |                           | 2.0   |              | Vcc | V  |
| V <sub>IL</sub>                            | Low-Level Input Voltage   |                           |       |              | 0.8 | V  |
| I <sub>IH</sub>                            | High-Level Input Current  | V <sub>IH</sub> = Vcc     | -5.0  |              | 5.0 | µA |
| I <sub>IL</sub>                            | Low-Level Input Current   | V <sub>IL</sub> = 0       | -40.0 |              | 5.0 | µA |
| V <sub>OH</sub>                            | High-Level Output Voltage | I <sub>OH</sub> = +500 µA |       | Vcc -<br>0.4 |     | V  |
| V <sub>OL</sub>                            | Low-Level Output Voltage  | I <sub>OL</sub> = -500 µA |       |              | 0.4 | V  |

| <b>Digital MICROWIRE Interfaces (Note 13)</b> |                          |                       |      |  |     |    |
|---|--------------------------|-----------------------|------|--|-----|----|
| V <sub>IH</sub>                               | High-Level Input Voltage |                       | 1.6  |  | Vcc | V  |
| V <sub>IL</sub>                               | Low-Level Input Voltage  |                       |      |  | 0.4 | V  |
| I <sub>IH</sub>                               | High-Level Input Current | V <sub>IH</sub> = Vcc | -5.0 |  | 5.0 | µA |
| I <sub>IL</sub>                               | Low-Level Input Current  | V <sub>IL</sub> = 0   | -5.0 |  | 5.0 | µA |

| <b>MICROWIRE Timing</b> |                             |                       |    |  |  |    |
|-------------------------|-----------------------------|-----------------------|----|--|--|----|
| t <sub>CS</sub>         | Data to Clock Set Up Time   | See Data Input Timing | 25 |  |  | ns |
| t <sub>CH</sub>         | Data to Clock Hold Time     | See Data Input Timing | 8  |  |  | ns |
| t <sub>CWH</sub>        | Clock Pulse Width High      | See Data Input Timing | 25 |  |  | ns |
| t <sub>CWL</sub>        | Clock Pulse Width Low       | See Data Input Timing | 25 |  |  | ns |
| t <sub>ES</sub>         | Clock to Enable Set Up Time | See Data Input Timing | 25 |  |  | ns |
| t <sub>CES</sub>        | Enable to Clock Set Up Time | See Data Input Timing | 25 |  |  | ns |
| t <sub>EWH</sub>        | Enable Pulse Width High     | See Data Input Timing | 25 |  |  | ns |

**Note 4:** The Electrical Characteristics table lists guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 5:** See 3.5 for more current consumption / power dissipation calculation information.

**Note 6:** A specification in modeling PLL in-band phase noise is the 1/f flicker noise, L<sub>PLL\_flicker</sub>(f), which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10kHz = L<sub>PLL\_flicker</sub>(10 kHz) - 20log(Fout / 1 GHz), where L<sub>PLL\_flicker</sub>(f) is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure L<sub>PLL\_flicker</sub>(f) it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). L<sub>PLL\_flicker</sub>(f) can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL inband phase noise performance is the sum of L<sub>PLL\_flicker</sub>(f) and L<sub>PLL\_flat</sub>(f).

**Note 7:** A specification in modeling PLL in-band phase noise is the Normalized Phase Noise Contribution, L<sub>PLL\_flat</sub>(f), of the PLL and is defined as PN1Hz = L<sub>PLL\_flat</sub>(f) - 20log(N) - 10log(f<sub>COMP</sub>). L<sub>PLL\_flat</sub>(f) is the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth and f<sub>COMP</sub> is the phase detector frequency of the synthesizer. L<sub>PLL\_flat</sub>(f) contributes to the total noise, L(f). To measure L<sub>PLL\_flat</sub>(f) the offset frequency, f, must be chosen sufficiently smaller than the loop bandwidth of the PLL, and yet large enough to avoid a substantial noise contribution from the reference and flicker noise. L<sub>PLL\_flat</sub>(f) can be masked by the reference oscillator performance if a low power or noisy source is used.

**Note 8:** Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction and stay in lock from the ambient temperature and programmed state at which the device was when register R15 was programmed. The action of programming the R15 register, even to the same value, activates a frequency calibration routine. This implies that the device will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reprogram the R15 register to ensure that the device stays in lock. Regardless of what temperature the device was initially programmed at, the ambient temperature can never drift outside the range of -40 °C ≤ T<sub>A</sub> ≤ 85 °C without violating specifications. For this specification to be valid, the programmed state of the device must not change after R15 is programmed.

**Note 9:** VCO phase noise is measured assuming the VCO is the dominant noise source due to a 75 Hz loop bandwidth. Over frequency, the phase noise typically varies by 1 to 2 dB, with the worst case performance typically occurring at the highest frequency. Over temperature, the phase noise typically varies by 1 to 2 dB, assuming the device is not reprogrammed. Reprogramming R15 will run the frequency calibration routine for optimum phase noise.

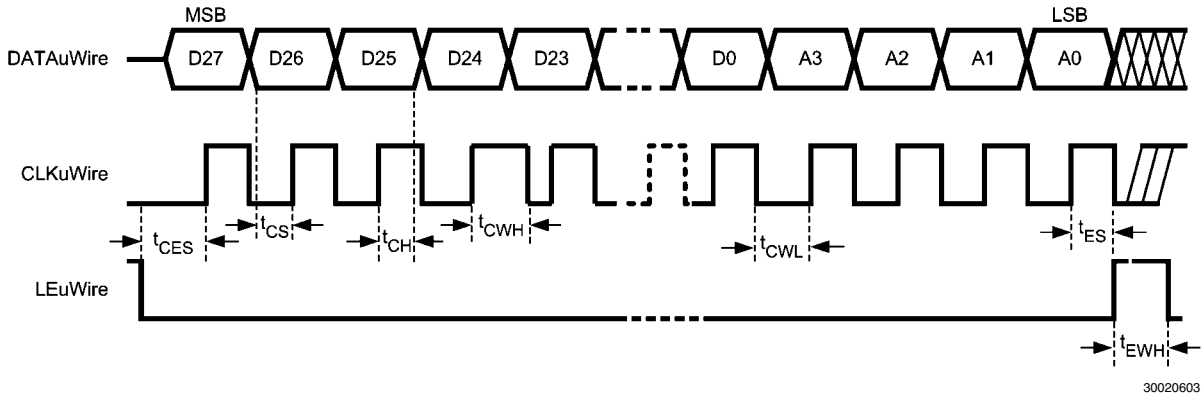
**Note 10:** The Clock Distribution Section includes all parts of the device except the PLL and VCO sections. Typical Additive Jitter specifications apply to the clock distribution section only and is in RMS form addition to the jitter from the VCO.

**Note 11:** Specification is guaranteed by characterization and is not tested in production.

**Note 12:** Applies to GOE, LD, and SYNC\*.

**Note 13:** Applies to CLKuWire, DATAuWire, and LEuWire.

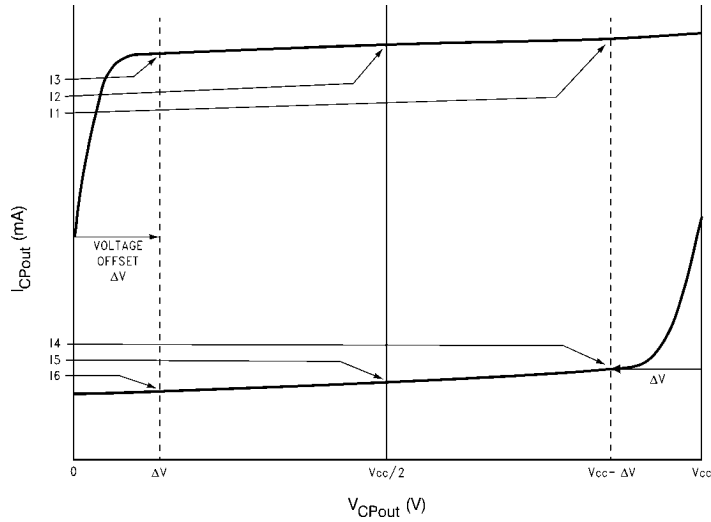
## Serial Data Timing Diagram



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Data bits set on the DATAuWire signal are clocked into a shift register, MSB first, on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the data is sent from the shift register to the addressed register determined by the LSB bits. After the programming is complete the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state.

## Charge Pump Current Specification Definitions



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I1 = Charge Pump Sink Current at  $V_{CPout} = V_{cc} - \Delta V$

I2 = Charge Pump Sink Current at  $V_{CPout} = V_{cc}/2$

I3 = Charge Pump Sink Current at  $V_{CPout} = \Delta V$

I4 = Charge Pump Source Current at  $V_{CPout} = V_{cc} - \Delta V$

I5 = Charge Pump Source Current at  $V_{CPout} = V_{cc}/2$

I6 = Charge Pump Source Current at  $V_{CPout} = \Delta V$

$\Delta V$  = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

### Charge Pump Output Current Magnitude Variation vs. Charge Pump Output Voltage

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

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### Charge Pump Sink Current vs. Charge Pump Output Source Current Mismatch

$$I_{CPout} \text{ Sink Vs } I_{CPout} \text{ Source} = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

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### Charge Pump Output Current Magnitude Variation vs. Temperature

$$I_{CPout} \text{ Vs } T_A = \frac{|I2|_{T_A} - |I2|_{T_A=25^\circ C}}{|I2|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I5|_{T_A} - |I5|_{T_A=25^\circ C}}{|I5|_{T_A=25^\circ C}} \times 100\%$$

30020634



## 1.0 Functional Description

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The LMK03002/LMK03002C precision clock conditioners combine the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The devices integrate a Voltage Controlled Oscillator (VCO), a high performance Integer-N Phase Locked Loop (PLL), a partially integrated loop filter, and four LVPECL clock output distribution blocks.

The devices include internal 3rd and 4th order poles to simplify loop filter design and improve spurious performance. The 1st and 2nd order poles are off-chip to provide flexibility for the design of various loop filter bandwidths.

The LMK03002/LMK03002C includes a 1.64 GHz VCO. The VCO output is optionally accessible on the Fout port. Internally, the VCO output goes through an VCO Divider to feed the various clock distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to four system components.

The clock conditioners come in a 48-pin LLP package and are footprint compatible with other clocking devices in the same family.

### 1.1 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1  $\mu$ F capacitor connected to Vcc. This is important for low noise performance.

### 1.2 LDO BYPASS

To properly use the device, bypass LDObyp1 (pin 9) with a 10  $\mu$ F capacitor and LDObyp2 (pin 10) with a 0.1  $\mu$ F capacitor.

### 1.3 OSCILLATOR INPUT PORT (OSCin, OSCin\*)

The purpose of OSCin is to provide the PLL with a reference signal. The OSCin port must be AC coupled, refer to the System Level Diagram in the Application Information section. The OSCin port may be driven single endedly by AC grounding OSCin\* with a 0.1  $\mu$ F capacitor.

### 1.4 LOW NOISE, FULLY INTEGRATED VCO

The LMK03002/LMK03002C devices contain a fully integrated VCO. In order for proper operation the VCO uses a frequency calibration algorithm. The frequency calibration algorithm is activated any time that the R15 register is programmed. Once R15 is programmed the temperature may not drift more than the maximum allowable drift for continuous lock,  $\Delta T_{CL}$ , or else the VCO is not guaranteed to stay in lock. For the frequency calibration algorithm to work properly OSCin must be driven by a valid signal when R15 is programmed.

### 1.5 CLKout DELAYS

Each individual clock output includes a delay adjustment. Clock output delay registers (CLKoutX\_DLY) support a 150 ps step size and range from 0 to 2250 ps of total delay.

### 1.6 LVPECL OUTPUTS

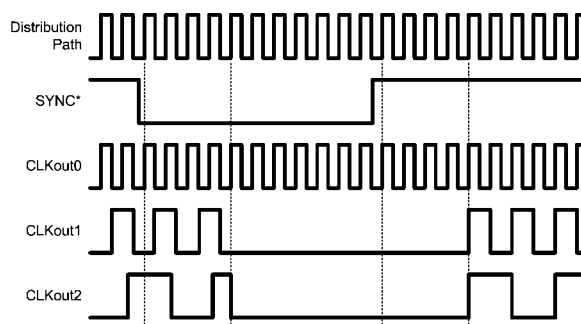
Each LVPECL output may be disabled individually by programming the CLKoutX\_EN bits. All the outputs may be disabled simultaneously by pulling the GOE pin low or programming EN\_CLKout\_Global to 0.

### 1.7 GLOBAL CLOCK OUTPUT SYNCHRONIZATION

The SYNC\* pin synchronizes the clock outputs. When the SYNC\* pin is held in a logic low state, the divided outputs are also held in a logic low state. When the SYNC\* pin goes high, the divided clock outputs are activated and will transition to a high state simultaneously. Clocks in the bypassed state are not affected by SYNC\* and are always synchronized with the divided outputs.

The SYNC\* pin must be held low for greater than one clock cycle of the output of the VCO Divider, also known as the distribution path. Once this low event has been registered, the outputs will not reflect the low state for four more cycles. Similarly once the SYNC\* pin becomes high, the outputs will not simultaneously transition high until four more distribution path clock cycles have passed. See the timing diagram below for further detail. In the timing diagram below the clocks are programmed as CLKout0\_MUX = Bypassed, CLKout1\_MUX = Divided, CLKout1\_DIV = 2, CLKout2\_MUX = Divided, and CLKout2\_DIV = 4.

#### SYNC\* Timing Diagram



30020604

The SYNC\* pin provides an internal pull-up resistor as shown on the functional block diagram. If the SYNC\* pin is not terminated externally the clock outputs will operate normally. If the SYNC\* function is not used, clock output synchronization is not guaranteed.

### 1.8 CLKout OUTPUT STATES

Each clock output may be individually enabled with the CLKoutX\_EN bits. Each individual output enable control bit is gated with the Global Output Enable input pin (GOE) and the Global Output Enable bit (EN\_CLKout\_Global).

All clock outputs can be disabled simultaneously if the GOE pin is pulled low by an external signal or EN\_CLKout\_Global is set to 0.

| CLKoutX_EN bit | EN_CLKout_Global bit | GOE pin           | Clock X Output State |
|----------------|----------------------|-------------------|----------------------|
| 1              | 1                    | Low               | Low                  |
| Don't care     | 0                    | Don't care        | Off                  |
| 0              | Don't care           | Don't care        | Off                  |
| 1              | 1                    | High / No Connect | Enabled              |

When an LVPECL output is in the Off state, the outputs are at a voltage of approximately 1 volt.

### 1.9 GLOBAL OUTPUT ENABLE AND LOCK DETECT

The GOE pin provides an internal pull-up resistor as shown on the functional block diagram. If it is not terminated externally, the clock output states are determined by the Clock Output Enable bits (CLKoutX\_EN) and the EN\_CLKout\_Global bit.

By programming the PLL\_MUX register to Digital Lock Detect Active High (See 2.6.2), the Lock Detect (LD) pin can be connected to the GOE pin in which case all outputs are set low automatically if the synthesizer is not locked.

### 1.10 POWER ON RESET

When supply voltage to the device increases monotonically from ground to Vcc, the power on reset circuit sets all registers to their default values, see 2.3.1 for more information on default register values. Voltage should be applied to all Vcc pins simultaneously.

## 2.0 General Programming Information

The LMK03002/LMK03002C devices are programmed using several 32-bit registers which control the device's operation. The registers consist of a data field and an address field. The last 4 register bits, ADDR[3:0] form the address field. The remaining 28 bits form the data field DATA[27:0].

During programming, LEuWire is low and serial data is clocked in on the rising edge of CLKuWire (MSB first). When LEuWire goes high, data is transferred to the register bank selected by the address field. Only registers R0, R4 to R8, R11, and R13 to R15 need to be programmed for proper device operation. After programming, CLKuWire, DATAuWire, LEuWire should remain low to prevent spurious.

For the frequency calibration algorithm to work properly OSCin must be driven by a valid signal when R15 is programmed. Any changes to the PLL R divider or OSCin require R15 to be programmed again to activate the frequency calibration routine.

### 2.1 RECOMMENDED PROGRAMMING SEQUENCE

The recommended programming sequence involves programming R0 with the reset bit set (RESET = 1) to ensure the device is in a default state. Registers are programmed in order with R15 being the last register programmed. An example programming sequence is shown below.

- Program R0 with the reset bit set (RESET = 1). This ensures the device is in a default state.
- Program R4 to R7 as necessary with desired clocks with appropriate enable, mux, divider, and delay settings.
- Program R8.
- Program R11 with DIV4 setting if necessary.
- Program R13 with oscillator input frequency and internal loop filter values.
- Program R14 with Fout enable bit, global clock output bit, power down setting, PLL mux setting, and PLL R divider.
- Program R15 with PLL charge pump gain, VCO divider, and PLL N divider. Also starts frequency calibration routine.



LMK03002/LMK03002C

| Register | 31                   | 30 | 29 | 28               | 27               | 26        | 25              | 24 | 23               | 22 | 21 | 20              | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
|----------|----------------------|----|----|------------------|------------------|-----------|-----------------|----|------------------|----|----|-----------------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R14      | 0                    | 0  | 0  | EN_Fout          | EN_CLKout_Global | POWERDOWN | 0               | 0  | PLL_MUX<br>[3:0] |    |    | PLL_R<br>[11:0] |    |    |    |    |    |    |    |    |    |    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R15      | PLL_CP_GAIN<br>[1:0] |    |    | VCO_DIV<br>[3:0] |                  |           | PLL_N<br>[17:0] |    |                  |    |    |                 |    |    |    |    |    | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 2.3 REGISTERS R0, R4 to R7

Registers R4 through R7 control the four clock outputs. Register R3 controls CLKout0, Register R4 controls CLKout1, and so on. There is one additional bit in register R0 called RESET. The X in CLKoutX\_MUX, CLKoutX\_DIV, CLKoutX\_DLY, and CLKoutX\_EN denote the actual clock output which may be from 0 to 3.

#### 2.3.1 RESET bit -- R0 only

This bit is only in register R0. The use of this bit is optional and it should be set to '0' if not used. Setting this bit to a '1'

forces all registers to their power on reset condition and therefore automatically clears this bit. If this bit is set, all other R0 bits are ignored and R0 needs to be programmed again if used with its proper values and RESET = 0.

| Bit Name                | Default Bit Value | Bit State                  | Bit Description                       | Register | Bit Location |
|-------------------------|-------------------|----------------------------|---------------------------------------|----------|--------------|
| RESET                   | 0                 | No reset, normal operation | Reset to power on defaults            | R0       | 31           |
| CLKoutX_MUX             | 0                 | Bypassed                   | CLKoutX mux mode                      | R0 to R7 | 18:17        |
| CLKoutX_EN              | 0                 | Disabled                   | CLKoutX enable                        |          | 16           |
| CLKoutX_DIV             | 1                 | Divide by 2                | CLKoutX clock divide                  |          | 15:8         |
| CLKoutX_DLY             | 0                 | 0 ps                       | CLKoutX clock delay                   |          | 7:4          |
| DIV4                    | 0                 | PDF ≤ 20 MHz               | Phase Detector Frequency              | R11      | 15           |
| OSCI <sub>n</sub> _FREQ | 10                | 10 MHz OSC <sub>in</sub>   | OSCI <sub>n</sub> Frequency in MHz    | R13      | 21:14        |
| VCO_R4_LF               | 0                 | Low (~200 Ω)               | R4 internal loop filter values        |          | 13:11        |
| VCO_R3_LF               | 0                 | Low (~600 Ω)               | R3 internal loop filter values        |          | 10:8         |
| VCO_C3_C4_LF            | 0                 | C3 = 0 pF, C4 = 10 pF      | C3 and C4 internal loop filter values |          | 7:4          |
| EN_Fout                 | 0                 | Fout disabled              | Fout enable                           | R14      | 28           |
| EN_CLKout_Global        | 1                 | Normal - CLKouts normal    | Global clock output enable            |          | 27           |
| POWERDOWN               | 0                 | Normal - Device active     | Device power down                     |          | 26           |
| PLL_MUX                 | 0                 | Disabled                   | Multiplexer control for LD pin        |          | 23:20        |
| PLL_R                   | 10                | R divider = 10             | PLL R divide value                    | R15      | 19:8         |
| PLL_CP_GAIN             | 0                 | 100 uA                     | Charge pump current                   |          | 31:30        |
| VCO_DIV                 | 2                 | Divide by 2                | VCO divide value                      |          | 29:26        |
| PLL_N                   | 760               | N divider = 760            | PLL N divide value                    |          | 25:8         |

#### 2.3.2 CLKoutX\_MUX[1:0] -- Clock Output Multiplexers

These bits control the Clock Output Multiplexer for each clock output. Changing between the different modes changes the blocks in the signal path and therefore incurs a delay relative to the bypass mode. The different MUX modes and associated delays are listed below.

| CLKoutX_MUX [1:0] | Mode                | Added Delay Relative to Bypass Mode             |
|-------------------|---------------------|---|
| 0                 | Bypassed (default)  | 0 ps  |
| 1                 | Divided             | 100 ps  |
| 2                 | Delayed             | 400 ps<br>(In addition to the programmed delay) |
| 3                 | Divided and Delayed | 500 ps<br>(In addition to the programmed delay) |

#### 2.3.3 CLKoutX\_DIV[7:0] -- Clock Output Dividers

These bits control the clock output divider value. In order for these dividers to be active, the respective CLKoutX\_MUX (See 2.3.2) bit must be set to either "Divided" or "Divided and Delayed" mode. After all the dividers are programmed, the

SYNC\* pin must be used to ensure that all edges of the clock outputs are aligned (See 1.7). The Clock Output Dividers follow the VCO Divider so the final clock divide for an output is VCO Divider × Clock Output Divider. By adding the divider block to the output path a fixed delay of approximately 100 ps is incurred.

The actual Clock Output Divide value is twice the binary value programmed as listed in the table below.

| CLKoutX_DIV[7:0] |   |   |   |   |   |   |   | Clock Output Divider value |
|------------------|---|---|---|---|---|---|---|----------------------------|
| 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Invalid                    |
| 0                | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 (default)                |
| 0                | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4                          |
| 0                | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 6                          |
| 0                | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8                          |
| 0                | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10                         |
| .                | . | . | . | . | . | . | . | ...                        |
| 1                | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 510                        |

#### 2.3.4 CLKoutX\_DLY[3:0] -- Clock Output Delays

These bits control the delay stages for each clock output. In order for these delays to be active, the respective CLKoutX\_MUX (See 2.3.2) bit must be set to either "Delayed" or "Divided and Delayed" mode. By adding the delay block to

the output path a fixed delay of approximately 400 ps is incurred in addition to the delay shown in the table below.

| CLKoutX_DLY[3:0] | Delay (ps)  |
|------------------|-------------|
| 0                | 0 (default) |
| 1                | 150         |
| 2                | 300         |
| 3                | 450         |
| 4                | 600         |
| 5                | 750         |
| 6                | 900         |
| 7                | 1050        |
| 8                | 1200        |
| 9                | 1350        |
| 10               | 1500        |
| 11               | 1650        |
| 12               | 1800        |
| 13               | 1950        |
| 14               | 2100        |
| 15               | 2250        |

**2.3.5 CLKoutX\_EN bit -- Clock Output Enables**

These bits control whether an individual clock output is enabled or not. If the EN\_CLKout\_Global bit (See 2.6.4) is set

| DIV4 | Digital Lock Detect Circuitry Mode                       |
|------|--|
| 0    | Not divided; Phase Detector Frequency ≤ 20 MHz (default) |
| 1    | Divided by 4; Phase Detector Frequency > 20 MHz          |

**2.5 REGISTER R13**

**2.5.1 VCO\_C3\_C4\_LF[3:0] -- Value for Internal Loop Filter Capacitors C3 and C4**

These bits control the capacitor values for C3 and C4 in the internal loop filter.

| VCO_C3_C4_LF[3:0] | Loop Filter Capacitors |              |
|-------------------|------------------------|--------------|
|                   | C3 (pF)                | C4 (pF)      |
| 0                 | 0 (default)            | 10 (default) |
| 1                 | 0                      | 60           |
| 2                 | 50                     | 10           |
| 3                 | 0                      | 110          |
| 4                 | 50                     | 110          |
| 5                 | 100                    | 110          |
| 6                 | 0                      | 160          |
| 7                 | 50                     | 160          |
| 8                 | 100                    | 10           |
| 9                 | 100                    | 60           |
| 10                | 150                    | 110          |
| 11                | 150                    | 60           |
| 12 to 15          | Invalid                |              |

**2.5.2 VCO\_R3\_LF[2:0] -- Value for Internal Loop Filter Resistor R3**

These bits control the R3 resistor value in the internal loop filter. The recommended setting for VCO\_R3\_LF[2:0] = 0 for optimum phase noise and jitter.

to zero or if GOE pin is held low, all CLKoutX\_EN bit states will be ignored and all clock outputs will be disabled. See 1.8 for more information on CLKout states.

| CLKoutX_EN bit | Conditions                             | CLKoutX State      |
|----------------|--|--------------------|
| 0              | EN_CLKout_Global                       | Disabled (default) |
| 1              | bit = 1<br>GOE pin = High / No Connect | Enabled            |

**2.4 REGISTER R11**

This register only has one bit and only needs to be programmed in the case that the phase detector frequency is greater than 20 MHz and digital lock detect is used. Otherwise, it is automatically defaulted to the correct values.

**2.4.1 DIV4 -- High Phase Detector Frequencies and Lock Detect**

This bit divides the frequency presented to the digital lock detect circuitry by 4. It is necessary to get a reliable output from the digital lock detect output in the case of a phase detector frequency greater than 20 MHz.

| VCO_R3_LF[2:0] | R3 Value (k $\Omega$ )         |
|----------------|--------------------------------|
| 0              | Low (~600 $\Omega$ ) (default) |
| 1              | 10                             |
| 2              | 20                             |
| 3              | 30                             |
| 4              | 40                             |
| 5 to 7         | Invalid                        |

### 2.5.3 VCO\_R4\_LF[2:0] -- Value for Internal Loop Filter Resistor R4

These bits control the R4 resistor value in the internal loop filter. The recommended setting for VCO\_R4\_LF[2:0] = 0 for optimum phase noise and jitter.

| VCO_R4_LF[2:0] | R4 Value (k $\Omega$ )         |
|----------------|--------------------------------|
| 0              | Low (~200 $\Omega$ ) (default) |
| 1              | 10                             |
| 2              | 20                             |
| 3              | 30                             |
| 4              | 40                             |
| 5 to 7         | Invalid                        |

**2.5.4 OSCin\_FREQ[7:0] -- Oscillator Input Calibration**

**Adjustment**

These bits are to be programmed to the OSCin frequency. If the OSCin frequency is not an integral multiple of 1 MHz, then round to the closest value.

| OSCin_FREQ[7:0] | OSCin Frequency  |
|-----------------|------------------|
| 1               | 1 MHz            |
| 2               | 2 MHz            |
| ...             | ...              |
| 10              | 10 MHz (default) |
| ...             | ...              |
| 200             | 200 MHz          |
| 201 to 255      | Invalid          |

**2.6 REGISTER R14**

**2.6.1 PLL\_R[11:0] -- R Divider Value**

These bits program the PLL R Divider and are programmed in binary fashion. Any changes to PLL\_R require R15 to be programmed again to activate the frequency calibration routine.

| PLL_R[11:0]             | PLL R Divide Value |
|-------------------------|--------------------|
| 0 0 0 0 0 0 0 0 0 0 0 0 | Invalid            |
| 0 0 0 0 0 0 0 0 0 0 0 1 | 1                  |

| PLL_R[11:0]             | PLL R Divide Value |
|-------------------------|--------------------|
| 0 0 0 0 0 0 0 0 0 0 1 0 | 2                  |
| . . . . .               | ...                |
| 0 0 0 0 0 0 0 0 1 0 1 0 | 10 (default)       |
| . . . . .               | ...                |
| 1 1 1 1 1 1 1 1 1 1 1 1 | 4095               |



### 2.6.2 PLL\_MUX[3:0] -- Multiplexer Control for LD Pin

These bits set the output mode of the LD pin. The table below lists several different modes.

| PLL_MUX[3:0] | Output Type     | LD Pin Function                     |
|--------------|-----------------|-------------------------------------|
| 0            | Hi-Z            | Disabled (default)                  |
| 1            | Push-Pull       | Logic High                          |
| 2            | Push-Pull       | Logic Low                           |
| 3            | Push-Pull       | Digital Lock Detect (Active High)   |
| 4            | Push-Pull       | Digital Lock Detect (Active Low)    |
| 5            | Push-Pull       | Analog Lock Detect                  |
| 6            | Open Drain NMOS | Analog Lock Detect                  |
| 7            | Open Drain PMOS | Analog Lock Detect                  |
| 8            | Invalid         |                                     |
| 9            | Push-Pull       | N Divider Output/2 (50% Duty Cycle) |
| 10           | Invalid         |                                     |

| PLL_MUX[3:0] | Output Type | LD Pin Function                     |
|--------------|-------------|-------------------------------------|
| 11           | Push-Pull   | R Divider Output/2 (50% Duty Cycle) |
| 12 to 15     | Invalid     |                                     |

### 2.6.3 POWERDOWN bit -- Device Power Down

This bit can power down the device. Enabling this bit powers down the entire device and all blocks, regardless of the state of any of the other bits or pins.

| POWERDOWN bit | Mode                       |
|---------------|----------------------------|
| 0             | Normal Operation (default) |
| 1             | Entire Device Powered Down |

### 2.6.4 EN\_CLKout\_Global bit -- Global Clock Output Enable

This bit overrides the individual CLKoutX\_EN bits (See 2.3.5). When this bit is set to 0, all clock outputs are disabled, regardless of the state of any of the other bits or pins. See 1.8 for more information on CLKout states.

| EN_CLKout_Global bit | Clock Outputs              |
|----------------------|----------------------------|
| 0                    | All Off                    |
| 1                    | Normal Operation (default) |

### 2.6.5 EN\_Fout bit -- Fout port enable

This bit enables the Fout pin.

| EN_Fout bit | Fout Pin Status    |
|-------------|--------------------|
| 0           | Disabled (default) |
| 1           | Enabled            |

**2.7 Register R15**

Programming R15 also activates the frequency calibration routine.

**2.7.1 PLL\_N[17:0] -- PLL N Divider**

These bits program the divide value for the PLL N Divider. The PLL N Divider follows the VCO Divider and precedes the PLL phase detector. Since the VCO Divider is also in the feedback path from the VCO to the PLL Phase Detector, the total N divide value,  $N_{Total}$ , is also influenced by the VCO Divider value.  $N_{Total} = PLL\ N\ Divider \times VCO\ Divider$ . The VCO frequency is calculated as,  $f_{VCO} = f_{OSCin} \times PLL\ N\ Divider \times VCO\ Divider / PLL\ R\ Divider$ . Since the PLL N divider is a pure binary counter there are no illegal divide values for PLL\_N [17:0] except for 0.

| PLL_N[17:0]                         | PLL N Divider Value |
|-------------------------------------|---------------------|
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Invalid             |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 | 1                   |
| . . . . .                           | ...                 |
| 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 0 0 0 | 760 (default)       |
| . . . . .                           | ...                 |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | 262143              |

**2.7.2 VCO\_DIV[3:0] -- VCO Divider**

These bits program the divide value for the VCO Divider. The VCO Divider follows the VCO output and precedes the clock distribution blocks. Since the VCO Divider is in the feedback path from the VCO to the PLL phase detector the VCO Divider

contributes to the total N divide value,  $N_{Total}$ .  $N_{Total} = PLL\ N\ Divider \times VCO\ Divider$ . The VCO Divider can not be bypassed. See 2.7.1 (PLL N Divider) for more information on setting the VCO frequency.

| VCO_DIV[3:0] |   |   |   | VCO Divider Value |
|--------------|---|---|---|-------------------|
| 0            | 0 | 0 | 0 | Invalid           |
| 0            | 0 | 0 | 1 | Invalid           |
| 0            | 0 | 1 | 0 | 2 (default)       |
| 0            | 0 | 1 | 1 | 3                 |
| 0            | 1 | 0 | 0 | 4                 |
| 0            | 1 | 0 | 1 | 5                 |
| 0            | 1 | 1 | 0 | 6                 |
| 0            | 1 | 1 | 1 | 7                 |
| 1            | 0 | 0 | 0 | 8                 |
| 1            | 0 | 0 | 1 | Invalid           |
| .            | . | . | . | ...               |
| 1            | 1 | 1 | 1 | Invalid           |

**2.7.3 PLL\_CP\_GAIN[1:0] -- PLL Charge Pump Gain**

These bits set the charge pump gain of the PLL.

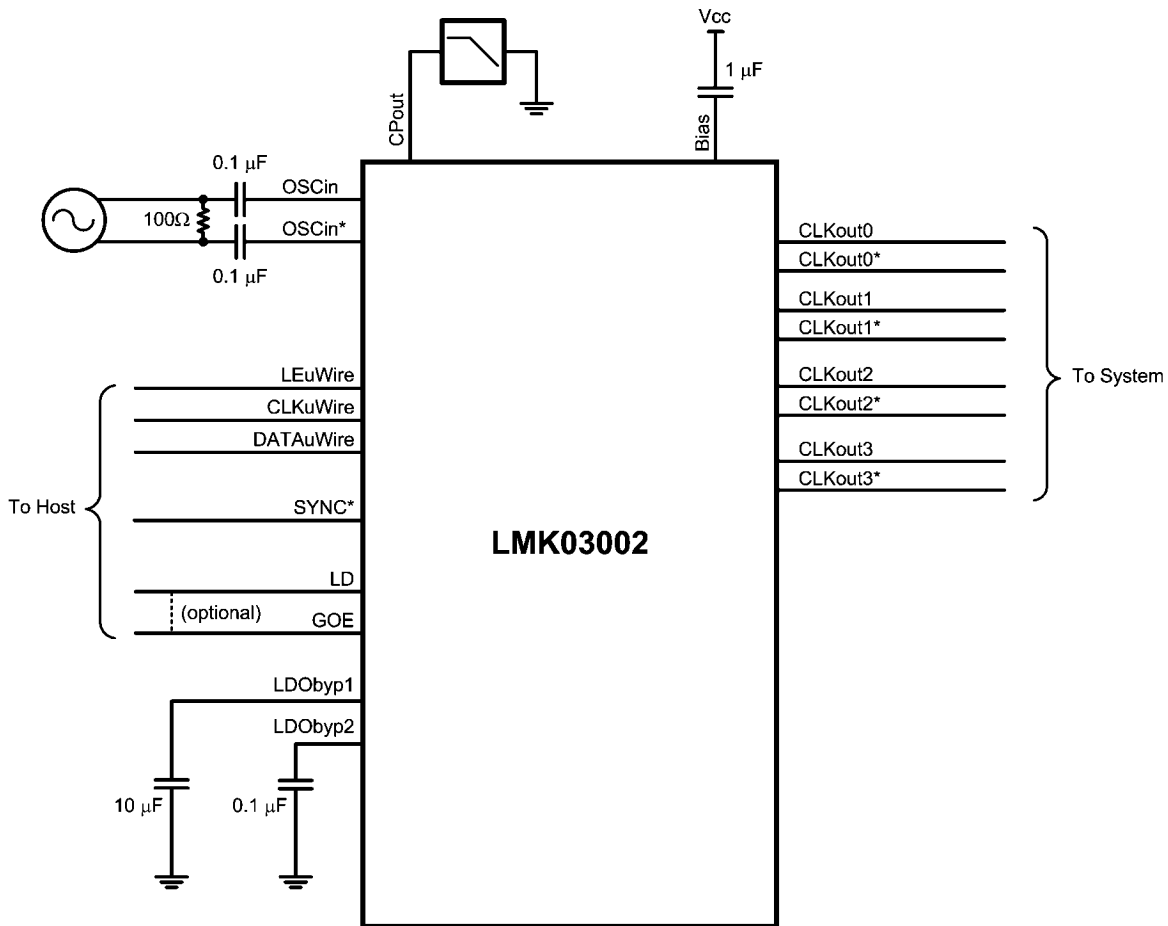
| PLL_CP_GAIN[1:0] | Charge Pump Gain |
|------------------|------------------|
| 0                | 1x (default)     |
| 1                | 4x               |
| 2                | 16x              |
| 3                | 32x              |

### 3.0 Application Information

distributed. The first and second pole of the loop filter are external. The third and fourth poles are integrated.

#### 3.1 SYSTEM LEVEL DIAGRAM

The following shows the LMK300xx in a typical application. In this setup the clock may be multiplied, reconditioned, and re-



30020670

FIGURE 1. Typical Application

#### 3.2 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1 μF capacitor connected to Vcc. This is important for low noise performance.

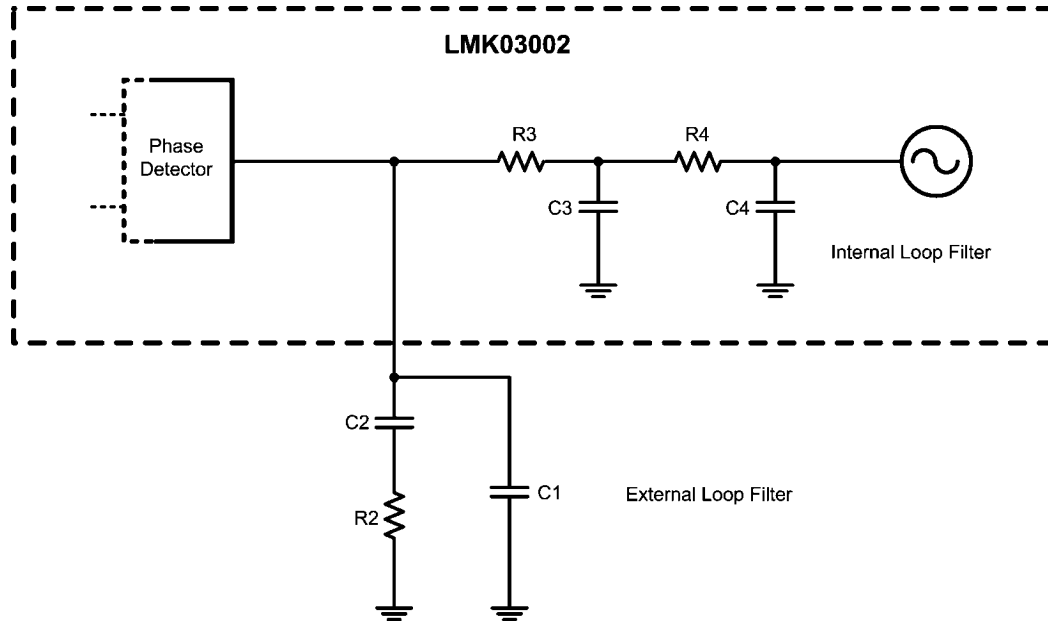
#### 3.3 LDO BYPASS

To properly use the device, bypass LDObyp1 (pin 9) with a 10 μF capacitor and LDObyp2 (pin 10) with a 0.1 μF capacitor.

**3.4 LOOP FILTER**

The internal charge pump is directly connected to the integrated loop filter components. The first and second pole of the loop filter are externally attached as shown in *Figure 2*. When

the loop filter is designed, it must be stable over the entire frequency band, meaning that the changes in  $K_{V_{tune}}$  from the low to high band specification will not make the loop filter unstable.



30020671

**FIGURE 2. Loop Filter**

### 3.5 CURRENT CONSUMPTION / POWER DISSIPATION

calculate estimated current consumption of the device. Unless otherwise noted  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .

#### CALCULATIONS

Due to the myriad of possible configurations the following table serves to provide enough information to allow the user to

**Table 3.5 - Block Current Consumption**

| Block                       | Condition  | Current Consumption at 3.3 V (mA) | Power Dissipated in device (mW) | Power Dissipated in LVPECL emitter resistors (mW) |
|-----------------------------|--|-----------------------------------|---------------------------------|---|
| Entire device, core current | All outputs off; No LVPECL emitter resistors connected                           | 86.0                              | 283.8                           | -   |
| Clock buffers (internal)    | The clock buffers are enabled anytime one of CLKout0 through CLKout3 are enabled | 9                                 | 29.7                            | -   |
| Output buffers              | Fout buffer, EN_Fout = 1   | 14.5                              | 47.8                            | -   |
|                             | LVPECL output, bypass mode (includes 120 $\Omega$ emitter resistors)             | 40                                | 72                              | 60  |
|                             | LVPECL output, disabled mode (includes 120 $\Omega$ emitter resistors)           | 17.4                              | 38.3                            | 19.1  |
|                             | LVPECL output, disabled mode. No emitter resistors placed; open outputs          | 0                                 | 0                               | -   |
| Divide circuitry per output | Divide enabled, divide = 2   | 5.3                               | 17.5                            | -   |
|                             | Divide enabled, divide > 2   | 8.5                               | 28.0                            | -   |
| Delay circuitry per output  | Delay enabled, delay < 8   | 5.8                               | 19.1                            | -   |
|                             | Delay enabled, delay > 7   | 9.9                               | 32.7                            | -   |
| Entire device               | CLKout0 & CLKout3 enabled in bypass mode   | 175                               | 457.5                           | 120   |

From Table 3.5 the current consumption can be calculated in any configuration. For example, the current for the entire device with two LVPECL (CLKout0 and CLKout3) outputs in bypass mode can be calculated by adding up the following blocks: core current, clock buffers, and two LVPECL output buffer currents. There will also be two LVPECL outputs drawing emitter current, but some of the power from the current draw is dissipated in the external 120  $\Omega$  resistors which doesn't add to the power dissipation budget for the device. If delays or divides are switched in, then the additional current for these stages needs to be added as well.

For power dissipated by the device, the total current entering the device is multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs. If no emitter resistors are connected to the LVPECL outputs, this power will be 0 watts. For example, in the case of two LVPECL (CLKout0 & CLKout3) outputs operating at 3.3 volts, we calculate  $3.3\text{ V} \times (86 + 9 + 40 + 40)\text{ mA} = 3.3\text{ V} \times 175\text{ mA} = 577.5\text{ mW}$ . Because two LVPECL outputs (CLKout0 and CLKout3) have the emitter resistors hooked up and the power dissipated by these resistors is 60 mW for each clock, the total device power dissipation is  $533.9\text{ mW} - 120\text{ mW} = 457.5\text{ mW}$ .

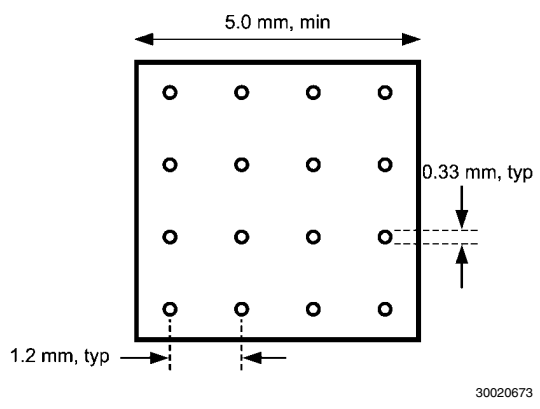
When the LVPECL output is active,  $\sim 1.9\text{ V}$  is the average voltage on each output as calculated from the LVPECL  $V_{OH}$

&  $V_{OL}$  typical specification. Therefore the power dissipated in each emitter resistor is approximately  $(1.9\text{ V})^2 / 120\text{ } \Omega = 30\text{ mW}$ . When the LVPECL output is disabled, the emitter resistor voltage is  $\sim 1.07\text{ V}$ . Therefore the power dissipated in each emitter resistor is approximately  $(1.07\text{ V})^2 / 120\text{ } \Omega = 9.5\text{ mW}$ .

### 3.6 THERMAL MANAGEMENT

Power consumption of the LMK03002/LMK03002C devices can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125  $^\circ\text{C}$ . That is, as an estimate,  $T_A$  (ambient temperature) plus device power consumption times  $\theta_{JA}$  should not exceed 125  $^\circ\text{C}$ .

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in *Figure 3*. More information on soldering LLP packages can be obtained at [www.national.com](http://www.national.com).



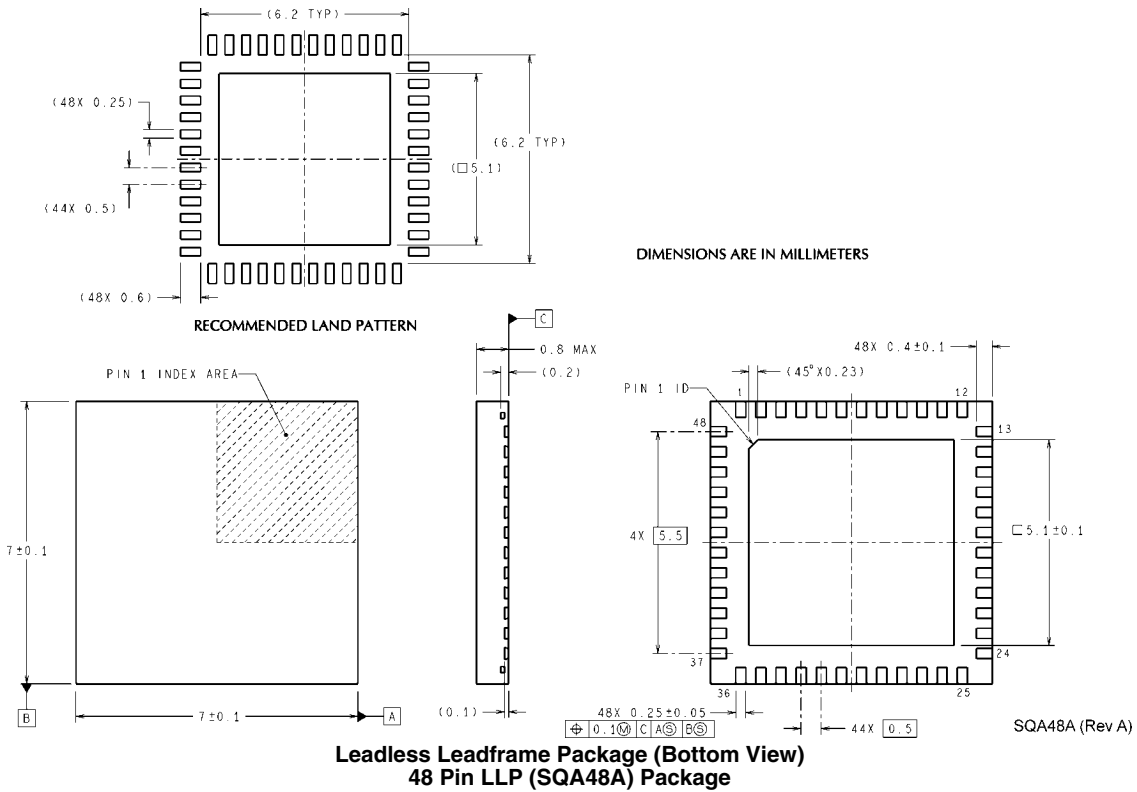
**FIGURE 3. Recommended Land and Via Pattern**

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if

possible), which could provide thermal insulation. The vias shown in *Figure 3* should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

**Physical Dimensions** inches (millimeters) unless otherwise noted

www.DataSheet4U.com



**Ordering Information**

| Order Number  | Package Marking | Packing                 | VCO Version | Performance Grade | LVPECL Outputs |
|---------------|-----------------|-------------------------|-------------|-------------------|----------------|
| LMK03002ISQ   | K03002 I        | 250 Unit Tape and Reel  | 1.64 GHz    | 800 fs            | 4              |
| LMK03002ISQX  | K03002 I        | 2500 Unit Tape and Reel | 1.64 GHz    | 800 fs            | 4              |
| LMK03002CISQ  | K03002CI        | 250 Unit Tape and Reel  | 1.64 GHz    | 400 fs            | 4              |
| LMK03002CISQX | K03002CI        | 2500 Unit Tape and Reel | 1.64 GHz    | 400 fs            | 4              |

## Notes

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