LMN1072KTFF 20V N-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}$ = 350mΩ @V_{GS} =4.5V
- $R_{DS(ON)}$ = 450mΩ @V_{GS} =2.5V
- $R_{DS(ON)}$ = 700mΩ @V_{GS} =1.8V
- $R_{DS(ON)}$= 1200mΩ@V_{GS} =1.5V
- ESD Protected
- DFN1006-3L Package design

Product Description

LMN1072 KTFF, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent RDS(ON), low gate charge.

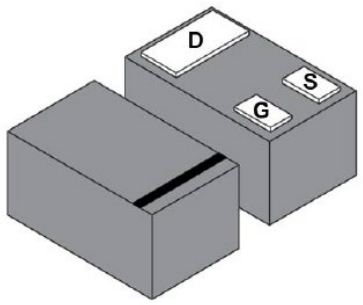
The device is particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

Applications

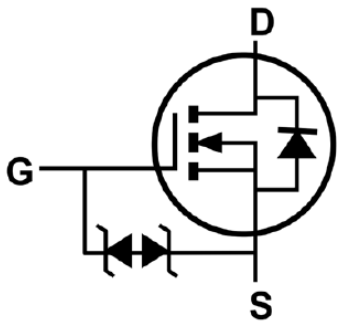
- Power Management in Notebook
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

Pin Configuration

LMN1072KTFF (DFN1006-3L)



PIN	Description
1	Gate
2	Source
3	Drain



Email:amy@lfc-semi.com www.lfc-semi.com

Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN1072KTFF	LMN1072K	TF	F	DFN1006-3L	10,000 PCS

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
2XWM	2	XWM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	±10	V
I_D	Continuous Drain Current (T_J=150℃)	0.75	A
I_{DM}	Pulsed Drain Current	3.0	A
I_S	Continuous Source Current (Diode Conduction)	0.3	A
P_D	Power Dissipation	0.35	W
T_J	Operating Junction Temperature	-55 to +150	℃
T_{STG}	Storage Temperature Range	-55 to +150	℃

Email:amy@lfc-semi.com www.lfc-semi.com

Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, ID=250uA	0.3	-	1	V
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V, V_{GS}=±10V	-	-	±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V	-	-	1	uA
		V_{DS}=20V, V_{GS}=0V T_J=85ºC	-	-	30	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=4.5V, ID=0.5A	-	210	350	mΩ
		V_{GS}=2.5V, ID=0.4A	-	300	450	
		V_{GS}=1.8V, ID=0.2A	-	420	700	
		V_{GS}=1.5V, ID=0.1A	-	600	1200	
g_{FS}	Forward Transconductance	V_{DS}=10V, ID=0.4A	-	1.0	-	S
V_{SD}	Diode Forward Voltage	I_S=0.15A, V_{GS}=0V	-	0.8	1.2	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=0.25A		0.73		nC
Q_{gs}	Gate-Source Charge			0.93		
Q_{gd}	Gate-Drain Charge			0.12		
C_{iss}	Input Capacitance	V_{DS}=16V, V_{GS}=0V, f=1MHz		60.7		pF
C_{oss}	Output Capacitance			9.7		
C_{rss}	Reverse Transfer Capacitance			5.4		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L=47Ω, I_D=0.2A, V_{GS}=4.5V, R_G=10Ω		5.1		ns
t_r	Turn-On Rise Time			7.4		
$t_{d(off)}$	Turn-Off Delay Time			26.7		
t_f	Turn-Off Fall Time			12.3		

Email:amy@lfc-semi.com www.lfc-semi.com

Typical Performance Characteristics

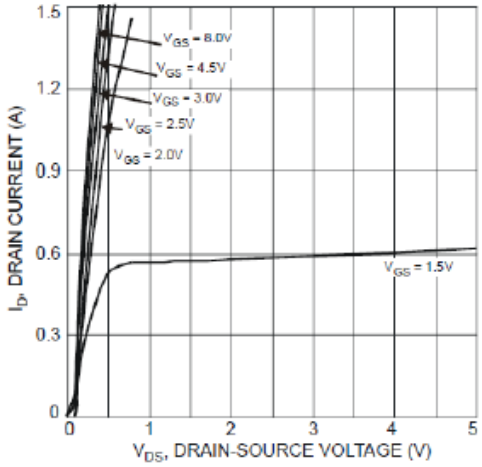


Fig. 1 Typical Output Characteristics

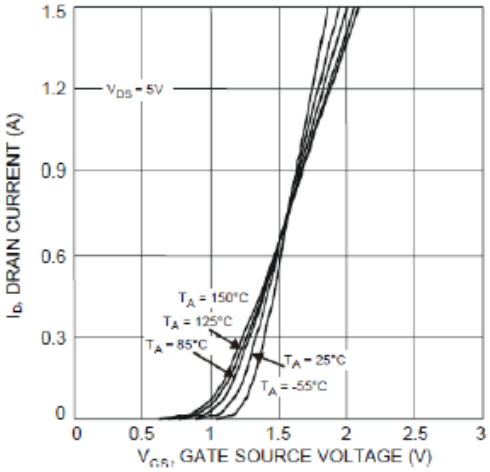


Fig. 2 Typical Transfer Characteristics

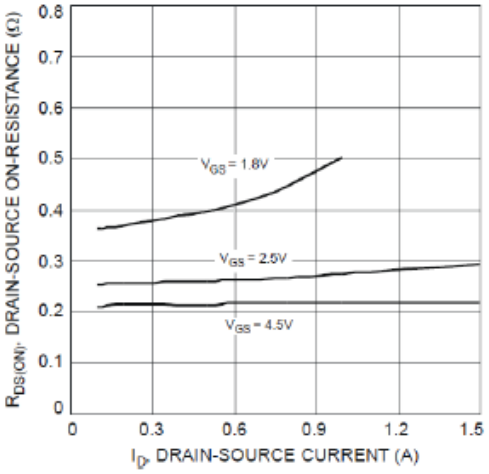


Fig. 3 Typical On-Resistance vs. I_D and V_{GS}

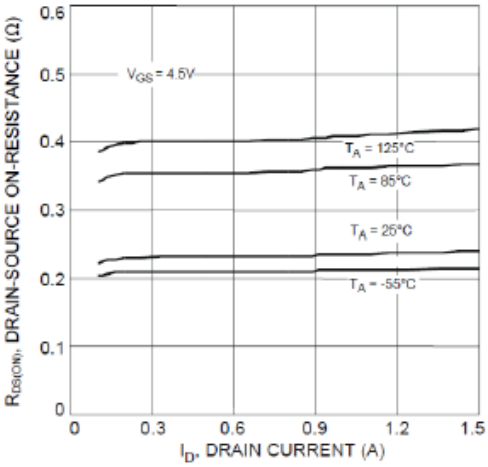


Fig. 4 Typical Drain-Source On-Resistance vs. I_D and T_J

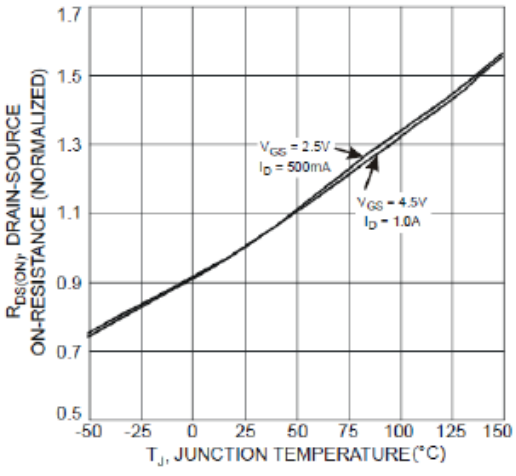


Fig. 5 On-Resistance Variation with T_J

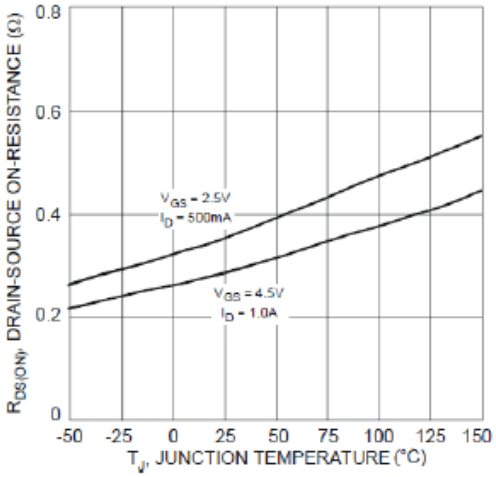


Fig. 6 On-Resistance Variation with T_J

Email:amy@lfc-semi.com www.lfc-semi.com

Typical Performance Characteristics(continue)

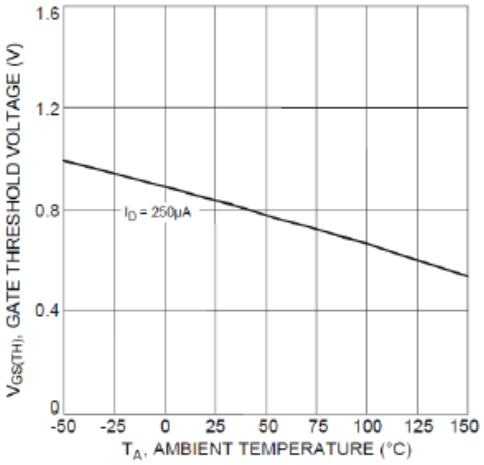


Fig. 7 Gate Threshold Variation vs. T_A

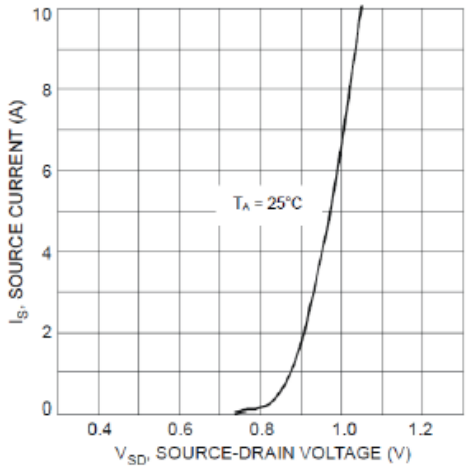


Fig. 8 Diode Forward Voltage vs. Current

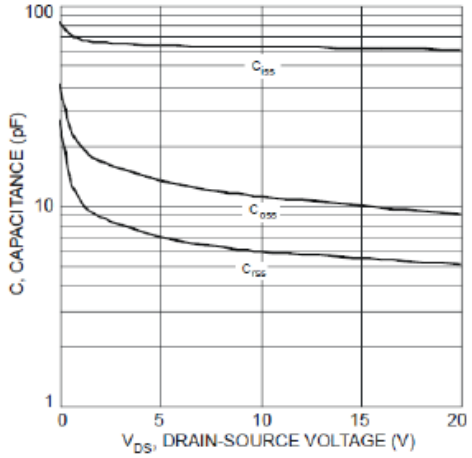


Fig. 9 Typical Capacitance

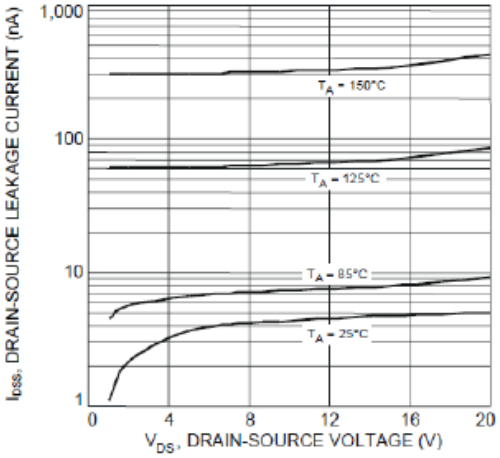


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

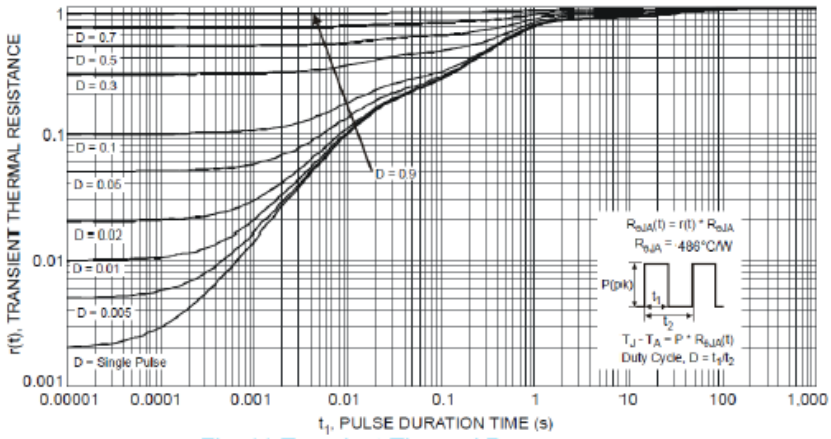


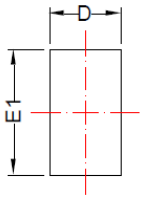
Fig. 11 Transient Thermal Response

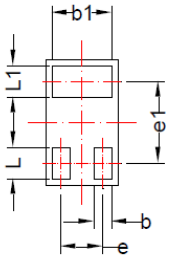
Email:amy@lfc-semi.com www.lfc-semi.com

Package Dimension:

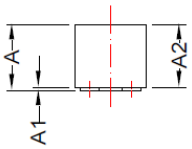
DFN1006-3L

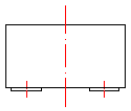
Package Dimension



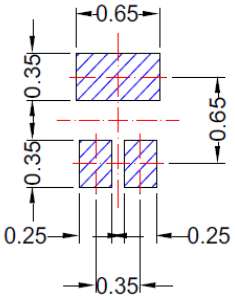


BACKSIDE VIEW





Recommended Land Pattern



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.60	0.018	0.024
A1	0.00	0.05	0.000	0.002
A2	0.40	0.60	0.016	0.024
b	0.10	0.20	0.004	0.008
b1	0.45	0.55	0.018	0.022
D	0.55	0.65	0.022	0.026
E1	0.95	1.05	0.037	0.041
e	0.35BSC		0.014BSC	
e1	0.65BSC		0.026BSC	
L	0.20	0.30	0.008	0.012
L1	0.20	0.30	0.008	0.012

NOTE:
DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH, NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

Email:amy@lfc-semi.com www.lfc-semi.com

NOTICE:

LFC Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all LFC Semiconductor products described or contained herein. LFC Semiconductor products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. LFC Semiconductor makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Information furnished is believed to be accurate and reliable. However LFC Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of LFC Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of LFC Semiconductor.